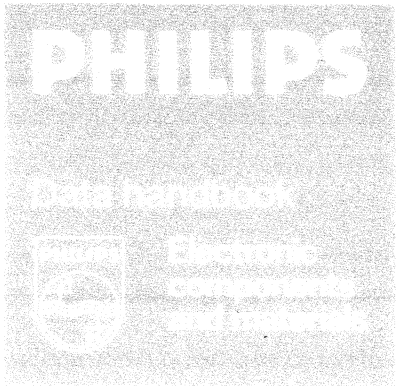


Integrated circuits

Book IC15N 1984
New series

FAST TTL Logic series

signetics

FAST TTL LOGIC SERIES

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks comprises:

T1 **Tubes for r.f. heating**

T2a **Transmitting tubes for communications, glass types**

T2b **Transmitting tubes for communications, ceramic types**

T3 **Klystrons, travelling-wave tubes, microwave diodes**

ET3 **Special Quality tubes, miscellaneous devices** (will not be reprinted)

T4 **Magnetrons**

T5 **Cathode-ray tubes**
Instrument tubes, monitor and display tubes, C.R. tubes for special applications

T6 **Geiger-Müller tubes**

T7 **Gas-filled tubes**
Segment indicator tubes, indicator tubes, dry reed contact units, thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes, associated accessories

T8 **Picture tubes and components**
Colour TV picture tubes, black and white TV picture tubes, colour monitor tubes for data graphic display, monochrome monitor tubes for data graphic display, components for colour television, components for black and white television and monochrome data graphic display

T9 **Photo and electron multipliers**
Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates

T10 **Camera tubes and accessories**

T11 **Microwave semiconductors and components**

T12 **Vidicons and Newvicons**

T13 **Image intensifiers**

T14 **Infrared detectors**

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

S1 **Diodes**
Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes(< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes

S2 **Power diodes, thyristors, triacs**
Rectifier diodes, voltage regulator diodes (> 1,5 W), rectifier stacks, thyristors, triacs

S3 **Small-signal transistors**

S4a **Low-frequency power transistors and hybrid modules**

S4b **High-voltage and switching power transistors**

S5 **Field-effect transistors**

S6 **R.F. power transistors and modules**

S7 **Microminiature semiconductors for hybrid circuits**

S8 **Devices for optoelectronics**
Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.

S9 **Power MOS transistors**

S10 **Wideband transistors and wideband hybrid IC modules**

INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks comprises:

EXISTING SERIES

IC1 **Bipolar ICs for radio and audio equipment**

IC2 **Bipolar ICs for video equipment**

IC3 **ICs for digital systems in radio, audio and video equipment**

IC4 **Digital integrated circuits**
CMOS HE4000B family

IC5 **Digital integrated circuits – ECL**
ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs

IC6 **Professional analogue integrated circuits**

IC7 **Signetics bipolar memories**

IC8 **Signetics analogue circuits**

IC9 **Signetics TTL logic**

IC10 **Signetics Integrated Fuse Logic (IFL)**

IC11 **Microprocessors, microcomputers and peripheral circuitry**

NEW SERIES

IC01N **Radio, audio and associated systems**
Bipolar, MOS

IC02N **Video and associated systems**
Bipolar, MOS

IC03N **Telephony equipment**
Bipolar, MOS

IC04N **HE4000B logic family**
CMOS

IC05N **HE4000B logic family uncased integrated circuits** (published 1984)
CMOS

IC06N **PC54/74HC/HCU/HCT logic families**
HCMOS

IC07N **PC54/74HC/HCU/HCT uncased integrated circuits**
HCMOS

IC08N **10K and 100K logic family**
ECL

IC09N **Logic series** (published 1984)
TTL

IC10N **Memories**
MOS, TTL, ECL

IC11N **Analogue - industrial**

IC12N **Semi-custom gate arrays & cell libraries**
ISL, ECL, CMOS

IC13N **Semi-custom integrated fuse logic**
IFL series 20/24/28

IC14N **Microprocessors, microcontrollers & peripherals**
Bipolar, MOS

IC15N **Logic series**
FAST TTL (published 1984)

Note

Books available in the new series are shown with their date of publication.

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

C1 **Assemblies for industrial use**
PLC modules, PC20 modules, HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices, hybrid ICs

C2 **Television tuners, video modulators, surface acoustic wave filters**

C3 **Loudspeakers**

C4 **Ferroxcube potcores, square cores and cross cores**

C5 **Ferroxcube for power, audio/video and accelerators**

C6 **Synchronous motors and gearboxes**

C7 **Variable capacitors**

C8 **Variable mains transformers**

C9 **Piezoelectric quartz devices**
Quartz crystal units, temperature compensated crystal oscillators, compact integrated oscillators, quartz crystal cuts for temperature measurements

C10 **Connectors**

C11 **Non-linear resistors**
Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)

C12 **Variable resistors and test switches**

C13 **Fixed resistors**

C14 **Electrolytic and solid capacitors**

C15 **Film capacitors, ceramic capacitors**

C16 **Permanent magnet materials**

C17 **Stepping motors and associated electronics**

C18 **D.C. motors**

C19 **Piezoelectric ceramics**

C20 **Wire-wound components for TVs and monitors**

PREFACE

Signetics would like to thank you for your interest in our FAST™ product line. Because of its wide customer acceptance, FAST has become the preferred high-performance Logic family of the 80's. We are proud to participate in and contribute to the dynamic growth of this market.

Each data sheet contained in this manual is designed to stand alone and reflect the latest DC and AC specifications for a particular product. Features of this first Signetics FAST Data Manual include:

- Availability and Functional Cross-Reference Guides
- A Circuit Characteristics Section
- A User's Guide
- Selected Application Notes
- A Chapter on Surface-Mounted Devices (SMD)
- Introduction of the SO surface-mounted package as a commercial option

New FAST part types are being released monthly. As you see new product announcements, you should contact your local Signetics sales office, representative or authorized distributor, or write Signetics, c/o Information Services at 811 East Arques Avenue, P.O. Box 3409, Sunnyvale, California 94088-3409, for the latest technical information.

In addition to FAST, Signetics Logic Division offers a line of commercial Logic products which spans a wide speed/power spectrum from 10K/100K ECL to HC/HCT High-Speed CMOS, and includes industry-standard families such as 4000 Series CMOS, 74, 74LS, and 74S Logic. Information on these product lines is also available from your nearest Signetics sales office, sales representative or authorized distributor.

Signetics Logic Division

THE HIGH-SPEED LOGIC OF THE 80's

PRODUCT DESCRIPTION

Signetics has combined advanced oxide-isolated fabrication techniques with standard TTL functions to create a new family designed for the 80's. The high operating speeds of FAST can push system operating speeds into areas previously reserved for 10K ECL, but with simple TTL design rules and single 5V power supplies. Low input loading allows the user to mix LS, ALS,and HCMOS in the same system without the need for translators and restrictive fanout requirements.

FAST circuits are pin-for-pin replacements for 74S types, but offer power dissipation 3-4 times lower and higher operating speeds. Existing systems can achieve much lower power by replacing the 74S types with the corresponding FAST devices, with no changes other than reducing the size of the power supply.

The input structure provides better noise immunity because of higher thresholds, while the oxide-isolation and new circuit techniques create devices that have less variation with temperature or supply voltage than existing TTL logic families. Signetics guarantees all ac parameters under realistic system conditions—across the supply voltage spread and the temperature range, and with heavy 50pF output loads.

The use of high-capacitance PNP inputs has been avoided, and clamping diodes have been added to both the inputs and outputs to prevent negative overshoots. High input breakdown voltages allow unused inputs to be tied directly to V_{CC} without pullup resistors.

Multiple sources and a complete family of powerful circuits combine to make Signetics FAST the logic choice of the 80's!

FEATURES

- **3ns propagation delays**
- **4mW/gate power dissipation**
- **Guaranteed AC performance over temperature and supply voltage spreads**
- **Improved input and output structures**
- **Standard TTL functions and pinouts**
- **Replacement for "S" types . . . 1/4 the power**
- **Designer's choice for new system designs**

THE SPEED/POWER SPECTRUM

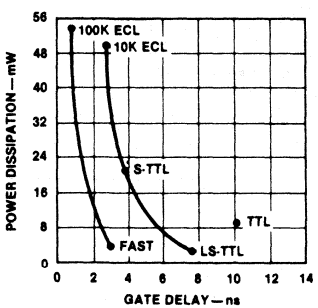


Figure 1

BASIC FAST GATE

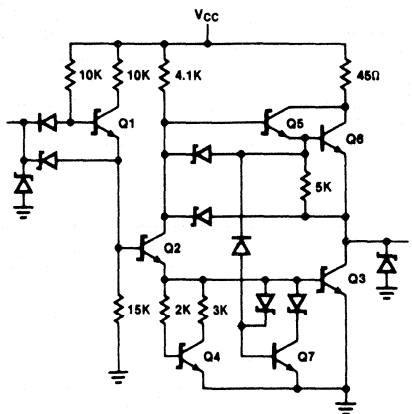


Figure 2

TRANSFER FUNCTIONS AT ROOM TEMPERATURE

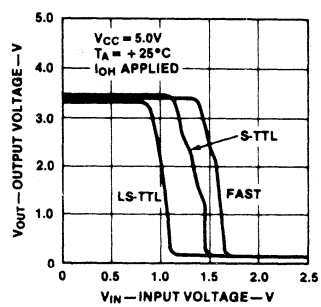


Figure 3

PROPAGATION DELAY VS LOAD CAPACITANCE
'F00

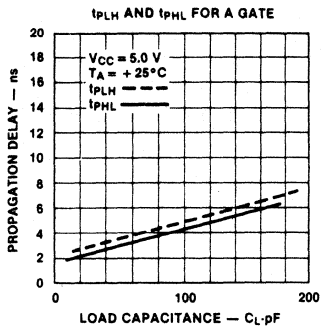


Figure 4

OUTPUT LOW CHARACTERISTICS
'F00

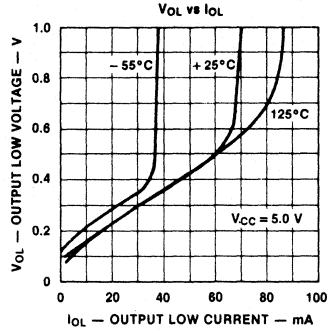


Figure 5

FALL TIME VS LOAD CAPACITANCE
'F00

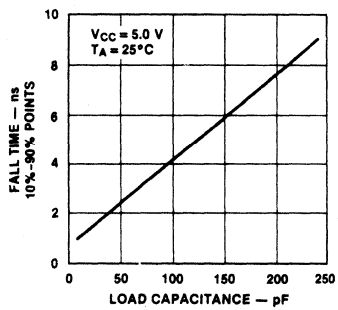


Figure 6

OUTPUT HIGH CHARACTERISTICS
'F00

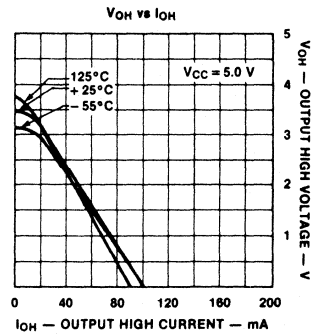


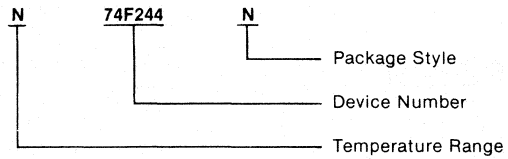
Figure 7

ORDERING INFORMATION

ORDERING INFORMATION

The Signetics FAST products are available in a variety of packages and two temperature ranges. The correct ordering code of part number for the devices is an alphanumeric sequence as explained below. The commercial range (74FXX) devices are available in plastic dual-in-line (DIP) and SO packages, and the military range (54FXX) devices are available in ceramic DIP and leadless chip carrier (LLCC). All devices are not available in both temperature ranges or all packages. The ordering codes on the individual data sheets indicate the normal or planned availability of the product. However, the availability of specifc part numbers can be obtained from your local Signetics sales office or franchised distributor.

ORDERING CODE



TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE STYLE
N = Commercial Range 0°C to +70°C	74F244	N = Plastic DIP D = SO Plastic
S = Military Range −55°C to +125°C	54F244	F = Ceramic DIP G = Leadless Chip Carrier

PRODUCT STATUS AND DEFINITIONS

DEFINITION OF TERMS

Data Sheet Identification	Product Status	Definition
Preview	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Advance Information	Sampling or Pre-Production	This data sheet contains advance information and specifications are subject to change without notice.
Preliminary	First Production	This data sheet contains preliminary data and supplementary data will be published at a later data. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Section 1
Selection Guide

NUMERICAL INDEX

NUMERICAL INDEX

AVAILABILITY GUIDE

DEVICE	DESCRIPTION	AVAIL-ABILITY
74F00	Quad 2-Input NAND Gate	A
74F02	Quad 2-Input NOR Gate	A
74F04	Hex Inverter	A
74F08	Quad 2-Input AND Gate	A
74F10	Triple 3-Input NAND Gate	A
74F11	Triple 3-Input AND Gate	A
74F13	Dual 4-Input NAND Schmitt Trigger	A
74F14	Hex Schmitt Trigger	A
74F20	Dual 4-Input NAND Gate	A
74F32	Quad 2-Input OR Gate	A
74F37	Quad 2-Input NAND Buffer	1H 84
74F38	Quad 2-Input NAND Buffer, OC	1H 84
74F40	Dual 4-Input NAND Buffer	1H 84
74F64	4-2-3-2 Input AND/OR Invert Gate	A
74F74	Dual D-Type Flip-Flop	A
74F85	4-Bit Magnitude Comparator	1H 84
74F86	Quad 2-Input Exclusive-OR Gate	A
74F109	Dual JK Flip-Flop	A
74F112	Dual JK Flip-Flop	2H 84
74F113	Dual JK Flip-Flop	2H 84
74F114	Dual JK Flip-Flop	2H 84
74F132	Quad 2-Input NAND Schmitt Trigger	A
74F138	1-of-8 Decoder/Demultiplexer	A
74F139	Dual 1-of-4 Decoder/Demultiplexer	A
74F148	8-Bit Priority Encoder	2H 84
74F151	8-Input Multiplexer	1H 84
74F153	Dual 4-Input Multiplexer	2H 84
74F157	Quad 2-Input Multiplexer	A
74F158	Quad 2-Input Multiplexer	A
74F160A	BCD Decade Counter, Asynch Reset	2H 84
74F161A	4-Bit Binary Counter, Asynch Reset	2H 84
74F162A	BCD Decade Counter, Synch Reset	2H 84
74F163A	4-Bit Binary Counter, Synch Reset	2H 84
74F164	8-Bit SIPO Shift Register	2H 84
74F168	4-Bit Up/Down Decade Counter (3-State)	2H 84
74F169	4-Bit Up/Down Binary Counter (3-State)	2H 84
74F174	Hex D Flip-Flop with Common Master Reset	2H 84
74F175	Quad D Flip-Flop with Common Master Reset	2H 84
74F181	4-Bit Arithmetic Logic Unit	2H 84
74F182	Carry Lookahead Generator	2H 84
74F189	4-Bit Random Access Memory (3-State)	1985
74F190	Up/Down Decade Counter	2H 84
74F191	Up/Down Binary Counter	2H 84
74F192	Up/Down Decade Counter	2H 84
74F193	Up/Down Binary Counter	2H 84
74F194	4-Bit Bidirectional Universal Shift Register	A
74F195	4-Bit Parallel Access Shift Register	1H 84
74F198*	8-Bit Bidirectional Universal Shift Register	1985
74F240	Octal Inverting Bus/Line Driver (3-State)	A
74F241	Octal Bus/Line Driver (3-State)	A

DEVICE	DESCRIPTION	AVAIL-ABILITY
74F242	Quad Bus Transceiver (3-State)	A
74F243	Quad Bus Transceiver (3-State)	A
74F244	Quad Bus/Line Driver (3-State)	A
74F245	Octal Bus Transceiver (3-State)	1H 84
74F251	8-Input Multiplexer (3-State)	1H 84
74F253	Dual 4-Input Multiplexer (3-State)	2H 84
74F256	Dual 4-Bit Addressable Latch	A
74F257	Quad 2-Input Multiplexer (3-State)	A
74F258	Quad 2-Input Multiplexer (3-State)	A
74F259	8-Bit Addressable Latch	A
74F269	8-Bit Up/Down Counter (3-State)	1H 84
74F273	Octal D Flip-Flop	1H 84
74F280A	9-Bit Parity Generator/Checker	A
74F283	4-Bit Adder	1985
74F298	Quad 2-Input Multiplexer	1H 84
74F299	Octal Shift/Storage Register (3-State)	2H 84
74F322	Octal Shift/Storage Register (3-State)	2H 84
74F323	Octal Shift/Storage Register (3-State)	2H 84
74F350	4-Bit Shifter (3-State)	A
74F352	Dual 4-Input Multiplexer (Inverted '153)	2H 84
74F353	Dual 4-Input Multiplexer (Inverted '253)	2H 84
74F365	Hex Buffer with Common Enable (3-State)	1H 84
74F366	Hex Inverter with Common Enable (3-State)	1H 84
74F367	Hex Buffer, 4-Bit and 2-Bit (3-State)	1H 84
74F368	Hex Inverter, 4-Bit and 2-Bit (3-State)	1H 84
74F373	Octal D Latch (3-State)	A
74F374	Octal D Flip-Flop (3-State)	A
74F377	Octal D-Type Flip-Flop with Enable	A
74F378	Hex D Flip-Flop with Enable	2H 84
74F379	Quad D Flip-Flop with Enable	2H 84
74F381*	4-Bit Arithmetic Logic Unit	1985
74F382*	4-Bit Arithmetic Logic Unit	1985
74F384*	8-Bit Serial/Parallel Two's Complement Multiplier	1985
74F385*	Quad Serial Adder/Subtractor	1985
74F395	4-Bit Cascadable Shift Register (3-State)	1H 84
74F398	4-Bit Flip-Flop, True and Complement Outputs	2H 84
74F399	4-Bit Flip-Flop, True and Complement Outputs	2H 84
74F412	Multi-Mode Buffered Latch (3-State)	1985
74F521	Octal Comparator	A
74F524	8-Bit Register Comparator (OC)	2H 84
74F533	Inverting Octal D Latch (3-State)	A
74F534	Inverting Octal D Flip-Flop (3-State)	A
74F545	Octal Bus Transceiver (3-State)	1H 84
74F568	4-Bit Binary Up/Down Counter (3-State)	2H 84
74F569	4-Bit Decade Up/Down Counter (3-State)	2H 84
74F579	8-Bit Up/Down Counter, Common I/O (3-State)	2H 84
74F588	GPIB Compatible Octal Transceiver	1H 84
74F595*	8-Bit Shift Register with Output Latch	1985

*Data sheets soon to be available. Contact nearest Signetics sales office.

AVAILABILITY GUIDE

DEVICE	DESCRIPTION	AVAIL-ABILITY
74F597*	8-Bit Shift Register with Input Latch	1985
74F598*	8-Bit Shift Register with Input Latch	1985
74F604	Dual 8-Bit Latch (3-State)	1H 84
74F605	Dual 8-Bit Latch (OC)	1H 84
74F620	Octal Bus Transceiver (3-State)	1H 84
74F621	Octal Bus Transceiver (3-State)	1H 84
74F622	Octal Bus Transceiver (OC)	1H 84
74F623	Octal Bus Transceiver (3-State)	1H 84
74F630	Memory Error Detector/Corrector (3-State)	2H 84
74F631	Memory Error Detector/Corrector (OC)	2H 84
74F646	Octal Bus Transceiver and Register (3-State)	1H 84
74F647	Octal Bus Transceiver and Register (OC)	1H 84
74F648	Octal Bus Transceiver and Register (3-State)	1H 84
74F649	Octal Bus Transceiver and Register (OC)	1H 84
74F655	Octal Inverting Buffer with Parity Generator-Checker (3-State)	A

DEVICE	DESCRIPTION	AVAIL-ABILITY
74F656	Octal Buffer with Parity Generator-Checker (3-State)	A
74F657	Octal Bus Transceiver with Parity Generator-Checker (3-State)	2H 84
74F673	16-Bit Serial-In/Parallel-Out Shift Register (3-State)	1985
74F674	16-Bit Parallel-In/Serial-Out Shift Register (3-State)	1985
74F675	16-Bit Serial-In/Parallel-Out Shift Register with SO Capability	1985
74F676	16-Bit Parallel-In/Serial-Out Shift Register with SO Capability	1985
74F779	8-Bit Counter (3-State)	2H 84
74F784*	8-Bit Serial/Parallel Multiplier (with Adder/Subtractor)	1985
74F3037*	Quad 2-Input 30Ω Transmission Line Driver	A
74F3040*	Dual 4-Input 30Ω Transmission Line Driver	A

*Data sheets soon to be available. Contact nearest Signetics sales office.

FAST ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to + 70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = − 55°C to + 125°C
Plastic DIP	N74F---N	
Plastic SO(1)	N74F---D	
Ceramic DIP		S54F---F
Ceramic LLCC(2)		S54F---G

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is ceramic surface-mounted leadless chip carrier.

FUNCTION SELECTION GUIDE

GATES

FUNCTION	DEVICE NUMBER
Inverters	
Hex Inverter	54/74F04
Hex Inverter Schmitt Trigger	74F14
NAND	
Quad 2-Input	54/74F00
Triple 3-Input	54/74F10
Dual 4-Input, Schmitt Trigger	74F13
Dual 4-Input	54/74F20
Quad 2-Input, Schmitt Trigger	74F132
AND	
Quad 2-Input	54/74F08
Triple 3-Input	54/74F11
NOR	
Quad 2-Input	54/74F02
OR	
Quad 2-Input	54/74F32
Exclusive-OR	
Quad	54/74F86
Combination Gates	
4-2-3-2 Input AND-OR-Invert	74F64

DUAL FLIP-FLOPS

FUNCTION	DEVICE NUMBER	CLOCK EDGE	SET	CLEAR
D	54/74F74	↑	LOW	LOW
JK	54/74F109	↑	LOW	LOW
JK	74F112	↓	LOW	LOW
JK	74F113	↓	LOW	
JK	74F114	↓	LOW	LOW

MULTIPLE FLIP-FLOPS

FUNCTION	DEVICE NUMBER	RESET LEVEL	CLOCK EDGE	OUTPUT
Quad D	54/74F175	LOW	↑	True Comp
Quad D with Enable	74F379		↑	True Comp
Hex D	74F174	LOW	↑	True
Hex D with Enable	74F378		↑	True
Octal D	74F273	LOW	↑	True
Octal D, 3-State	54/74F374		↑	True
Octal D, 3-State	74F534		↑	Comp
Octal D with Enable	74F377		↑	True

OTHER REGISTERS, REGISTER FILES

FUNCTION	DEVICE NUMBER	BITS	SERIAL ENTRY	PARALLEL ENTRY	CLOCK
Quad 2 Port	74F298	4 x 2		2D (mux)	↓
Quad 2 Port	74F398	4 x 2		2D (mux)	↑
Quad 2 Port	74F399	4 x 2		2D (mux)	↑

FUNCTION SELECTION GUIDE

LATCHES

FUNCTION	DEVICE NUMBER	COMMON CLEAR (LEVEL)	ENABLE INPUT (LEVEL)	OUTPUT
Dual 4-Bit Addressable	74F256	LOW	1 (L)	True
Dual 4-Bit Addressable	74F259	LOW	1 (H)	True
Octal, 3-State	54/74F373		1 (H)	True
Octal Inverting, 3-State	74F533		1 (H)	Comp
Multi-Mode Buffered, 3-State	74F412*	LOW	1 (L), 2 (H)	True

MULTIPLEXERS

FUNCTION	DEVICE NUMBER	ENABLE INPUT (LEVEL)	SELECT INPUTS	OUTPUT
Quad 2-Input	54/74F157	1 (L)	1	True
Quad 2-Input	74F158	1 (L)	1	True
Quad 2-Input, 3-State	54/74F257		1	True
Quad 2-Input, 3-State	74F258		1	Comp
Dual 4-Input	54/74F153	2 (L)	2	True Comp
Dual 4-Input	74F352	2	2	Comp
Dual 4-Input, 3-State	54/74F253		2	True
Dual 4-Input, 3-State	74F353	2	2	Comp
8-Input	74F151	1 (L)	3	True Comp
8-Input, 3-State	54/74F251		1	True Comp

DECODER/DEMULTIPLEXERS

FUNCTION	DEVICE NUMBER	ADDRESS INPUTS	ENABLE LEVEL	OUTPUT LEVEL
Dual 1-of-4	74F139	2 + 2	1 (L) + 1 (L)	4 (L) + 4 (L)
1-of-8	54/74F138	3	2 (L), 1 (H)	8 (L)

BUFFERS, DRIVERS AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad 2-Input NAND Buffer	74F37	Comp
Quad 2-Input NAND Buffer, OC	74F38	Comp
Dual 4-Input NAND Buffer	74F40	Comp
Quad 2-Input NAND Transmission Driver	74F3037*	Comp
Dual 4-Input NAND Transmission Driver	74F3040*	Comp
Octal Transceiver	74F621	True
Octal Transceiver	74F622	Comp
Octal Transceiver and Registers	74F647	True
Octal Transceiver and Registers	74F649	Comp

*Data sheets soon to be available. Contact nearest Signetics sales office.

FUNCTION SELECTION GUIDE

SHIFT REGISTERS

FUNCTION	DEVICE NUMBER	BITS	SERIAL ENTRY	PARALLEL ENTRY	CLOCK
Serial-In/Parallel-Out	74F164	8	D_{sa}, D_{sb}		⎍
Serial-In/Parallel-Out Output Latch, 3-State	74F595*	8	D_s		⎍
Serial-In/Serial-Out/Parallel-Out, 3-State	74F673	16	SI/O		⎍
Serial-In/Serial-Out/Parallel-Out	74F675	16	D		⎍ ⎍
Serial-In/Parallel-In/Serial-Out, Parallel-Out	74F195	4	J,K	4D	⎍
Serial-In/Parallel-In/Serial-Out, Parallel-Out	74F598*	8	D_{so}, D_{si}	8 I/O	⎍
Serial-In/Parallel-In/Serial-Out	74F674	16	SI/O	SI/O, 16D	⎍
Serial-In/Parallel-In/Serial-Out	74F676	16	SI	16D	⎍
Serial-In/Parallel-In/Parallel-Out Shift Right, 3-State	74F395	4	D_s	4D	⎍
Serial-In/Parallel-In/Serial-Out, Parallel-Out, 3-State	74F322	8	D_0, D_1	8 I/O	⎍
Serial-In/Parallel-In/Parallel-Out	54/74F194	4	D_{sr}, D_{sl}	4D	⎍
Serial-In/Parallel-In/Parallel-Out, Bidirectional	74F198*	8	D_{sr}, D_{sl}	8D	⎍
Serial-In/Parallel-In/Serial-Out, Parallel-Out, 3-State	74F299	8	D_{s0}, D_{s7}	8 I/O	⎍
Serial-In/Parallel-In/Serial-Out, Parallel-Out, 3-State	74F323	8	D_{s0}, D_{s7}	8 I/O	⎍
Parallel-In/Serial-Out Input Latch	74F597*	8	D_s	8D	⎍
Parallel-In/Parallel-Out, 3-State	74F350	4	I_{-3}-I_{+3}	4Y	
Parallel-In/Parallel-Out, 3-State	74F604	16		A_1-A_8, B_1-B_8	⎍
Parallel-In/Parallel-Out, OC	74F605	16		A_1-A_8, B_1-B_8	⎍
Parallel-In/Parallel-Out, True and Complement Output	74F398	8	S	I_{0a}-I_{0d}, I_{1a}-I_{1d}	⎍
Parallel-In/Parallel-Out	74F399	8	S	I_{0a}-I_{0d}, I_{1a}-I_{1d}	⎍

COUNTERS

FUNCTION	DEVICE NUMBER	MODULUS	PARALLEL ENTRY	PRESETTABLE	CLOCK EDGE
Synchronous	74F160	10	S	X	⎍
Synchronous	74F161	16	S	X	⎍
Synchronous	74F162	10	S	X	⎍
Synchronous	74F163	16	S	X	⎍
Up/Down	74F168	10	S	X	⎍
Up/Down	74F169	16	S	X	⎍
Up/Down	74F190	10	A	X	⎍
Up/Down	74F191	16	A	X	⎍
Up/Down	74F192	10	A	X	⎍
Up/Down	74F193	16	A	X	⎍
Up/Down	74F269	8	S	X	⎍
Up/Down	74F579	8	S (I/O)	X	⎍
Up/Down, 3-State Multiplexed	74F779	8	S (I/O)	X	⎍

THREE-STATE BUFFERS, DRIVERS AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad Bus Transceiver	74F242	Comp
Quad Bus Transceiver	74F243	True
Hex Buffer	74F365	True
Hex Inverter	74F366	Comp
Hex Buffer, 4-Bit and 2-Bit	74F367	True
Hex Inverter, 4-Bit and 2-Bit	74F368	Comp
Octal Buffer	54/74F240	Comp
Octal Buffer	54/74F241	True
Octal Buffer	54/74F244	True
Octal Buffer with Parity	74F655	Comp
Octal Buffer with Parity	74F656	True
Octal Transceiver	74F245	True
Octal Transceiver	74F545	True
Octal Transceiver with IEEE-488 Termination Resistors	74F588	True
Octal Transceiver	74F620	Comp
Octal Transceiver	74F623	True
Octal Transceiver with Parity	74F657	True
Octal Transceiver/Register	74F646	True
Octal Transceiver/Register	74F648	Comp

*Data sheets soon to be available. Contact nearest Signetics sales office.

FUNCTION SELECTION GUIDE

PRIORITY ENCODERS

FUNCTION	DEVICE NUMBER	INPUT ENABLE (LEVEL)	INPUT/OUTPUT (LEVEL)
8-to-3	74F148	LOW	Active-LOW

ARITHMETIC FUNCTIONS

FUNCTION	DEVICE NUMBER
4-Bit ALU	74F181
4-Bit ALU	74F381*
4-Bit ALU with Overflow Output for Two's Complement	74F382*
4-Bit Binary Full Adder with FAST Carry	54/74F283
Lookahead Carry Generator	74F182
Quad Serial Adder/Subtractor	74F385*

COMPARATORS

FUNCTION	DEVICE NUMBER
4-Bit Comparator	74F85
8-Bit Comparator	54/74F521
8-Bit Register Comparator	74F524

PARITY

FUNCTION	DEVICE NUMBER
9-Bit Odd/Even Parity Generator/Checker	54/74F280A

SPECIAL FUNCTIONS

FUNCTION	DEVICE NUMBER
16-Bit Error Detection	74F630
16-Bit Error Detection/Correction Circuit	74F631
64-Bit RAM	74F189
8-Bit Serial/Parallel Two's Complement Multiplier	74F384*
2-Bit Serial/Parallel (with Adder/Subtractor)	74F784*

*Data sheets soon to be available. Contact nearest Signetics sales office.

Section 2
Quality and Reliability

QUALITY AND RELIABILITY

SIGNETICS LOGIC QUALITY

Signetics' Logic Division has put together a winning process for manufacturing ICs with built-in quality and reliability. We're striving to ship zero defects, and current quality levels demonstrate our commitment to this goal. Quality guarantees are continually being reviewed to reflect the tangible improvements we have made.

The digital ICs produced in the Logic Division must meet rigid criteria as defined by our design rules and evaluated in a thorough product characterization process. The capabilities of our manufacturing process are measured and the results evaluated and reported through our corporate-wide data base system, QA05. The SURE (Systematic Uniform Reliability Evaluation) program monitors the performance of our product in a variety of accelerated environmental stress conditions. All of these programs and systems are intended to prevent product-related problems and to inform our customers and employees of our progress in achieving zero defects.

RELIABILITY BEGINS WITH THE DESIGN

Reliability and quality must begin with design. No amount of extra testing or inspection will produce reliable ICs from a design that is inherently unreliable. Signetics follows very strict design and layout practices with its digital circuits. To eliminate the possibility of metal migration, current density in any path cannot exceed 2×10^5 amps/cm^2. Layout rules are followed to minimize the possibility of shorts, circuit anomalies, and SCR type latch-up effects. Numerous ground-to-substrate connections are required to ensure that the entire chip is at the same ground potential, thereby precluding internal noise problems.

PRODUCT CHARACTERIZATION

Before a new design is released, the characterization phase must be completed so that the distribution of parameters resulting from lot-to-lot variations is well within specified limits. Such extensive characterization data also provides a basis for identifying unique application-related problems which are not part of normal data sheet guarantees. Characterization takes place from $-55°C$ to $+125°C$ and a $+10\%$ supply voltage.

QA05

The QA05 system collects the results of product assurance testing on all finished goods lots and feeds this data back to concerned organizations where appropriate action can be taken. The QA05 reports EPA (Estimated Process Average) and AOQ (Average Outgoing Quality) results for electrical, visual/mechanical, hermeticity, and documentation audits. Data from this system is available on request.

THE SURE PROGRAM

The SURE (Systematic Uniform Reliability Evaluation) program audits/monitors products from all Signetics' divisions under a variety of accelerated environmental stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements.

The SURE III program has two major functions: long-term accelerated stress performance audit and a short-term accelerated stress monitor. In the case of logic products, samples are selected which represent all generic product groups in all wafer fabrication and assembly locations. A series of detailed specifications (3230-009X) defines the criteria by which sample selection and evaluation testing is conducted.

THE LONG-TERM AUDIT

One-hundred devices from each generic family are subjected to each of the following stresses every eight weeks:

- High Temperature Operating Life: $T_j = 150°C$, 1000 hours, static biased or dynamic operation, as appropriate (worst-case bias configuration is chosen);
- High Temperature Storage: $T_j = 150°C$, 1000 hours;
- Temperature-Humidity Biased Life: 85 °C, 85% relative humidity, 1000 hours, static biased;
- Temperature Cycling (Air-to-Air): $-65°C$ to $+150°C$, 1000 cycles.

THE SHORT-TERM MONITOR

Every other week a 50-piece sample from each generic family is run to 168 hours of pressure pot (15 psig, 121 °C, 100% saturated steam) and 300 cycles of thermal shock ($-65°C$ to $+150°C$).

In addition, each Signetics assembly plant performs SURE product monitor stresses weekly on each generic family and molded package, by pin count and frame type. Fifty pieces are run on each stress, in pressure pot to 96 hours, thermal shock to 300 cycles.

SURE REPORTS

The data from these test matrices provides a basic understanding of product capability, an estimated failure rate resulting from each stress, and an indication of major failure mechanisms. This data is compiled periodically and is available to customers upon request.

RELIABILITY ENGINEERING

In addition to the product performance monitors encompassed in the Logic SURE Program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering program are:

- evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities and subcontractors;
- device or generic group failure rate studies;
- advanced environmental stress development;
- failure mechanism characterization.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE monitor; however, more highly accelerated conditions and extended durations typify the engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity,are also included in the evaluation programs.

FAILURE ANALYSIS

The SURE Program and the Reliability Engineering Program both include failure analysis activities and are complemented by Corporate, Divisional, and Plant Failure Analysis departments. These engineering units provide a service to our customers who desire detailed failure analysis support, and they in turn provide Signetics with the technical understanding of the failure

QUALITY AND RELIABILITY

modes and mechanisms actually experienced in service. This information is essential feedback, necessary for the continued assessment of the applicability of the stress conditions utilized to measure product performance.

ZERO DEFECTS PROGRAM

Industry Requires Improved Product Quality

In recent years United States industry, and particularly those of you who buy integrated circuits, has increasingly demanded improved product quality. We at Signetics believe you have every right to expect quality products. If you buy components from a quality conscious manufacturer, the reward can be summed up in the words, *lower cost of ownership*.

Those of you who invest in costly test equipment and engineering to assure that incoming products meet your specifications have a special understanding of the cost of ownership. And your cost does not end there; you are also burdened with inflated inventories, lengthened lead times, and more rework.

Signetics Understands Customers' Needs

Signetics has long had an organization of quality professionals inside the operating units, coordinated by a corporate quality department. This organization provides leadership, feedback, and direction for achieving our high level of quality. Special programs are targeted on specific quality issues. For example, a program to reduce electrically defective units improved outgoing quality levels by an order of magnitude.

In 1980 we recognized that in order to achieve outgoing levels on the order of 100 PPM (parts per million), down from an industry practice of 10,000 PPM, we needed to supplement our traditional quality programs with one that encompassed all activities and all levels of the company. Such unprecedented low defect levels could only be achieved by contributions from all employees, from the R&D laboratory to the shipping dock. In short, a program that would effect a total cultural change within Signetics in our attitude toward quality.

This new concept is based on the 14-step quality improvement program developed by Phil Crosby and outlined in his book *Quality is Free*. The program focuses on defect prevention as the means of attaining improved quality.

Quality Pays Off for Our Customers

Signetics' dedicated programs in product quality improvement, supplemented by close working relationships with many of our customers, have improved outgoing product quality more than twenty-fold. Today, many major customers no longer test Signetics circuits. Incoming product moves directly from the receiving dock to the production line, greatly accelerating throughput and reducing inventories. Additional customers have pared significantly the amount of sampling done on our products. Others are beginning to adopt these cost-saving practices.

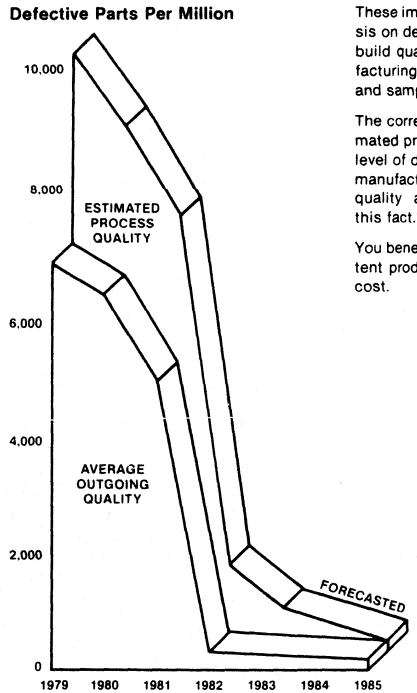
We closely monitor the electrical, visual, and mechanical quality of all our products and review each return to find and correct the cause. Since 1981, over 90% of our customers report a significant improvement in overall quality.

At Signetics, quality means more than working circuits. It means on-time delivery of the *right* quantity of the *right* product at

LOGIC PRODUCT QUALITY GOALS (1984-1986)

	ELECTRICAL	VISUAL/MECHANICAL	CUMULATIVE
1984 EPQ/AOQ Targets, PPM	150/100	500/250	650/350
1985 EPQ/AOQ Targets, PPM	100/50	300/100	400/150
1986 EPQ/AOQ Targets, PPM	50/10	100/50	150/60

This graph shows how dramatically electrical, mechanical, and visual defects have been reduced across all product lines.



These improvements result from our emphasis on defect prevention which allows us to build quality into the product during manufacturing, instead of relying on screening and sampling to remove defective parts.

The corresponding improvement in the estimated process quality (which measures the level of defective units produced during the manufacturing process prior to outgoing quality assurance) conclusively supports this fact.

You benefit from improved and more consistent product conformance at lower product cost.

QUALITY AND RELIABILITY

the *agreed upon* price. Our quality improvement programs extend out from the traditional areas of product conformance into the administrative areas which affect order entry, scheduling, delivery, shipping, and invoicing.

Ongoing Quality Programs at Signetics

The "14-Step" Quality Improvement Program or "Do it Right the First Time"

The intent of this innovative program is to change the perception of Signetics' employees that somehow quality is solely a manufacturing issue where some level of defects is inevitable. This attitude has been replaced by one of acceptance of the fact that all errors and defects are preventable, a point of view shared by technical and administrative functions equally, and, we are sure, welcomed by our customers.

This program is company-wide and top down. It is personally led by President Charles Harwood who, with his staff, forms the corporate quality improvement team which implements corporate quality policy. Supporting the corporate quality improvement team are more than 40 quality improvement teams representing every unit in the company, each led by the unit manager.

Key components of the program are the Quality College, the "Make Certain" Program, Corrective Action Teams, and the Error Cause Removal System.

The core concepts of doing it right the first time are embodied in the four absolutes of quality:

1. The definition of quality is conformance to requirements.
2. The system to achieve quality improvement is prevention.
3. The performance standard is zero defects.
4. The measurement system is the cost of quality.

Quality College

Almost continuously in session, the Quality College is a prerequisite for all management and technical employees. The intensive two-day curriculum is built around the four "absolutes" of quality; colleges are conducted at company facilities throughout the world. More than 3000 employees have attended.

"Making Certain" — Administrative Quality Improvement

Signetics' experience has shown that the largest source of errors affecting product and service quality is found in paperwork and in other administrative functions. The "Make Certain" program focuses the attention of management and administrative personnel on error prevention, beginning with each employee's own actions.

This program promotes defect prevention in three ways: by educating employees as to the impact and cost of administrative errors, by changing attitudes from accepting occasional errors to one of accepting a personal work standard of zero defects, and by providing a formal mechanism for preventing errors.

Corrective Action Teams

Employees with the perspective, knowledge, and necessary skills are formed into ad hoc groups called Correction Action Teams. These teams, the major force within the company for quality improvement, resolve administrative, technical and manufacturing problems.

Error Cause Removal (ECR) System

The ECR System permits our employees to report to management any impediment to doing their job right the first time. Once reported, management is obliged to respond promptly with a corrective program. Doing it right the first time in all company activities produces lower cost of ownership through product defect prevention and in all other ways meets our customers' expectations.

Product Quality Program

To reduce defects in outgoing products to nearly immeasurable levels, we created the Product Quality Program. This is managed by the Product Engineering Council, a task force composed of the top product engineering and test professionals in the company. This group:

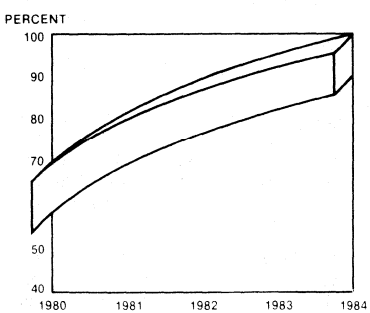
1. Sets aggressive product quality improvement goals.
2. Provides corporate-level visibility and focuses on problem areas.
3. Serves as a corporate resource for any group requiring assistance in quality improvement.
4. Drives quality improvement projects.

As a result of this aggressive program, every major customer who reports back to us on product performance is reporting significant progress.

Performance to Schedule

Signetics' attention to administrative quality has resulted in improved performance to schedule. Doing it right the first time means on-time delivery.

On-Time Delivery



Signetics is Organized for Quality

Managing Cultural Change — The "14-Step" Program
- Quality College
- Quality Improvement Teams
- "Make Certain" Program
- Corrective Action Teams
- Error Cause Removal System

Engineering Quality into the Product
- SURE Program
- Manufacturing Plant Product Monitoring
- Qualification Programs
- Vendor Certification Programs
- Product Quality Program

Supporting Quality Maintenance
- Product Line
- Quality and Reliability Assurance
- Corporate Quality and Reliability
- Failure Analysis Laboratories
- Reliability Data Base
- Statistical Quality Control

Standard Quality Programs

"SURE" — The acronym stands for ***S***ystematic ***U***niform ***Q***uality ***E***valuation and is an ongoing product evaluation first introduced in 1964. This activity provides our customers and us with an ongoing view of reliability performance of all generic families of Signetics' products.

Product Monitor — Each manufacturing facility monitors its generic product groups with short-term stress tests, pressure pot and thermal shock. These tests are performed weekly, and performance trends are

QUALITY AND RELIABILITY

monitored to ensure that unwanted process deviations are spotted quickly and corrected before appearing in products received by our customers.

Qualification — Formal qualification procedures are required for all new or changed products, processes and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by the corporation and by the quality organizations of the product line that will operate the facility. After qualification, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that the products can meet rigorous failure rate requirements. New or changed processes are qualified similarly.

Failure Analysis — This vital function is conducted by product line and plant failure analysis units coordinated through the corporate failure analysis group, a part of corporate reliability engineering. Our ten failure analysis groups will be expanded to 16 by the end of 1984 in our ongoing effort to accelerate and improve our understanding of product failure mechanisms.

Reliability Data Base — This computerized data base contains product reliability information collected from around the world. It is updated and published quarterly in "Signetics Product Reliability Summary."

Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly procedures.

Vendor Certification Program — Our vendors are taking ownership of their own product quality by establishing improved process control and inspection systems. They subscribe to the zero defects philosophy. Progress has been excellent. Through intensive work with vendors, we have improved our lot acceptance rate on incoming materials as shown in the graph. Simultaneously, waivers of incoming material have been eliminated.

Material Waivers

1983 — 0 (Goal)
1982 — 2
1981 — 3
1980 — 134

Higher incoming quality material to us ensures higher outgoing quality products for you.

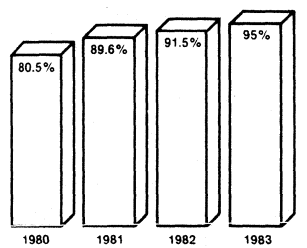
Quality and Reliability Organization

Quality and reliability specialists at the product-line level are involved in all aspects of the product, from design through every step in the manufacturing process, and provide product assurance testing of outgoing product. A separate corporate-level group provides direction and common facilities.

Quality and Reliability Functions

- Manufacturing quality control
- Product assurance testing
- Laboratory facilities — failure analysis, chemical, metallurgy, thin film, oxides
- Environmental stress testing
- Quality and reliability engineering
- Customer liaison

Lot Acceptance Rate from Signetics' Vendors



Communicating with Each Other

For information on Signetics' quality programs or for any question concerning product quality, the field representative in your area will provide you with the quickest access to answers. Or, write on your letterhead directly to the Corporate Director of Quality at the corporate address shown at the back of this data manual.

We are dedicated to preventing defects. When product problems do occur, we want to know about them so we can eliminate their causes. We are committed to zero defects. Here are some ways we can help each other:

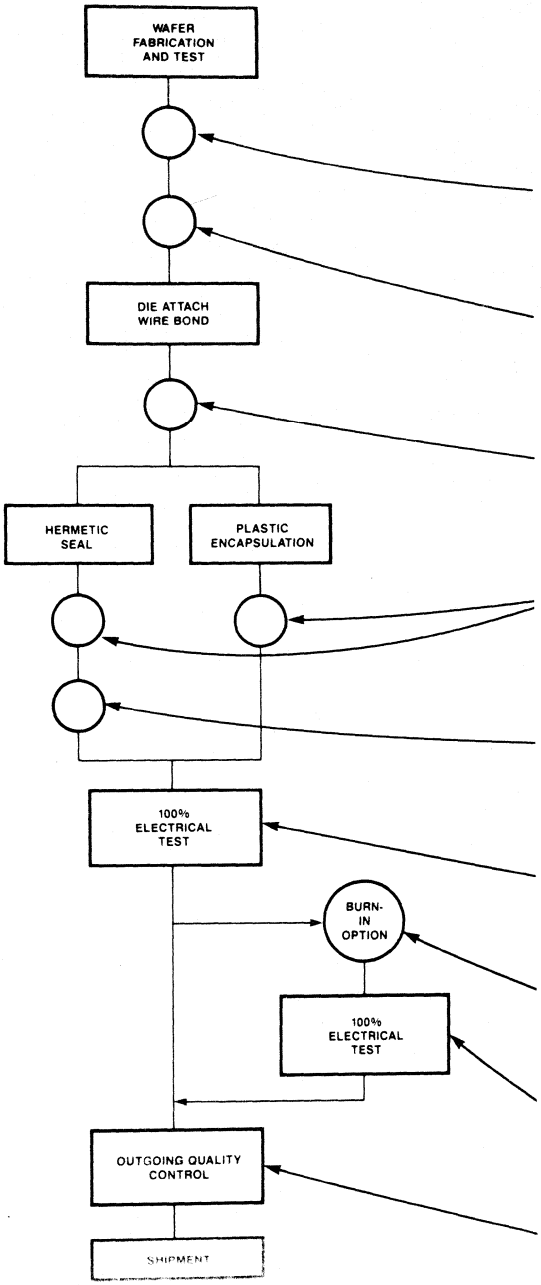
- Provide us with one informed contact within your organization. This will establish continuity and build confidence levels.
- Periodic face-to-face exchanges of data and quality improvement ideas between your engineers and ours can help prevent problems before they occur.
- Test correlation data is very useful. Line-pull information and field failure reports also help us improve product performance.
- Provide us with as much specific data on the problem as soon as possible to speed analysis and enable us to take corrective action.
- An advance sample of the devices in question can start us on the problem resolution before physical return of shipment.

This teamwork with you will allow us to achieve our mutual goal of improved product quality.

QUALITY AND RELIABILITY

Process Flows

This diagram shows the process flow for all Signetics Logic integrated circuits. This includes TTL, Schottky, Low Power Schottky, Interface and FAST.



Scanning Electron Microscope Control (SEM)

Wafers are sampled daily by the Quality Control Laboratory from each fabrication area and subjected to SEM analysis. This process control reveals manufacturing defects such as contact and oxide step coverage in the metalization process which may result in early failures.

Die Sort Visual Acceptance

Product is inspected for defects caused during fabrication, wafer testing, or the mechanical scribe and break operation. Defects such as scratches, smears and glassivated bonding pads are included in the lot acceptance criteria.

Pre-Seal Visual Acceptance

Product is inspected to detect any damage incurred at the die attach and wire bonding stations. Defects such as scratches, contamination and smeared ball bonds are included in the lot acceptance criteria.

Symbolization

Devices are marked with the device number and date code using laser marking equipment. This prevents part number mixing during later processing steps.

Seal Tests

Package seal integrity is ensured by 100% fine and gross leak testing.

100% Production Electrical Testing

Every device is tested for functional and DC parameters at 25°C guard banded to assure performance over temperature. Selected product lines receive 100% AC testing. Product assurance sampling is performed at room, hot and cold temperatures and includes AC/DC and functionality.

Burn-In (Level B Option)

Devices are burned in for 21 hours, T_j = 175°C maximum.

100% Production Electrical Testing

Every device is tested for functional and DC parameters at 70°C. Selected product lines receive 100% AC testing. Product assurance sampling is performed at room, hot and cold temperatures and includes AC/DC functionality.

QA Guarantees

A final QA inspection step guarantees the mechanical and electrical quality. Every shipment is sealed and identified by QA personnel.

NOTES

Section 3
Circuit Characteristics

CIRCUIT CHARACTERISTICS

INPUT STRUCTURES

There are six types of input structures that are commonly employed in TTL families: diffusion diode, Schottky diode, multiple emiter, diode cluster, PNP, and NPN.

The diffusion diode input is most often used with FAST circuits. The input diode is labeled as D1 in Figure 1. There can be more than one of them if NAND logic is to be performed. In the oxide-isolated processes these are base-collector diffusions. Each input pad also has a Schottky clamp diode D2. This diode is standard for most TTL circuits, and is included to limit negative input voltage excursions that are generally the result of inductive undershoot.

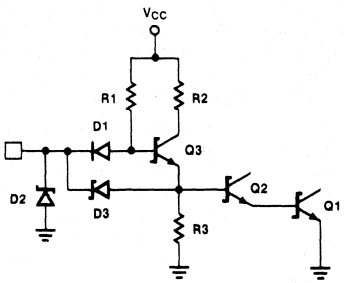


Figure 1. Diode Input

The static diode input function of voltage versus current is shown in Figure 2. If the pad voltage is negative, most of the relatively high, negative current flows through the clamp Schottky D2. At zero volts the current flows from V_{CC} through R1 and D1 to the pad. Switching from a logic LOW level to a logic HIGH level occurs when the input pad voltage rises high enough to force the current from the D1 path to the Q3-Q2-Q1 path. This happens when the base voltage of transistor Q3 is at three base-emitter drops ($3V_{BE}$), and the pad is at $2V_{BE}$, which is the standard FAST threshold switching voltage. At this voltage the input current is very small, just the leakage currents of diodes D1, D3 and clamp diode D2. The current remains at this small, positive value until breakdown voltage is reached.

Transistor Q3 and resistor R2 provide a current gain by increasing the amount of current available to Q2 and Q1 when the pad voltage is high. R3 bleeds current off the base of Q2 to pull it low when the pad voltage is low. D3 speeds up this process during the HIGH-to-LOW pad transition. When the switching transients are over, D3 is reverse biased.

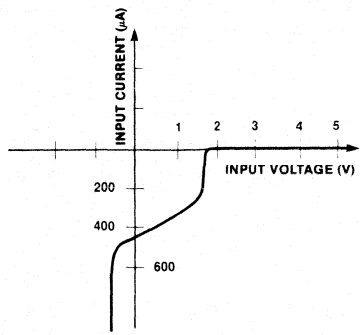


Figure 2. Static Diode Input Function of Voltage vs Current

The current of Figure 2 is scaled for the case where the pad is required to pull down a single 10K-ohm resistor R1 (20μA maximum in the HIGH state and 0.6mA maximum in the LOW state), which is defined as a standard FAST Unit Load (UL). For some parts, pad current can exceed a UL, especially in the logic LOW state. This will happen if the pad must sink the current from more than one R1 resistor or if the value of R1 is less than 10K ohms, which will be the case if the capacitance at the base of the transistor Q3 is too large for the required switching speed. In this event, the actual number of ULs is listed for each input in the specification sheet for the part. Note that a UL as defined here is less than the normally defined Schottky TTL Unit Load; the correlation is one Schottky Unit Load = 1.67 ULs. This is an important point to remember for fan-in and fan-out calculations in systems that mix FAST with other TTL families.

The Schottky diode input is shown in Figure 3. Its function is much the same as the diffusion diode input, except that the switching threshold voltage is lower by the Schottky diode forward drop, about 500mV. Because a higher threshold voltage is usually advantageous from a noise-margin standpoint in high-speed systems, the Schottky diode input is not used with FAST.

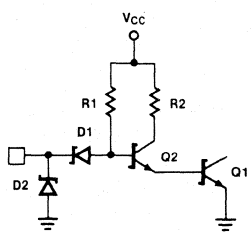


Figure 3. Schottky Diode Input

The multiple-emitter input is shown in Figure 4. Its function is also much the same as the diffusion diode input, but with the base-emitter junction used instead of the base-collector junction. In some respects this would be a better choice for high-speed logic, but it has one serious disadvantage which is the emitter-base breakdown voltage that may be as low as 5 volts. This low breakdown allows a high input current to flow through the Q2-Q1 base-emitter path which cannot be limited to an acceptable value with a series resistor.

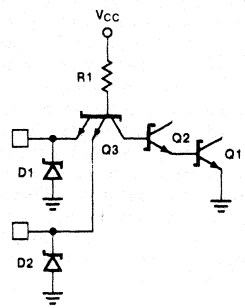


Figure 4. Multiple-Emitter Input

The diode cluster input (Figure 5) looks like a multiple-emitter input, except that its breakdown voltage is higher because separate Schottky junctions are used instead of a transistor. It has limited use in FAST circuits.

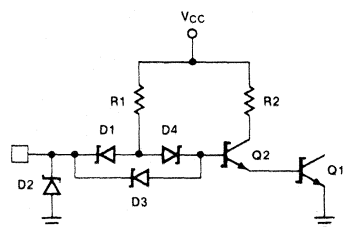


Figure 5. Diode Cluster Input

The PNP input in various forms has found wide acceptance in low power Schottky logic because it provides a desirable high-impedance input. Unfortunately, it is not well-suited for FAST circuits using the presently available processes because of problems associated with the vertical PNP device. A typical TTL usage is shown in Figure 6.

CIRCUIT CHARACTERISTICS

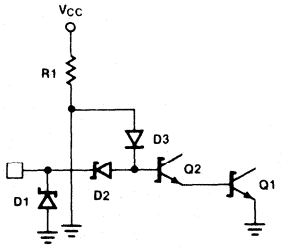


Figure 6. PNP Input

The NPN input is shown with two variations in Figures 7a and 7b. It has limited use in standard TTL circuits, and is used in selected FAST devices, especially where its superior high-impedance input characteristics are useful. A typical plot of static input current versus input voltage is shown in Figure 8. There are some significant differences between this function and that of the diffusion diode input shown in Figure 2, the most important being the much lower input current in the region from zero volts to threshold, and the controlled increase of input current above V_{CC}.

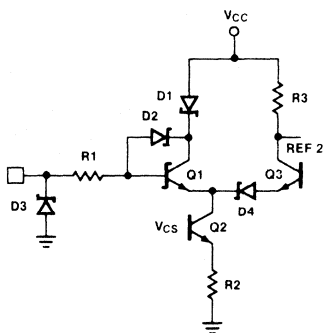


Figure 7a. NPN Input

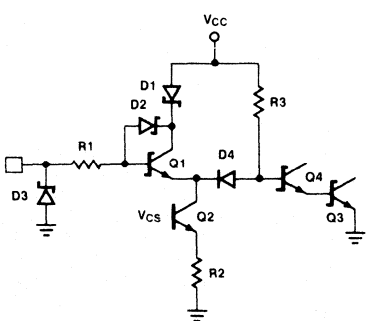


Figure 7b. NPN Input

When the pad voltage is negative, the large negative clamp current is supplied through the clamp Schottky diode D3. For positive voltages, from zero volts to the switching threshold of $2V_{BE}$, Q1 is off, and the input current I_{IL} is very small, just the leakage current of Q1, D2, and D3 with low reverse bias. As the input voltage rises above $2V_{BE}$, Q1 turns on and the current that had been flowing through D4 now flows through Q1, and blocking Schottky diode D1 to V_{CC}. The value of this current is determined by the current source transistor Q2 with its base connected to voltage reference V_{CS}, and by the size of the emitter resistor R2. The current is nearly constant within the normal operating range of input voltages, and has a typical value of 0.1mA to 1.0mA. The pad must supply only a small fraction of this bias current, the ratio of Q1 collector current to base current being the bipolar BETA factor. Typically, I_{IH} base input current is less than 20μA in the voltage range from zero volts to V_{CC}. This value is the specification for a standard FAST NPN Unit Load. As in the diode input case, if larger currents are needed to reduce delay times or to provide for multiple-input transistors connected to the same pad, the specification sheet for the particular device will identify the input pads which have NPN ULs larger than one, and will list their values.

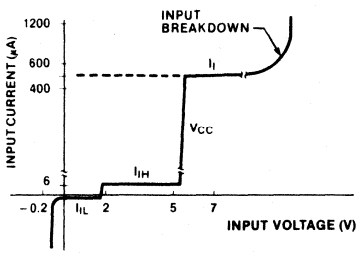


Figure 8. NPN Input Characteristics (not to scale)

In normal operation, the negative input voltage is limited by clamp Schottky D3 and the positive input voltage is less than V_{CC}. The actual input voltage may exceed V_{CC} for three reasons: there will be inductive overshoot in badly terminated systems; the V_{CC} pad may be floating or grounded; or the input pad may be forced high by electrostatic discharge or incoming inspection testing.

For the inductive overshoot case, when the pad voltage exceeds V_{CC}, part of the Q1 collector current begins to flow from the pad through limiting resistor R1 and Schottky diode D2. The current from V_{CC} through D1 decreases by exactly this amount, since Q2 is a constant current source. As the voltage continues to rise, D1 becomes reverse biased and prevents high currents flowing from the pad into V_{CC}. All the Q2 current flows into the pad through the R1-D2-Q1-Q2-R2 to ground. As stated before, this current is typically small, in the range of 0.1mA to 1.0mA, and nearly independent of pad voltage, as shown by the I_I plateau in Figure 8. It flows in the correct direction to provide a desirable positive overshoot clamp. This is an advantage over the diode input which does not clamp positive overshoots.

For the case where V_{CC} is grounded or floating, the input current is nearly zero for positive voltages between zero and approximately 7 volts. The conducting path through R1-D2-Q1 is available, but the current source Q2 will be shut off because, without V_{CC} drive, the Q2 base reference V_{CS} will be at zero volts.

For the incoming inspection testing case where V_{CC} and ground are connected, the response is shown in Figure 8. The current remains on the Q2-limited plateau until the pad voltage is high enough to cause non-destructive collector-emitter reach-through of Q2. At this point, input current increases as the pad voltage rises, and R1 functions to limit this current and prevent damage to Q2.

The electrostatic discharge case is similar to the incoming inspection case except that Q2 may be off if the V_{CC} pad is floating, in which case it breaks down at a slightly higher voltage. The NPN input produces reach-through at a relatively low voltage compared with the diode input. The effect of this non-destructive reach-through is to greatly increase the ability of the device to survive electrostatic discharge. The discharge current is passed through the chip at a relatively low power dissipation, and this is shared by elements R1, D2, Q1, Q2 and R2, so that none of them dissipate enough power to do damage. By way of contrast, with a diode input, the clamp Schottky diode breaks down at high voltage with high dissipation in a localized area, and may suffer damage.

Another advantage of the NPN input is its ability to interface on the chip to either a conventional TTL interior design, or to the less widely-used current-mode logic. The conventional TTL interface is shown in Figure 7b. In this case the Q2 current source is designed to provide sufficient current to insure that in the LOW state, with current flowing through the R3-D4-Q2 path, the base-emitter stack of Q3-Q4 is shut off.

CIRCUIT CHARACTERISTICS

The $2V_{BE}$ input threshold is set by the forward drops of Q1, D4, Q4 and Q3. The current-mode logic interface is shown in Figure 7a. The output voltage is the drop across R3, and is referenced to V_{CC} (or some on-chip regulated voltage lower than V_{CC}) as is required for current-mode logic. For this case, voltage reference REF2 is normally fixed at $2V_{BE}+1$ Schottky drop to provide a pad threshold voltage of $2V_{BE}$. In fact, REF2 can be tailored to set the switching threshold voltage to any desirable level; it can be set to something other than an integral number of base emitter drops, or it can be designed to reduce the sometimes undesirable temperature variations of input threshold.

One point worth observing is the tendency of an unconnected NPN input to float LOW, while diode input structures usually float HIGH. Generally, floating inputs should be avoided. Unused inputs should be tied to V_{CC} or ground to increase noise immunity and reduce electrostatic problems.

Of course, one of the most important features of the NPN input structures used on selected parts is the fact that they require less than 20μ A of input current in either logic state to drive them. This is a load current 30 times lower than is required by diode-type input structures in the logic LOW state, and makes it possible to eliminate the buffer/drivers that are often required to drive TTL loads from a MOS output, and thus reduce part count in certain applications.

OUTPUT STAGES

The purpose of the output stage is to supply current to a load to force it to a HIGH state or to sink current from the load to force it to a LOW state. The speed at which the load can be switched from one state to the other depends on how much supply of sink current is available from the output driver. There must be an amount in excess of that which is required to maintain the static load voltage, and it is the excess current that is available to charge or discharge the load capacitance. Most FAST circuits are designed to fit into one of two categories, based on output drive capability; the normal output stage, and the buffer driver which can supply approximately twice as much current.

Both normal drivers and buffers may be 3-state, which means that, in addition to LOW and HIGH states, they can be forced to a high-impedance OFF state as a third possible choice. This allows multiple components to be connected to a bus simultaneously, with only the single-selected device providing actual drive capability.

Every output stage has the basic components shown in Figure A.

The pull-down driver components sink load currents to force a LOW state at the output pad; the pull-up driver components supply current to force a HIGH state. The control components turn on the selected driver and turn off the non-selected driver in response to the logic input signal. For 3-state parts, the control components turn off both drivers if the 3-state control signal is active. The output Schottky clamp is included to suppress inductive undershoots, and is a part of every FAST circuit. The load requires a static current to keep it in either a logic HIGH or LOW state. The drivers must also charge and discharge the load capacitance C_L, which is generally one of the major factors that influence switching speed.

Since, to a large extent, they function independently of each other, the pull-up driver, pull-down driver, and control blocks are discussed independently.

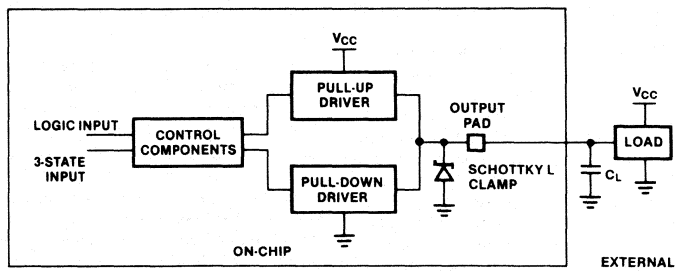


Figure A. Output Stage Basic Components

PULL-UP DRIVERS

Open Collector

The simplest pull-up driver consists of no more than a fixed pull-up resistor tied to V_{CC}. For this case, the control stage interacts only with the pull-down driver. In the LOW state, this must sink the current from both the pull-up resistor and load. In the HIGH state, the pull-up resistor must supply all of the load current. Most often, the pull-up resistor is not physically part of the integrated circuit chip itself, but is added externally; in this case the only circuit element connected to the output pad (in addition to the ever-present Schottky clamp) is the collector of the pull-down driver transistor, hence the name "open collector." Parts with this output stage can be tied together for bus applications without the need to 3-state. If any of the various pull-down drivers are active, the bus is low; only if all of them are off can the external resistor pull the bus positive. The positive voltage limit in this case depends on the amount of current the various loads require; with conventional TTL, the output can go almost as high as V_{CC}; with FAST, the process will generally not sustain a large collector-to-emitter voltage, and the collector of the pull-down drivers will begin to leak at about 4.5V and clamp the output at a voltage less than V_{CC}.

One obvious advantage of open-collector parts is that their outputs can be tied together to obtain a "free" wired logic AND. The higher output voltage swing provides a larger positive noise margin, which may be an important consideration in some designs. Open-collector parts are significantly slower than standard outputs because they must switch through larger voltage excursions and because they have no active pull up. For this reason, they are not available in as many FAST functions as they are in other TTL families.

Standard Darlington

Most FAST pull-up drivers use dual transistors, connected as shown in Figure B1, with the emitter of the first device Q_b delivering current to the base of the driver Q_a. This configuration is called a Darlington circuit and provides a composite current gain nearly as large as the product of the current gains of Q_b and Q_a.

The major advantage of the Darlington pull up, as compared to the open collector, is that the pad is actively pulled high by the emitter-follower action of Q_a which is capable of supplying large currents to quickly charge the output capacitance. Despite the large output current that is available, the drive requirements of Q_b are low, so that the voltage drop across R_c is small, and the

CIRCUIT CHARACTERISTICS

pad will pull up to a voltage nearly as high as $V_{CC}-2V_{BE}$.

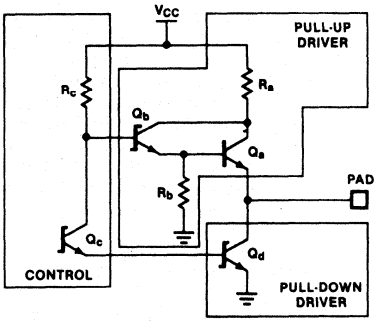


Figure B1. Basic Darlington Pull Up

For the case where the pad voltage is high, the phase-splitter transistor Q_c is off, and the base of Q_b is pulled high by resistor R_c. The current which flows through R_c is just sufficient to provide base drive to Q_b. The base voltage of Q_b will be just slightly below V_{CC}, and the output pad voltage will be less than this by the sum of the V_{BE} drops of Q_b and Q_a, both of which are on. Most of the base current for Q_a and the current through pull-down resistor R_b is supplied from V_{CC} through R_a and Q_b. Q_b has a Schottky clamp to prevent saturation when the current through R_a is large. Resistor R_a limits the amount of current flowing from V_{CC} through Q_a to a value small enough that Q_a will not be damaged if the output pad is accidentally grounded for a short period of time. In this, the current is called output short-circuit current (I_{OS}), and its maximum value is approximately the current available to charge the output capacitance at the beginning of a LOW-to-HIGH transition. The minimum current available when the pad has reached the minimum guaranteed high voltage V_{OH} is called output high current (I_{OH}), and is specified to be either 1mA or 3mA, depending on the type of driver. The maximum output voltage that the pull-up driver can achieve occurs at maximum V_{CC}, and at high temperature with corresponding low values of transistor V_{BES} and high current gain. Conversely, the minimum high voltage occurs at low V_{CC} and low temperature.

In the LOW state, the pull-down driver Q_d is on and the pad voltage is the Q_d saturation voltage V_{sat}. Q_c is on and its collector resistor R_c is pulled down to a $V_{BE}+V_{sat}$; the V_{BE} of Q_d, V_{sat} of Q_c. Q_b is also on, with its emitter at V_{sat}, and the current through R_b is low. The base-emitter voltage of Q_a is nearly zero and Q_a is off.

The rate at which the pull-up driver can force a LOW-to-HIGH transition depends on a number of factors. The first, and obvious, consideration is that the control components must turn off the pull-down driver very quickly. During the short time that both pull up and pull down are on, there is a large feed-through current spike that is wasted as far as switching the load is concerned; it also increases chip power dissipation and produces undesirable voltage spikes in V_{CC} and ground. Assuming the pull down is off, the LOW-to-HIGH transition speed is governed by: 1) the rate at which R_c can pull up the base of Q_b; 2) the amount of pad current required to drive the load and charge the load capacitance; 3) the value of R_a; 4) the physical size and current gain of Q_a; and 5) the amount of Q_a base drive current that is lost through R_b to ground. The amount of R_b drive current lost can be reduced by connecting R_b to the output pad instead of ground, and this is done in a number of FAST parts. For this case, the static current through R_b with the pad high is less than if R_b is grounded, but switching feed-through current spike for a HIGH-to-LOW transition may be increased because R_b cannot effectively pull down the base of Q_a until after the pad voltage falls.

The pad can be driven above its maximum high value by an external pull up or by positive reflections from a transmission line. When this happens, Q_a and Q_b do not have sufficient base-emitter drive to keep them on. If the pad voltage rises significantly above V_{CC}, Q_a will begin to leak current into V_{CC}. For the case where R_b is tied to the pad instead of ground, the reverse transistor action of Q_a allows a high pad to V_{CC} current. This is not usually a problem in normal operation, but should be avoided in system applications where the V_{CC} pad may be intentionally grounded.

3-State

For all 3-state FAST parts, the leakage paths to a grounded V_{CC} pin are blocked with Schottky diodes. A typical 3-state pull up is shown in Figure B2. S_a is the series Schottky blocking diode. 3-State Schottkys S_{t1} and S_{t2} serve to simultaneously turn off the pull-up and pull-down drivers. The 3-state control is active when it is pulled low to within V_{sat} of ground. In this state it sinks all the available drive current for Q_b and Q_c, and pulls their bases down to ($V_{sat}+V_{Schottky}$), which is essentially one V_{BE}. The voltage drop across R_c is large and 3-state power dissipation is typically high. Q_a and Q_b are off for normal TTL voltage ranges of the output pad; a negative undershoot large enough to drive the pad about one V_{BE} below ground will allow them to turn on and supply current from V_{CC}; this action aids the clamping Schottky diode in preventing the pad voltage from falling lower.

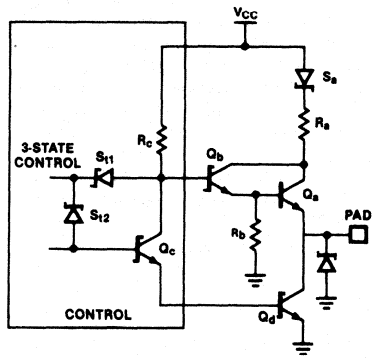


Figure B2. Basic 3-State Pull Up

PULL-DOWN DRIVERS

The basic FAST pull down is shown in Figure C. Q_d is the pull-down driver transistor, a big Schottky-clamped device capable of sinking large currents. C_d is the stray base-collector capacitance of Q_d and its unavoidable presence has an important effect on the performance of the pull-down driver. Q_c is the Schottky-clamped phase splitter. It functions as a current-limited, low-impedance driver for Q_d when the logic input voltage V_{IN} is high, and as an inverting driver for pull up Q_b by virtue of the current through R_c when V_{IN} is low and Q_c is off. Z_d is the pull-down impedance network which insures that Q_d is off when V_{IN} is low.

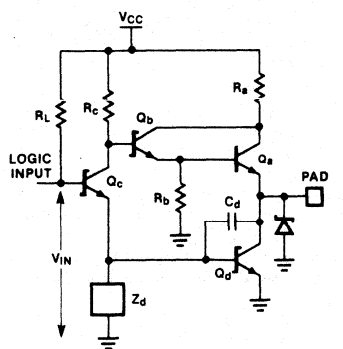


Figure C. Basic FAST Pull Down

CIRCUIT CHARACTERISTICS

Switching to the logic LOW state occurs when V_{IN} is larger than the V_{BE} drops of Q_c and Q_d, both of which are on. Part of the total emitter current available from Q_c comes from R_c, which has a voltage drop of $V_{CC}-V_{BE}-V_{sat}$. The remainder of the Q_c emitter current is supplied through its base Schottky clamp or by other components not shown in Figure C but discussed in the section on control components. A portion of the total Q_c emitter current is lost in the pull-down network Z_d; the remainder is available as base current for pull-down driver Q_d. The amount of current Q_d can sink depends on its base drive, its current gain, and its collector voltage. This current is specified on a per-part basis in the data sheets at output low voltage (V_{OL}) of 0.5V. The current which Q_d can sink in the switching range with the pad voltage at 2.5V is called available current (I_{AVL}), and is guaranteed to be at least 70mA for FAST. The manner in which this current varies as the pad voltage decreases from 2.5V to V_{OL} is not specified as a FAST family parameter, since it is critically-dependent on circuit design for a particular part, but is included as a specification for selected parts, especially those tailored to drive transmission lines. Several innovative circuit improvements that increase I_{AVL} by increasing the drive current for Q_d are shown in Figures D1 and D2. Speed-up Schottky diodes S_{s1} and S_{s2} have been added to the standard pull-down circuit as shown in Figure D1. Both are reverse-biased and off in the HIGH state, since R_c pulls the collector of Q_c nearly to V_{CC}. Both connect the collector of Q_c to nodes that need to be discharged during a HIGH-to-LOW transition, S_{s1} to the base of Q_a, S_{s2} to the pad. They will conduct if these node voltages are higher than $V_{BE}+V_{sat}+V_{Schottky}$, or approximately $2V_{BE}$; they are quite effective above 2V. Other networks are available which function down to lower voltages; these are especially useful for transmission line drivers. Figure D2 shows a dynamic kicker that gives an impulse of current which is especially useful in discharging high capacitive loads.

The network of elements labeled Z_d in Figure C is the pull-down impedance which insures that Q_d is off when the value of V_{IN} falls below $2V_{BE}$. When the voltage at the base of Q_d is being pulled high by Q_c or low by Z_d, the output pad voltage responds by moving in the opposite direction. This produces a change in voltage across C_d, which is the sum of the base voltage change and the collector voltage change, so the amount of charge required by C_d is magnified by a factor which is larger than unity. This well-known Miller-effect causes the apparent value of C_d, as perceived by the drivers, to be a factor of about five times larger than the already large physical junction capacitance, all of which means that the drivers Q_c and Z_d need to supply or sink much more current during an output transition than is necessary to maintain static conditions. When static conditions do exist internally in the circuit, noise voltage spikes on the output pad, V_{CC}, or ground can momentarily force the base of Q_d in the direction to produce a serious output glitch, and the drivers must respond quickly to counter this coupled noise.

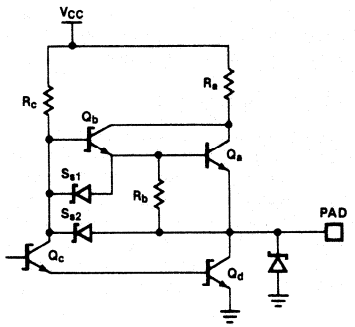


Figure D1

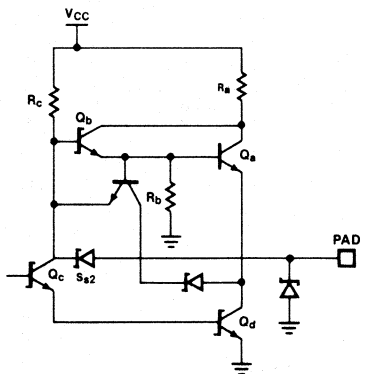


Figure D2

The simplest Z_d element is a resistor R_{Z1} tied to ground, as shown in Figure E1. It will pull the base of Q_d all the way down to zero volts if V_{IN} is less than one V_{BE}. This provides good immunity to coupled noise, but slows down the HIGH-to-LOW pad transition somewhat because the base of Q_d must rise a full V_{BE} before the output can begin to change. The value of R_{Z1} needs to be relatively large to prevent a serious loss of base drive current when Q_d is on, which makes it easier to capacitively couple voltage spikes to the base of Q_d and, in part, nullifies the good noise immunity the full V_{BE} swing provides.

The addition of a series Schottky diode solves most of the problems. This is shown in Figure E2. The Q_d base voltage cannot pull below a Schottky drop, so the switching speed is unimpaired. The value of R_{Z2} can be less than R_{Z1} for the same current when the base is high, so the effect of coupled charge is less and the noise margin is acceptable.

The circuit of Figure E3 is standard with many TTL families. It pulls the base of Q_d down even less than does $R_{Z2}-S_{d2}$, but it has a relatively high dynamic impedance and is somewhat noise sensitive. It has the advantage that it tends to "square up" the input voltage-to-output voltage transfer function, hence its popular name "squaring circuit." It is frequently used in simple gates where the shape of the transfer function may be important. For more complicated circuits, where there are one or more stages of logic with gain between input and output pads, the squaring ability is pretty much lost; in fact, it is likely that high-gain, multiple-logic-level FAST circuits will oscillate if the input voltage is held exactly at threshold for any length of time.

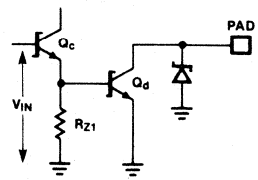


Figure E1

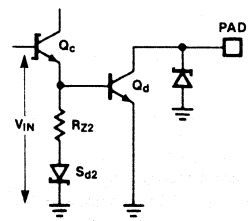


Figure E2

CIRCUIT CHARACTERISTICS

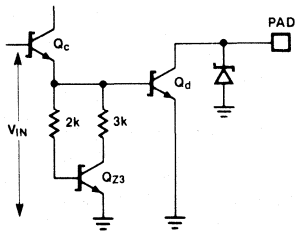


Figure E3

Figure E4 shows a popular dynamic circuit that is used in conjunction with a resistor or squaring circuit pull down, and which insures that C_d cannot couple enough charge to the base of Q_d to slow down a LOW-to-HIGH transition. In operation, as the emitter of Q_d rises, charge is coupled through C_{Z4} into the base of Q_{Z4} which turns on and shunts the Miller current flowing through C_d to ground. When the transition is finished, the current through C_{Z4} stops and Q_{Z4} turns off. When the HIGH-to-LOW transition of Q_b occurs, C_{Z4} discharges through S_{d4}. Because Q_{Z4} reduces the problem associated with Miller current, the circuit is called a "Miller Killer."

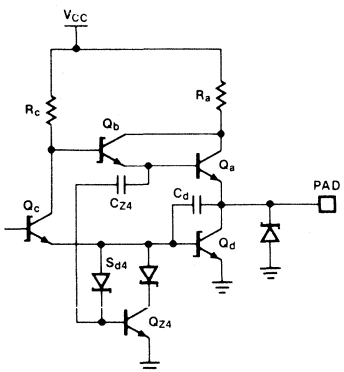


Figure E4

Figure E5 shows an active pull down for the base of Q_d. The drive for Q_{Z5} (not shown) must be generated from the same signal that drives the base of Q_c. When Q_c is on, Q_{Z5} must be off and when Q_c is off, Q_{Z5} turns on to hold the base of Q_d low. The impedance is very low, eliminating the capacitive-coupling noise problem.

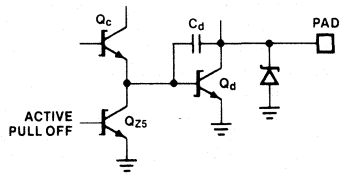


Figure E5

NOISE MARGIN AND CONTROL COMPONENTS

This section covers the following topics: 3-state control drivers and special 3-state problems; V_{CC} turn-on current and 3-state glitches during power-up; and noise margin and ground voltage as relates to inputs.

3-State Control Drivers

The normal TTL 3-state scheme is shown in Figure B2. The 3-state control voltage in the OFF state is high enough that S_{t1} and S_{t2} are reverse-biased; in the active state the control voltage is low, usually V_{sat}, so that the Q_a-Q_b base emitter stack is off, as is the Q_c-Q_d stack. In the 3-state mode, R_c is dissipating maximum power. Blocking Schottky diode S_a prevents current from flowing backwards through Q_a if the V_{CC} pad is grounded, and the output pad high voltage can be about 4.5V before there is any significant 3-state leakage current. The only exception to this general rule with FAST is for the diode input transceiver function, where the same pad acts as an input or an output. In this case, the pad supplies one or more normal FAST unit loads of current if it is LOW, and tends to pull to $2V_{BE}$ if it is floating. NPN input transceivers have normal low 3-state leakage.

There are several innovative improvements to the basic 3-state circuit, as shown in Figure F. The addition of inverter Q_{c2}-R_{c2} with a blocking Schottky S_{c2} allows the addition of feedback diodes S_{s1} and S_{s2} to increase I_{AVL}; S_{c2} cannot be included in series with R_{c1} because its forward voltage drop would lower V_{OH}. An added benefit is that 3-state power is not increased, since only one R_{c1} needs to be pulled low. The current through Q_{c2} is available as added base drive to Q_d, so nothing is wasted. An additional transistor may be paralleled with Q_{c1} and Q_{c2} to control an active pull-down version of impedance Z_d which, discussed in a previous section, eliminates the Miller turn-on problem of Q_d.

Turn-On Current and 3-State Glitches

There is no formal family specification that limits the amount of V_{CC} current a FAST circuit may draw during turn-on as V_{CC} rises from zero to 4.5V. However, for most new designs, and especially for circuits that have high I_{CC} requirements, an effort has been made to limit maximum turn-on I_{CC} to 110% of I_{CC} max. This precaution prevents an undesirable system situation where the V_{CC} power supply is large enough to drive the devices, but can't power them up. The major component of turn-on current is V_{CC} to ground feed-through of output stages. Unless specific steps are taken to prevent it, the pull-up Darlington turns on if V_{CC} is

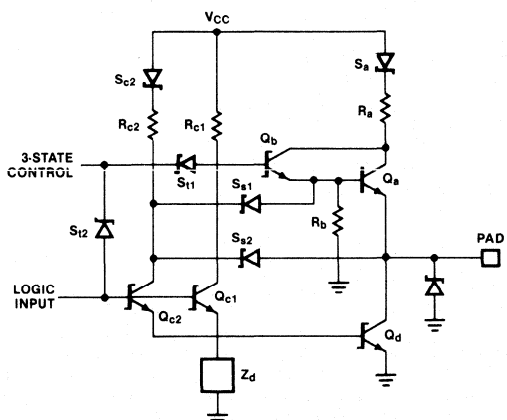


Figure F. Improved 3-State Circuit

CIRCUIT CHARACTERISTICS

greater than $2V_{BE}$, and remains on until the on-chip voltage is high enough to set the phase splitter solidly in one or the other of its two states. The solution is to incorporate extra circuit components that will set the phase splitter at voltages nearly as low as $2V_{BE}$, or turn off the top device with a separate 3-state-type structure which activates at low V_{CC} voltages and becomes inoperative when V_{CC} is high.

The amount of current that can be fed from an output pad back into a grounded V_{CC} pad, or through the chip to ground for an open V_{CC} pad, depends on the design. Generally, 3-state feedback current is specifically limited to low values which are leakage or breakdown related. Other parts have medium to high current. Those with Darlington pull-downs connected to the output pad conduct the most.

Some 3-state parts, especially selected buffer functions, have additional circuit elements to insure that as they power on they source or sink no appreciable output current, provided that the 3-state control pads are in the active state as V_{CC} rises. This means that V_{CC} can be turned on or off at will in the system to conserve power, and bus voltages will not be affected. Parts with this capability are identified in the specific data sheets.

Noise Margin and Ground Voltage

One current-related noise problem that can influence system operation is described with reference to Figure G which shows an equivalent input and output stage. The main consideration is the problem of ground voltage as it affects input noise margin. The equivalent input circuit is represented by R_{IN} and the four diodes D_1–D_4. These components establish a switching threshold voltage of $2V_{BE}$ relative to chip ground. The on-chip voltage V_{IN} must exceed this value by a margin large enough to guarantee a static HIGH logic level with sufficient overdrive to insure switching speed. The actual on-chip voltage V_{IN} is the voltage applied between the input pad and ground pad less the voltage drop of the ground impedances R_g and L_g. This ground voltage is the sum of the steady-state voltage due to ground current flowing through R_g, and the inductive voltage drop across L_g, which is proportional to the rate at which the ground current is changing. The inductive drop is usually the larger of the two, and usually has a maximum positive value at the beginning of a HIGH-to-LOW transition of an output. The total ground current is the sum of the contributions from all the output stages on a chip, and

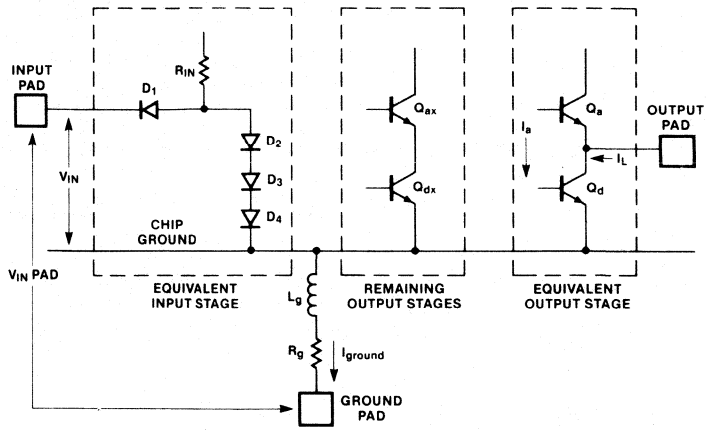


Figure G. Equivalent Input and Output Stages

the total ground voltage for a multiple-output product can be much higher than that caused by switching a single output.

Excessive ground noise voltage in a system is likely to result, at the very least, in serious degradation of switching speed, and may produce glitches on outputs or cause system relaxation oscillations. The problem is not unique with FAST, but is greatly aggravated by the fast edge rates and large currents that FAST is designed to produce. Because of this, it is not always possible to replace other TTL families directly with equivalent FAST products. The major design considerations are the ground inductance between a stage and its driver; the efficiency of V_{CC} bypassing, especially at low V_{CC}; the total amount of load current the chip must switch at any one time, including the simultaneous contributions of multiple outputs; the size and timing of inductive output ringing or reflections from transmission lines; and the amount of feed-through current during switching of an output stage. The system designer has control of all of these factors except the last, which is determined by those circuit elements labeled as control components in Figure A.

The primary function of the control components is to force the state of the output pull-up and pull-down drivers. These must be driven differentially because the pull-up stage is a non-inverting emitter follower, and the pull-down is an inverting grounded emitter. During a switching transient it is possible for both drivers to be on simultaneously, and large V_{CC}-to-ground current spikes are the result. One important function of the differential driver is to minimize the feed-through current. This can be accomplished in one of two ways: either turn one stage off before the other is switched on, or, more commonly, drive them together, but very fast so the feed-through current can flow for only a very short time. Both procedures are used with multiple variations in FAST circuits. The actual circuit design depends on how much of a problem feed-through current is for a particular logic function.

The simplest driver is the so-called phase splitter, which consists of R_c, Q_c and Z_d, as shown in Figure C. R_c provides the drive to the pull-up stage when Q_c is off, and Q_c emitter drives the output pull-down when Q_d is on. The ON condition requires a voltage V_{IN} high enough to provide current to the $2V_{BE}$ base emitter stack of Q_c and Q_d. The OFF condition requires that V_{IN} be less than $2V_{BE}$. The actual V_{IN} low voltage is a compromise between insuring that Q_c is off with a comfortable noise margin, and the increased delay in turning Q_c on if its base is pulled lower than necessary. If the base is not pulled down sufficiently low, a system-related noise problem can occur, as illustrated in Figure H.

The scenario is that Q_d is presently on with the pad low at a V_{sat}. Th output is on the verge of a LOW-to-HIGH transition with V_{IN} falling and Q_c ready to turn off. A problem occurs if, at the instant before the pull-up device turns on to force the output positive, the voltage from output pad to chip ground falls. This can happen if inductive ringing or transmission line undershoot occurs at the right moment to pull the pad down, or if ground current from additional on-chip complementary drivers flowing through Z_g

CIRCUIT CHARACTERISTICS

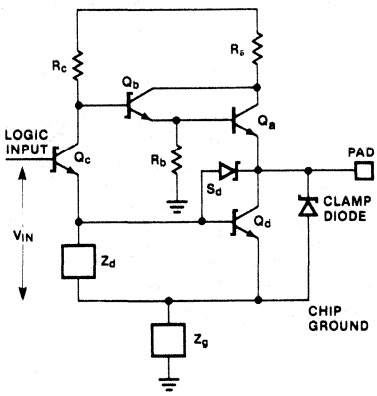


Figure H

forces the chip ground positive with respect to the pad ground. The low pad voltage pulls down the emitter of Q_c through the Schottky clamp diode S_d, and if V_{IN} is not sufficiently low, Q_c cannot turn off. The net result is that R_c cannot rise, hence the LOW-to-HIGH transition is delayed until the voltage from output pad to chip ground can rise. The preventative actions are to reduce ground impedance, limit load currents on parts that have on-chip complementary outputs, and reduce undershoot by using good PC layout practices. Products that are particularly susceptible because of a higher than usual voltage for the LOW-state value of V_{IN} are identified on the individual data sheets.

To reiterate, control of ground and V_{CC} noise is imperative if one is to realize the full speed advantages of FAST. The most vital consideration is the reduction of ground lead inductance to the lowest possible value by using ground planes and wide ground traces on PC boards; adequate low-inductance V_{CC} bypassing is also necessary. Total load switching current for sensitive circuits must not exceed a value which overdrives actual ground or V_{CC} impedance. Special pinouts with side-bonded V_{CC} and ground pins are available on some part types. Low-impedance, short-lead surface-mounted packages may be used where fast, high-current switching is vital.

Section 4
FAST User's Guide

DATA SHEET SPECIFICATION GUIDE

INTRODUCTION

Signetics' FAST data sheets have been configured for quick usability.

They are self-contained and should require minimum reference to other sections for amplifying information.

TYPICAL PROPAGATION DELAY AND SUPPLY CURRENT

The typical propagation delays listed at the top of the data sheets are the average between t_{PLH} and t_{PHL} for the most significant data path through the part.

In the case of clocked products, this is sometimes the maximum frequency of operation. In any event, this number is under the operating conditions of $V_{CC} = 5.0V$ and $T_A = 25°C$.

The typical I_{CC} current shown in that same specification block is the average current (in the case of gate, this will be the average of the I_{CCH} and I_{CCL} currents) at $V_{CC} = 5.0V$ and $T_A = 25°C$. It represents the total current through the package, not the current through the individual functions.

LOGIC SYMBOLS

There are two types of logic symbols. The conventional one, "Logic Symbol," explicitly shows the internal logic (except for complex logic). The other is "Logic Symbol (IEEE/IEC)" as developed by the IEC and IEEE. The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without explicitly showing the internal logic. Internationally, Working Group 2 of IEC Technical Committee TC-3 is preparing a new document (Publication 617-12) that will consolidate the original work started in the mid-1960's and published in 1972 (Publication 117-15), and the amendments and supplements that have followed. Similarly, for the U.S.A., IEC Committee SCC 11.9 is revising the publication IEEE Std 91/ANSI Y32.14.

The up-to-date version of the IEEE/IEC logic symbols prepared by the IEEE and IEC can be purchased from either:

Institute of Electrical and
Electronic Engineers/NC
345 East 47th Street
New York, NY 10017

or

American National Standards
Institute, Inc.
1430 Broadway
New York, NY 10018

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table carries the maximum limits to which the part can be subjected without damaging it . . . there is no implication that the part will function at these extreme conditions. Thus, specifications such as the most negative voltage that may be applied to the outputs only guarantees that if less than −0.5V is applied to the output pin, after that voltage is removed, the part will still be functional and its useful life will not have been shortened.

Input and output voltage specifications in this table reflect the device breakdown voltages in the positive direction (+7.0V) and the effect of the clamping diodes in the negative direction (−0.5V).

Absolute maximum ratings imply that any transient voltages, currents, and temperatures will not exceed the maximum ratings. Typical absolute maximum ratings are shown in Table 1.

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table has a dual purpose. In one sense, it sets some environmental conditions (operating free-air temperature), and in another, it sets the conditions under which the limits set forth in the DC Electrical Characteristics table and AC Electrical Characteristics table will be met. Another way of looking at this table is to think of it not as a set of limits guaranteed by Signetics, but as the conditions Signetics uses to test the parts and guarantee that they will then meet the limits set forth in the DC and AC Electrical Characteritics tables.

Some care must be used in interpreting the numbers in these tables. Signetics feels strongly that the specifications set forth in a data sheet should reflect as accurately as possible the operation of the part in an actual system. In particular, the input threshold values of V_{IH} and V_{IL} can be tested by the user with parametric test equipment . . . if V_{IH} and V_{IL} are applied to the inputs, the outputs will be at the voltages guaranteed by the DC Electrical Characteristics table. There is a tendency on the part of some users to use V_{IH} and V_{IL} as conditions applied to the inputs to test the part for functionality in a "truth-table exerciser" mode. This frequently causes problems because of the noise present at the test head of automated test equipment. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, on the order of milliseconds, and any noise present at the inputs has settled out before the outputs are measured. But in functionality testing, the outputs are examined much faster, before the noise on the inputs has settled out and the part has assumed its final and correct output state. Thus, V_{IH} and V_{IL} should never be used in testing the functionality of any FAST part type. For these types of tests, input voltages of +4.5V and 0.0V should be used for the HIGH and LOW states, respectively.

Table 1. Absolute Maximum Ratings

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	48	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

In no way does this imply that the devices are noise sensitive in the final system. The use of "hard" HIGHs and LOWs during functional testing is done primarily to reduce the effects of the large amounts of noise typically present at the test heads of automated test equipment with cables that may at times reach several feet. The situation in a system on a PC board is less severe than in a noisy production environment. Typical recommended operating conditions are shown in Table 2.

by sinking the energy to ground or to V_{CC}, depending on the state. The ability of the output to do that is determined by its output impedance. The lower half of the output stage is a very low-impedance transistor which can effectively pull the noise source down. Because of the higher impedance of the upper stage of the output, it is not as effective in shunting the noise energy to V_{CC}, so that an extra 0.4V of noise immunity in the HIGH state compensates for the

Over a period of time, I_{OS} became a measure of the ability of an output to charge line capacitance. Assume a device is driving a long line and is in the LOW state. When the output is switched HIGH, the rise time of the output waveform is limited by the rate at which the line capacitance can be charged to its new state of V_{OH}. At the instant the output switches, the line capacitance looks like a short to ground. I_{OS} is the current demanded by the capacitive load as the voltage begins to rise and the

Table 2. Recommended Operating Conditions (FAST Family)

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				-3	mA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	– 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS

This table reflects the DC limits used by Signetics during their testing operations conducted under the conditions set forth in the Recommended Operating Conditions table. V_{OH}, for example, is guaranteed to be no less than 2.7V when tested with V_{CC} = + 4.75V, V_{IH} = 0.8V across the temperature range of 0°C to + 70°C, and with an output current of I_{OH} = – 1.0mA. In this table, one sees the heritage of the original junction-isolated Schottky family . . . V_{OL} = 0.5V at I_{OL} = 20mA. This gives the user a guaranteed worst-case LOW-state noise immunity of 0.3V. In the HIGH state the noise immunity is 0.7V worst case. Although at first glance it would seem one-sided to have greater noise immunity in the HIGH state than in the LOW, this is a useful state of affairs. Because the impedance of an output in the HIGH state is generally much higher than in the LOW state, more noise immunity in the HIGH state is needed. This is because the noise source couples noise onto the output connection of the device — that output tries to pull the noise source down higher impedance. The result is a nice balance of sink and drive current capabilities with the optimum amount of noise immunity in both states.

I_I, the maximum input current at maximum input voltage, is a measure of the input leakage current at the guaranteed minimum input breakdown voltage of 7.0V. Although some users consider this to be a test of the input breakdown itself, that voltage is typically over 15V. At room temperature, this leakage current should be less than 10μA.

Short-circuit output current is a parameter that has appeared on digital data sheets since the inception of integrated circuit logic devices, but the meaning and implications of that specification have totally changed. Originally, I_{OS} was an attempt to reassure the user that if a stray oscilloscope probe accidentally shorted an output to ground, the device would not be damaged. In this manner, an extremely long time was associated with the I_{OS} test. However, thermally-induced malfunctions could occur after several seconds of sustained test.

demand decreases. We now reach the critical point in our discussion. The full value of I_{OS} need only be supplied for a few hundred microseconds at most, even with 1.0μFd of line capacitance tied to the output, a load that is unrealistically high by several orders of magnitude.

The effect of a large I_{OS} surge through the relatively small transistors that make up the upper part of the output stage is not serious — AS LONG AS THAT CURRENT IS LIMITED TO A SHORT DURATION. If the hard short is allowed to remain, the full I_{OS} current will flow through that output state and may cause functional failure or damage to the structure. A test-induced failure may occur if the I_{OS} test time is excessive. As long as the I_{OS} condition is very brief, typically 50ms or less with ATE equipment, the local heating does not reach the point where damage or functional failures might occur. As we have already seen, this is considerably longer than the time of the effective current surge that must be supplied by the device in the case of charging line capacitance. The Signetics' data sheet limits for I_{OS} reflect the conditions that the part will

see in the system — full I_{OS} spikes for extremely short periods of time. Problems could occur if slow test equipment or test methods ground and output for too long a time, causing functional failure or damage. DC electrical characteristics are shown in Table 3.

AC ELECTRICAL CHARACTERISTICS

The AC Electrical Characteristics table contains the guaranteed limits when tested under the conditions set forth in the AC Test Circuits and Waveforms section. In some cases, the test conditions are further defined by the AC setup requirements (see Table 5) — this is generally the case with counters and flip-flops where setup and hold times are involved.

All of the AC characteristics are guaranteed with 50pF load capacitance. The reason for choosing 50pF over 15pF as load capacitance is that it allows more leeway in dealing with stray capacitance, and also loads the device during rising or falling output transitions, which more closely resembles the loading to be expected in average applications, thus giving the designer more useful delay figures.

Although the 50pF load capacitance will increase the propagation delay by an average of about 1ns for FAST devices, it will increase several ns for standard Schottky devices.

The load resistor of 500Ω is conveniently specified as both pull-up and pull-down load resistor.

FAST products are being released in the surface-mounted SO package as a commercial option. Because of the reduced inductance inherent in this package, minimum propagation delays are being derated by 0.2ns. This is reflected by a note at the bottom of Table 4.

Table 3. DC Electrical Characteristics (FAST™ Family)

SYMBOL	PARAMETER		LIMITS[2] Min	LIMITS[2] Typ[3]	LIMITS[2] Max	UNIT	V_{CC}[4]	CONDITIONS[2]
V_{IH}	Input HIGH voltage		2.0			V		Recognized as a HIGH signal over recommended V_{CC} and T_A range
V_{IL}	Input LOW voltage				0.8	V		Recognized as a LOW signal over recommended V_{CC} and T_A range
V_{IK}	Input clamp diode voltage				−1.2	V	Min	I_{IN} = −18mA
V_{OH}	Output HIGH voltage	Std[5] Mil	2.5	3.4		V	Min	I_{OH} = 20μA multiplied by output HIGH U.L. shown on data sheet
		Std[5] Com'l	2.7	3.4				
V_{OL}	Output LOW voltage			0.35	0.5	V	Min	I_{OL} = −0.6mA multiplied by output LOW U.L. shown on data sheet
I_{IH}	Input HIGH current	1.0 U.L.		1	20	μA	Max	I_{IH} = 20μA multiplied by input HIGH U.L. shown on data sheet; V_{IH} = 2.7V
		2.0 U.L.		2	40			
		n U.L.			n(40)			
I_I	Input HIGH current, breakdown test, all inputs			5	100	μA	Max	V_{IN} = 7.0V
	NPN inputs:[6] Input clamp current			500	1000			
I_{IL}	Input LOW current	1.0 U.L.		−0.4	−0.6	mA	Max	I_{IL} = −0.6mA multiplied by input LOW U.L. shown on data sheet; V_{IN} = 0.5V
		2.0 U.L.		−0.8	−1.2			
		n U.L.			n(−0.6)			
	NPN inputs	0.033 U.L.			−0.02			
I_{OZH}	3-State output OFF current HIGH			2	50	μA	Max	V_{OUT} = 2.4V
I_{OZL}	3-State output OFF current LOW			2	−50	μA	Max	V_{OUT} = 0.5V
I_{OS}[7]	Output short-circuit current	Standard[5]/ 3-State	−60	−80	−150	μA	Max	V_{OUT} = 0V
		Buffers/Line Drivers	−100	−150	−225			

NOTES
1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. Unless otherwise stated on individual data sheets.
3. Typical characteristics refer to T_A = +25°C and V_{CC} = +5.0V.
4. Min and Max refer to the values listed in the table of recommended operating conditions.
5. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-State outputs.
6. Used as an input current test at maximum input voltage for parts with an NPN input structure. This is not a leakage test.
7. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Table 4. AC Characteristics

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS		54/74F T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F T_A, V_{CC} = Mil, C_L = 50pF, R_L = 500Ω		74F T_A, V_{CC} = Com'l, C_L = 50pF, R_L = 500Ω		UNIT
				Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 6, 'F374		100			60		70		MHz
t_{PLH} t_{PHL}	Propagation delay Latch Enable to output	Waveform 1, 'F373		3.0 2.0	9.0 4.0	11.5 7.0	3.0 2.0	17.0 8.5	5.0 3.0	13.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4, 'F373		3.0 2.0	5.3 3.7	7.0 5.0	3.0 1.7	8.5 6.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 6, 'F374		4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.5 13.0	4.0 4.0	10.0 10.0	ns
t_{PZH}	Enable time to HIGH level	Waveform 2	'F373 'F374	2.0 2.0	5.0 9.0	11.0 11.5	2.0 2.0	13.5 14.0	2.0 2.0	12.0 12.5	ns
t_{PZL}	Enable time to LOW level	Waveform 3	'F373 'F374	2.0 2.0	5.6 5.3	7.5 7.5	2.0 2.0	10.5 10.0	2.0 2.0	8.5 8.5	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2	'F373 'F374	2.0 2.0	4.5 5.3	6.5 7.0	2.0 2.0	10.0 8.0	2.0 2.0	7.5 8.0	ns
t_{PLZ}	Disable time from LOW level	Waveform 3	'F373 'F374	2.0 2.0	3.8 4.3	5.0 5.5	2.0 2.0	7.0 7.5	2.0 2.0	6.0 6.5	ns

NOTE
Subtract 0.2ns from minumum values for SO package.

Table 5. AC Setup Requirements

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F T_A, V_{CC} = Mil, C_L = 50pF, R_L = 500Ω		74F T_A, V_{CC} = Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_W (H) t_W (L)	Latch Enable pulse width	Waveform 1, 'F373	6.0 6.0			6.0 6.0		6.0 6.0		ns
t_s (H) t_s (L)	Setup time, Data to Latch Enable	Waveform 5, 'F373	2.0 2.0			2.0 2.0		2.0 2.0		ns
t_h (H) t_h (L)	Hold time, Data to Latch Enable	Waveform 5, 'F373	3.0 3.0			3.0 3.0		3.0 3.0		ns
t_w (H) t_w (L)	Clock Pulse width	Waveform 6, 'F374	7.0 6.0			7.0 6.0		7.0 6.0		ns
t_s (H) t_s (L)	Setup time, Data to Clock	Waveform 7, 'F374	2.0 2.0			2.5 2.0		2.0 2.0		ns
t_h (H) t_h (L)	Hold time, Data to Clock	Waveform 7, 'F374	2.0 2.0			2.0 2.5		2.0 2.0		ns

TEST CIRCUITS AND WAVEFORMS

The 500Ω load resistor, R_L to ground, as described in Figure 1, *acts as a ballast to slightly load the totem-pole pull-up* and limit the quiescent *HIGH-state voltage to about +3.5V*. Otherwise, an output would rise quickly to about +3.5V, but then continue to rise very slowly up to about +4.4V. On the subsequent HIGH-to-LOW transition, the observed t_{PHL} would vary slightly with duty cycle, depending on how long the output voltage was allowed to rise before switching to the LOW state. Perhaps, more importantly, the *500Ω resistor to ground can be a high-frequency, passive probe for a sampling scope*, which costs much less than the equivalent high-impedance probe. Alternatively, the *500Ω load to ground can simply be a 450Ω resistor feeding into a 50Ω coaxial cable leading to a sampling scope input connector, with the internal 50Ω* termination of the scope completing the path to ground. Note that with this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50Ω termination for the pulse generator that supplies the input signal.

Figure 2, Test Circuit for 3-State Outputs, shows a second 500Ω resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring a device with Open-Collector outputs and for measuring one set of the Enable/Disable parameters (LOW-to-OFF and OFF-to-LOW) of a 3-State output. With the switch closed, the pair of 500Ω resistors and the +7.0V supply establish a quiescent HIGH level of +3.5V, which correlates with the HIGH level discussed in the preceding paragraph.

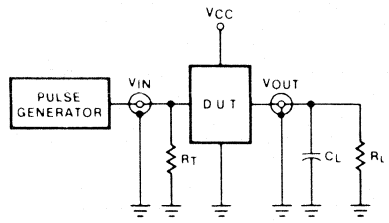
As shown in Figure 3, AC Waveforms for FAST 54/74F373, 54/74F374, the disable times are measured at the point where the output voltage has risen or fallen by 0.3V from the quiescent level (i.e., LOW for t_{PLH}[2] or HIGH for t_{PHL}[2]).

Since the rising or falling waveform is RC-controlled, the 0.3V of change is more linear and is less susceptible to external influences.

More importantly, from the system designer's point of view, 0.3V is adequate to ensure that a device output has turned OFF. It also gives system designers more realistic delay times to use in calculating minimum cycle times.

Good, high-frequency wiring practices should be used in constructing test jigs.

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS

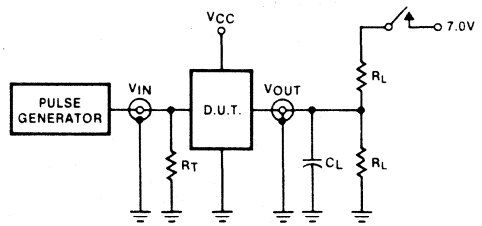


DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Figure 1. Test Circuit for Totem-Pole Outputs, 54/74F00

TEST CIRCUIT FOR 3-STATE AND OPEN-COLLECTOR (OC) OUTPUTS



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
OC	closed
All other	open

DEFINITIONS

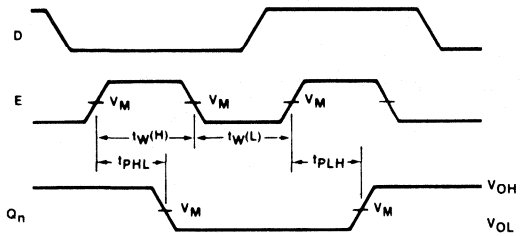
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

Figure 2. Test Circuits for 3-State and Open-Collector Outputs

Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths. Input signals should have rise and fall times of 2.5ns, and signal swing of 0V to +3.0V, 1.0MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{MAX}. Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time, etc.

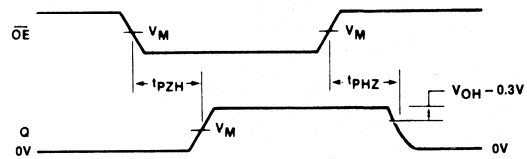
AC WAVEFORMS

LATCH ENABLE TO OUTPUT DELAYS
AND LATCH ENABLE PULSE WIDTH



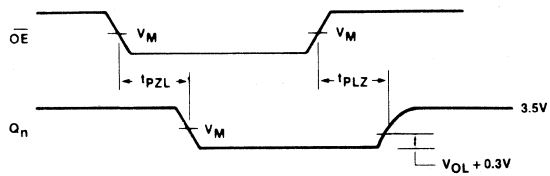
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL
AND DISABLE TIME FROM HIGH LEVEL



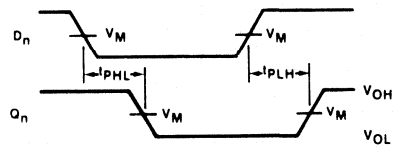
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL
AND DISABLE TIME FROM LOW LEVEL



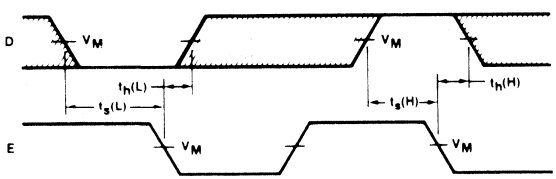
Waveform 3

PROPAGATION DELAY DATA
TO Q OUTPUTS



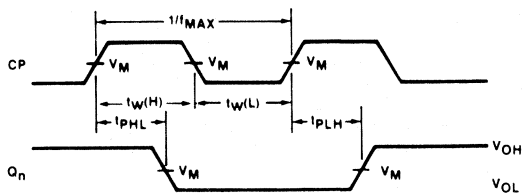
Waveform 4

DATA SETUP AND HOLD TIMES



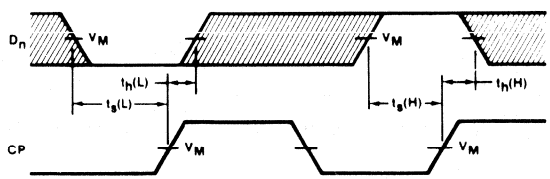
Waveform 5

CLOCK TO OUTPUT DELAYS
AND CLOCK PULSE WIDTH



Waveform 6

DATA SETUP AND HOLD TIMES



Waveform 7

$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 3. AC Waveforms for FAST 54/74F373, 54/74F374

DATA SHEET SPECIFICATION GUIDE

DC SYMBOLS AND DEFINITIONS

Voltages — All voltages are referenced to ground. Negative-voltage limits are specified as absolute values (i.e., – 10V is greater than – 1.0V).

V_{CC} **Supply voltage:** The range of power supply voltage over which the device is guaranteed to operate within the specified limits.

V_{IK} (Max) **Input clamp diode voltage:** The most negative voltage at an input when the specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode intended to clamp negative ringing at the input terminal.

V_{IH} **Input HIGH voltage:** The range of input voltages recognized by the device as a logic HIGH.

V_{IH} (Min) **Minimum Input HIGH voltage:** This value is the guaranteed input HIGH threshold for the device. The minimum allowed input HIGH in a logic system.

V_{IL} **Input LOW voltage:** The range of input voltages recognized by the device as a logic LOW.

V_{IL} (Max) **Maximum Input LOW voltage:** This value is the guaranteed input LOW threshold for the device. The maximum allowed input LOW in a logic system.

V_M **Measurement voltage:** The reference voltage level on AC waveforms for determining AC performance. Usually specified as 1.5V for the FAST family.

V_{OH} (Min) **Output HIGH voltage:** The minimum guaranteed HIGH voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.

V_{OL} (Max) **Output LOW voltage:** The maximum guaranteed LOW voltage at an output terminal sinking the specified load current I_{OL}.

V_{T+} **Positive-going threshold voltage:** The input voltage of a variable threshold device which causes operation according to specification as the input transition rises from below V_{T-} (Min).

V_{T-} **Negative-going threshold voltage:** The input voltage of a variable threshold device which causes operation according to specification as the input transition falls from above V_{T+} (Max).

Currents — Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of device. All current limits are specified as absolute values.

I_{CC} **Supply current:** The current flowing into the V_{CC} supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst-case operation unless specified.

I_I **Input leakage current:** The current flowing into an input when the maximum allowed voltage is applied to the input. This parameter guarantees the minimum breakdown voltage for the input.

I_{IH} **Input HIGH current:** The current flowing into an input when a specified HIGH-level voltage is applied to that input.

I_{IL} **Input LOW current:** The current flowing out of an input when a specified LOW-level voltage is applied to that input.

I_{OH} **Output HIGH current:** The leakage current flowing into a turned off Open-Collector output with a specified HIGH output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the HIGH state.

I_{OL} **Output LOW current:** The current flowing into an output which is the LOW state.

I_{OS} **Output short-circuit current:** The current flowing out of an output which is in the HIGH state when that output is short circuit to ground.

I_{OZH} **Output off current HIGH:** The current flowing into a disabled 3-State output with a specified HIGH output voltage applied.

I_{OZL} **Output off current LOW:** The current flowing out of a disabled 3-State output with a specified LOW output voltage applied.

AC SYMBOLS AND DEFINITIONS

f_{MAX} **Maximum clock frequency:** The maximum input frequency at a Clock input for predictable performance. Above this frequency the device may cease to function.

t_{PLH} **Propagation delay time:** The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} **Propagation delay time:** The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.

t_{PHZ} **Output disable time from HIGH level of a 3-State output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from the HIGH level to a high-impedance "off" state.

t_{PLZ} **Output disable time from LOW level of a 3-State output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from the LOW level to a high-impedance "off" state.

t_{PZH} **Output enable time to a HIGH level of a 3-State output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from a high-impedance "off" state to HIGH level.

t_{PZL} **Output enable time to a LOW level of a 3-State output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from a high-impedance "off" state to LOW level.

t_h **Hold time:** The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

DATA SHEET SPECIFICATION GUIDE

t_s **Setup time:** The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_W **Pulse width:** The time between the specified reference points on the leading and trailing edges of a pulse.

t_{rec} **Recovery time:** The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

t_{TLH} **Transition time, LOW-to-HIGH:** The time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from LOW to HIGH.

t_{THL} **Transition time, HIGH-to-LOW:** The time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from HIGH to LOW.

t_r, t_f **Clock input rise and fall times:** 10% to 90% value.

DESIGN CONSIDERATIONS

INTRODUCTION

The properties of high-speed FAST logic circuits dictate that care be taken in the design and layout of a system.

Some general design considerations are included in this section. This is not intended to be a thorough guideline for designing FAST systems, but a reference for some of the constraints and techniques to be considered when designing a high-speed system.

HANDLING PRECAUTIONS

As described in the Circuit Characteristics section, FAST devices can be more susceptible to damage from electrostatic discharge (ESD).

- Signetics FAST devices are shipped in conducting foam or anti-static tubes and foil-lined boxes to minimize ESD during shipment and unloading.
- Before opening the shipment of FAST devices, make sure that the individual is grounded and all handling means (such as tools, fixtures, and benches) are grounded.
- After removal from the shipping material, the leads of the FAST devices should always be grounded. In other words, FAST devices should be placed leads-down on a grounded surface, since ungrounded leads will attract static charge.
- Do not insert or remove devices in sockets with power applied. Ensure that power supply transients, such as occur during power turn on-off, do not exceed absolute maximum ratings.
- After assembly on PC boards, ensure that ESD is minimized during handling, storage or maintenance.
- FAST inputs should never be left floating on a PC board. This precaution applies to any TTL family. As a temporary measure, a resistor with a resistance greater than 10k ohms should be soldered on the open input. The resistor will limit accidental damage if the PC board is removed and brought into contact with static-generating materials.

INPUT CLAMPING

FAST circuits are provided with clamp diodes on the device inputs to minimize negative ringing effects. These diodes should not be used to clamp negative DC voltages or long-duration, negative pulses. Certain FAST part types with the NPN base input structure also provide clamping of positive overshoots.

UNUSED INPUTS

Proper digital design rules dictate that all unused inputs on TTL devices be tied either HIGH or LOW. This is especially important with FAST logic.

Electrically-open inputs can degrade AC noise immunity as well as the switching speed of the device. Small geometries make FAST more susceptible to damage by electrostatic discharge than other TTL families. Tying inputs to V_{CC} or GND, directly or through a resistor, protects the device from in-circuit electrostatic damage. Additionally, while most unconnected TTL inputs float HIGH, FAST devices with NPN inputs float LOW.

FAST devices do not require an input resistor to tie the input HIGH. Inputs can be connected directly to V_{CC} as well as ground.

Possible ways of handling unused inputs are:

1. Unused active-HIGH NAND or AND inputs to V_{CC}. The inputs should be maintained at a voltage greater than 2.7V, but should not exceed the absolute maximum rating.
2. Connect unused active-HIGH NOR or OR inputs to ground.
3. Tie unused active-HIGH NAND or AND inputs to an used input of the same gate, provided that the HIGH-level fan-out of the driving circuit is not impaired.
4. Connect the unused active-HIGH NAND or AND inputs to the output of an unused gate that is forced HIGH.

MIXING FAST WITH OTHER TTL FAMILIES

Most TTL families are intended to be used together, but this cannot be done indiscriminately. Each family of TTL devices has unique input and output characteristics optimized to achieve the desired speed or power features. High-speed devices such as 54/74F are designed with relatively low input and output impedances. The speed of these devices is determined primarily by fast rise and fall times internally, as well as at the input and output nodes. These fast transitions cause noise of various types in the system. Power and ground line noise is generated by the large currents needed to charge and discharge the circuit and load capacitances during the switching transitions. Signal line noise is generated by the fast output transitions and the relatively low output impedances, which tend to increase reflections.

The noise generated by these 54/74F devices can only be tolerated in systems designed with very short signal leads, ground planes, and good, well-bypassed power distribution networks. Mixing the slower TTL families such as 54/74 and 54LS/74LS with the higher speed families is also possible but must be done with caution. The slower speed families are more susceptible to induced noise than the higher speed families due to their higher input and output impedances. The low power Schottky 54/74LS family is especially sensitive to induced noise and must be isolated as much as possible from the 54/74F devices. Separate or isolated power and ground systems are recommended, and the LS input signal lines should not run adjacent to lines driven by 54/74F.

INPUT LOADING AND OUTPUT DRIVE COMPARISON

The logic levels of all TTL products are fully compatible with each other. However, the input loading and output drive characteristics of each family are different and must be taken into consideration when mixing them in a system. Table 1 shows the relative drive capabilities of each family for commercial temperature and voltage ranges. For military ranges, the 74LS drive capabilities must be cut in half. Note that 74F buffers have three times the drive capability of standard 74F devices; in fact, they can drive more loads than any other non-buffer TTL device.

INPUT-OUTPUT LOADING AND FAN-OUT TABLE

For convenience in system design, the input-output loading and fan-out characteristics of each circuit are specified in terms of unit loads and actual load value. One FAST Unit Load (U.L.) in the HIGH state is defined as 20μA; thus both the input HIGH leakage current, I_{IH}, and output HIGH current-sourcing capability, I_{OH}, are normalized to 20μA.

Similarly, one FAST Unit Load (U.L.) in the LOW state is defined as 0.6mA and both the input LOW current, I_{IL}, and input LOW current/TL, and the output LOW current-sinking capability, I_{OL}, are normalized to 0.6mA.

For added convenience, the actual load value in amperes is listed in the column adjacent to U.L.

On some FAST devices, high-impedance NPN base input structure has been utilized.

DESIGN CONSIDERATIONS

Table 1. Loading Comparisons

DRIVEN DEVICE FAMILY:		74F	74F (NPN)	74LS	74	74S	8200/9300	82S00
DRIVING DEVICE FAMILY	I_{IL} (Max) / I_{OL} (Min)	0.6mA	20μA	0.4mA	1.6mA	2.0mA	1.6mA	0.4mA
		Maximum Number of Loads Driven						
74F	20mA	33	1,000	50	12.5	10	12	50
74F (NPN)	64mA	106	3,200	160	40	32	40	160
74LS	8mA	13	400	20	5	4	5	20
74LS Buffer	24mA	40	1,200	60	15	12	15	60
74	16mA	26	800	40	10	8	10	40
74 Buffer	40mA	78	2,400	120	30	24	30	120
74S	20mA	33	1,000	50	12.5	10	12	50
74S Buffer	60mA	100	3,000	150	37.5	30	37	150
8800/9300	16mA	26	800	40	10	8	10	40
82S00	20mA	33	1,000	50	12	10	12	50

With this structure, the LOW level input current, I_{IL}, has been reduced to 20μA. This characteristic is 30 times lower than the requirement of devices using the conventional input structure. This feature improves fan-out in the LOW state and can help reduce part count in system design by eliminating buffers in some applications.

CLOCK PULSE REQUIREMENTS

All FAST clock inputs are buffered to increase their tolerance of slow positive-clock edges and heavy ground noise. Nevertheless, the rise time on positive-edge-triggered devices should be less than the nominal clock-to-output delay time measured between 0.8V to 2.0V levels of the clock driver for added safety margin against heavy ground noise. Not only a fast rising, clean clock pulse is required, but the path between the clock drive and clock input of the device should be well-shielded from electromagnetic noise.

FAST OUTPUTS TIED TOGETHER

The only FAST outputs that are designed to be tied together are Open-Collector and 3-State outputs. Standard FAST outputs should not be tied together unless their logic levels will always be the same; either all HIGH or all LOW. When connecting Open-Collector or 3-State outputs together, some general guidelines must be observed.

Open-Collector Outputs

These devices must be used whenever two or more OR-tied outputs will be at opposite logic levels at the same time. These devices must have a pull-up resistor (or resistors) added between the OR-tie connector and V_{CC} to establish an active-HIGH level. Only special high-voltage buffers can be tied to a higher voltage than V_{CC}. The minimum and maximum size of the pull-up resistor is determined as follows:

$$R(\text{Min}) = \frac{V_{CC}(\text{Max}) - V_{OL}}{I_{OL} - N_2(I_{IL})}$$

$$R(\text{Max}) = \frac{V_{CC}(\text{Min}) - V_{OH}}{N_1(I_{OH}) + N_2(I_{IH})}$$

where: I_{OL} = Minimum I_{OL} guarantee or OR-tied elements.

$N_2(I_{IL})$ = Cumulative maximum input LOW current for all inputs tied to OR-tie connection.

$N_1(I_{OH})$ = Cumulative maximum output HIGH leakage current for all outputs tied to OR-tie connection.

$N_2(I_{IH})$ = Cumulative maximum input HIGH leakage current for all inputs tied to OR-tie connection.

If a resistor divider network is used to provide the HIGH level, the R (Max) must be decreased enough to provide the required [(V_{OH}/R (pull-down)] current.

Minimum propagation delay results when the minimum value of external pull-up resistor is used in Load Circuit 1, Figure 1. Diodes should be fast recovery 1N4376 or equivalent. External pull-up resistor, Load Circuits 2 and 3, give progressively slower propagation delays.

3-State Outputs

3-State outputs are designed to be tied together, but are not designed to be active simultaneously. In order to minimize noise and protect the outputs from excessive power dissipation, only one 3-State output should be active at any time. This generally requires that the output enable signals be non-overlapping. When TTL decoders are used to enable 3-State outputs, the decoder should be disabled while the address is being changed. Since all TTL decoder outputs are subject to decoding spikes, non-overlapping signals cannot normally guarantee when the address is changing.

Since most 3-State output enable signals are active-LOW, shift registers or edge-triggered storage registers provide good output enable buffers. Shift registers with one circulating LOW bit, such as the 'F164 or 'F194, are ideal for sequential enable signals. The 'F174 or 'F273 can be used to buffer enable signals from TTL decoders or microcode (ROM) devices. Since the outputs of these registers will change from LOW-to-HIGH faster than from HIGH-to-LOW, the selection of one device at a time is assured.

GND

Good system design starts with a well-thought-out ground layout. Try to use ground plane if possible. This will save headaches later on. If ground strip is used, try to reduce ground path in order to minimize ground inductance. This prevents crosstalk problems. Quite often, jumper wire is used for connecting to ground at the breadboarding stage, but a solid ground must be used even at the breadboarding stage.

V_{CC}

Typical dynamic impedance of un-bypassed V_{CC} runs from 50Ω to 100Ω, depending on V_{CC} and GND configuration. This why a sudden current demand, due to an IC output switching, can cause momentary reduction in V_{CC} unless a bypass (decoupling) capacitor is located near V_{CC}.

Not only is there a sudden current demand due to output switching transient, there is also a heavy current demand by the buffer driver. Assuming the buffer output sees a 50Ω dynamic load and the buffer LOW-to-HIGH transition is 2.5V, the current demand is 50mA per buffer. If it is an octal buffer, the current demand could be 0.4mA per package in 3ns time!

DESIGN CONSIDERATIONS

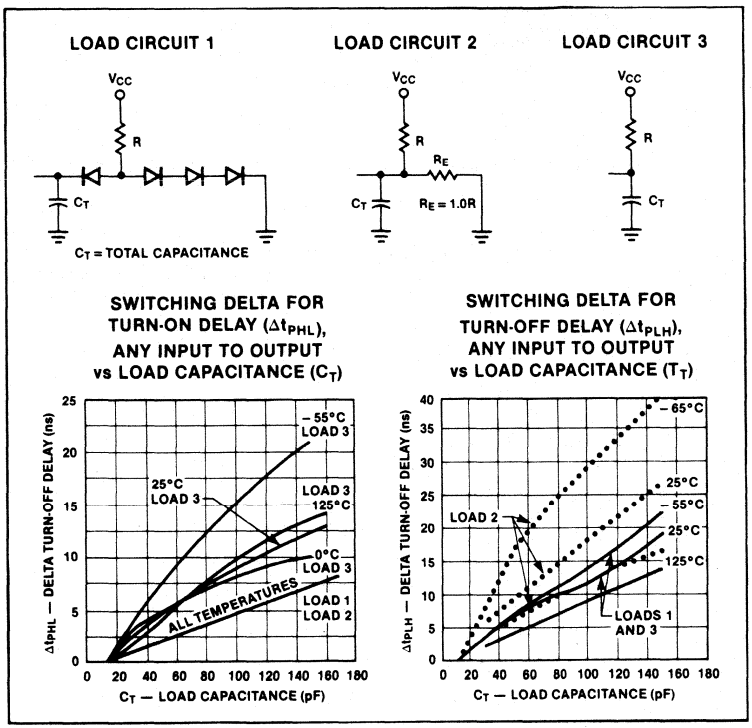


Figure 1

The next step is to figure out the capacitance requirement for each bypass capacitor. Using the previously-mentioned octal buffer and assuming the V_{CC} droop is 0.1V, then C is:

$$C = \frac{0.4A \times 3 \times 10^{-9}\,\text{sec}}{0.1V} = 12 \times 10F^{-9}$$

$$= 0.012\mu F$$

This formula is derived as follows:

$$Q = CV$$

by differentiation:

$$\frac{\Delta Q}{\Delta t} = C\frac{\Delta V}{\Delta t}$$

Since $\frac{\Delta Q}{\Delta t} = I$

the equation becomes $I = C\frac{\Delta t}{\Delta t}$

hence, $C = \frac{I\Delta t}{\Delta V}$

Select the C bypass ≥ 0.02μF and try to use a high-quality RF capacitor. Place one bypass capacitor for each buffer and one bypass capacitor every two other types of IC packages. Make sure that the leads are cut as short as possible.

In addition, place bypass capacitors on a board to take care of board-level current transients.

CROSSTALK

The best way to handle crosstalk is to prevent it from occurring in the first place; quick-fixes are troublesome and costly. To prevent crosstalk, maximize spacing between signal lines and minimize spacing between signal lines and ground lines. Preferably, place ground lines between signal lines. For added precaution, add a ground trace alongside either the potential crosstalker or the cross-listener.

For backplane, or wirewarp, use twisted pair for for sensitive functions — clocks, asynchronous set or reset, asynchronous parallel load especially leading to LS inputs. In flat cable, make every other conductor ground.

For multilayer P.C. boards, run signal lines in adjacent planes perpendicular to prevent magnetic coupling, and limit capacitive coupling. Use power shield (V_{CC} or ground plane) in between signal planes.

Since any voltage change, noise or otherwise, arriving at the unterminated end of transmission lines double in amplitude, terminating the line even partially reduces the amplitude of the signal (noise or otherwise) appearing at the end of the line; therefore, using a terminating resistor whose value is equal to the line characteristics impedance will help in reducing crosstalk.

NOTES

Section 5
54/74F Series

GATE

FAST 54/74F00

Quad Two-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F00	3.4ns	4.4mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74F00N	
Plastic SO	N74F00D	
Ceramic DIP		S54F00F
Ceramic LLCC		S54F00G

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

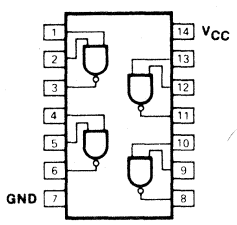
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A, B	Inputs	1.0/1.0	20μA/0.6mA
Y	Output	50/33	1.0mA/20mA

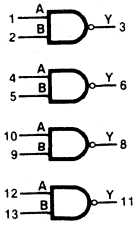
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

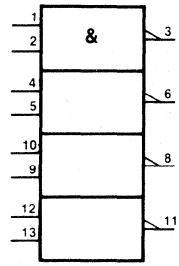
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F00			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V			−60	−80	−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	V_{IN} = GND		1.9	2.8	mA
			I_{CCL}	V_{IN} = 4.5V		6.8	10.2	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

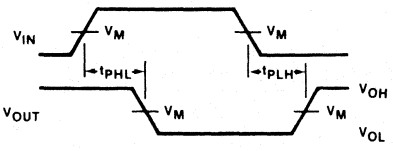
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1	2.4 2.0	3.7 3.2	5.0 4.3	2.0 1.2	7.0 6.5	2.4 2.0	6.0 5.3	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS

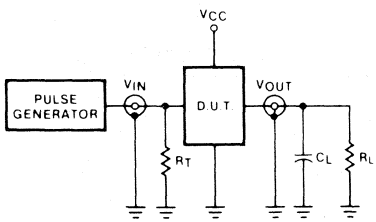


$V_M = 1.5V$

Waveform 1

TEST CIRCUITS AND WAVEFORMS

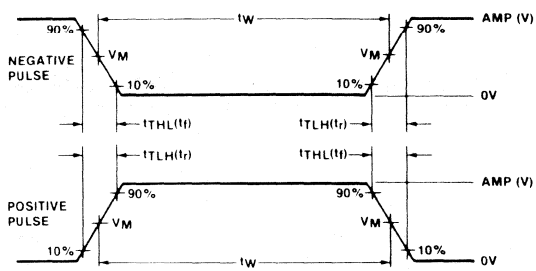
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

Quad Two-Input NOR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F02	3.4ns	4.4mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74F02N	
Plastic SO	N74F02D	
Ceramic DIP		S54F02F
Ceramic LLCC		S54F02G

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

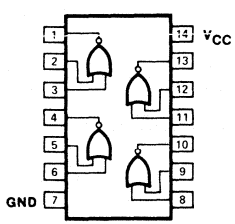
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

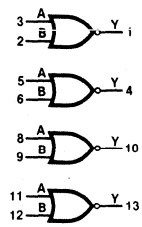
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A, B	Inputs	1.0/1.0	20μA/0.6mA
Y	Output	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

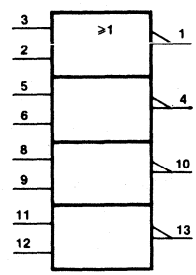
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

5

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F02			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V			−60	−80	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		3.0	5.6	mA
			I_{CCL}	Outputs LOW		7.0	13	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open.

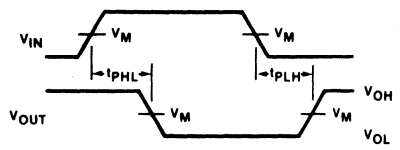
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL}	Waveform 1	2.5 2.0	4.4 3.2	5.5 4.3	2.5 1.5	7.5 6.5	2.5 2.0	6.5 5.3	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS

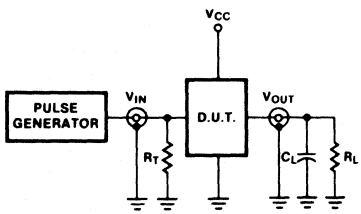


$V_M = 1.5V$

Waveform 1

TEST CIRCUITS AND WAVEFORMS

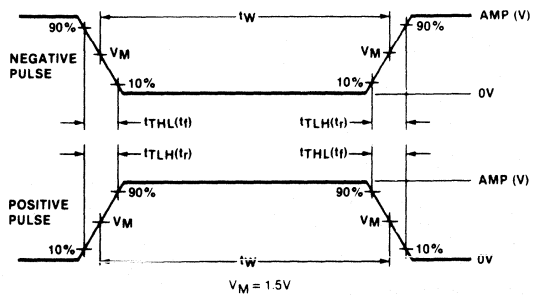
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

INVERTER

FAST 54/74F04

Hex Inverter

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F04	3.5ns	6.9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F04N	
Plastic SO	N74F04D	
Ceramic DIP		S54F04F
Ceramic LLCC		S54F04G

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

FUNCTION TABLE

INPUT	OUTPUT
A	Y
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

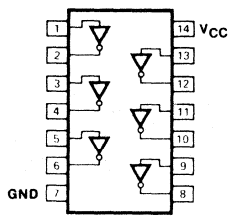
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	50/33	1.0mA/20mA

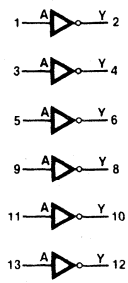
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

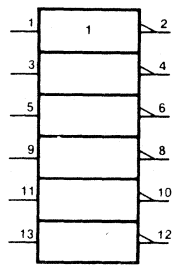
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



INVERTER FAST 54/74F04

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F04			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V			−60	−85	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		2.8	4.2	mA
			I_{CCL}	Outputs LOW		10.2	15.3	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH}, V_{IN} = GND; I_{CCL}, V_{IN} = 4.5V.

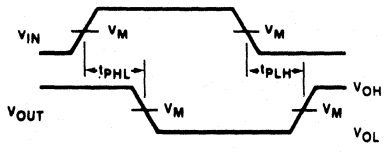
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F			54F		74F		UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1	2.4	3.7	5.0	1.5	8.0	2.4	6.0	ns
t_{PHL}		1.5	3.2	4.3	1.1	6.5	1.5	5.3	

NOTE
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS

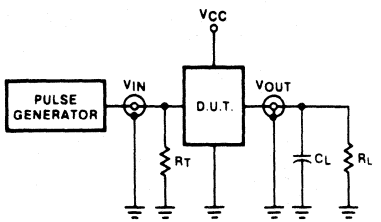


$V_M = 1.5V$

Waveform 1

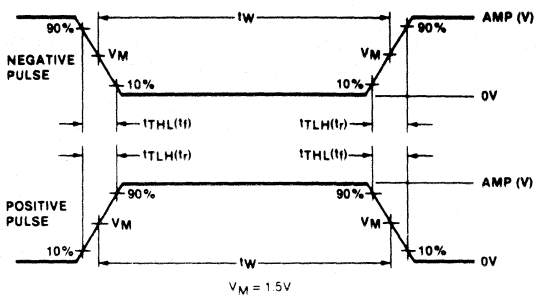
TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

Quad Two-Input AND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F08	4.1ns	7.1mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F08N	
Plastic SO	N74F08D	
Ceramic DIP		S54F08F
Ceramic LLCC		S54F08G

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

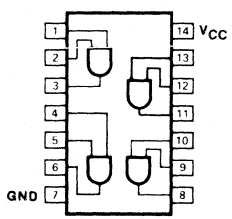
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

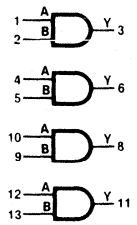
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A, B	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	50/33	1.0mA/20mA

Note:
One (1.0) FAST unit load (U.L.) is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

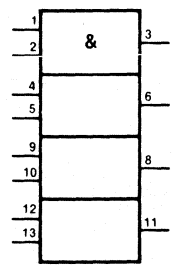
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

5

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F08			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		−60	−90	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		5.5	8.3	mA
			I_{CCL} Output LOW		8.6	12.9	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH}, V_{IN} = 4.5V; I_{CCL}, V_{IN} = GND.

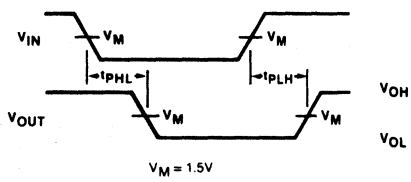
AC CHARACTERISTICS

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1	3.0 2.5	4.2 4.0	5.6 5.3	2.5 2.0	7.5 7.5	3.0 2.5	6.6 6.3	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS

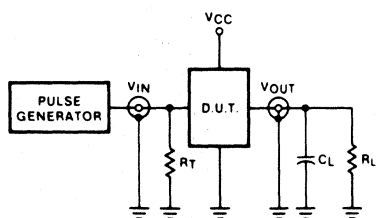


$V_M = 1.5V$

Waveform 1

TEST CIRCUITS AND WAVEFORMS

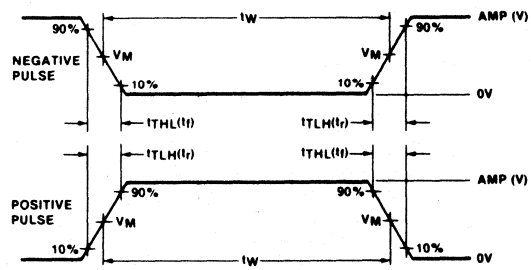
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Triple Three-Input NAND ('F10), AND ('F11) Gates

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F10	3.5ns	3.3mA
74F11	4.2ns	5.3mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F10N • N74F11N	
Plastic SO	N74F10D • N74F11D	
Ceramic DIP		S54F10F • S54F11F
Ceramic LLCC		S54F10G • S54F11F

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	C	Y('F10)	Y('F11)
L	L	L	H	L
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

H = HIGH voltage level
L = LOW voltage level

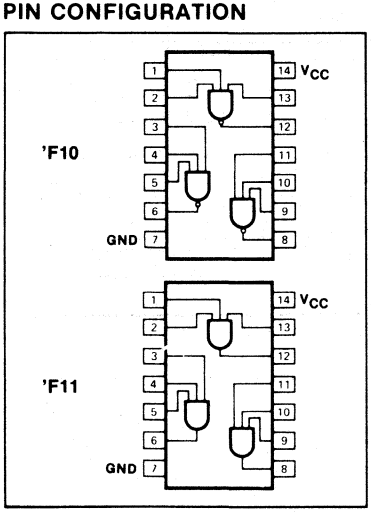
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A-C	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	50/33	1.0mA/20mA

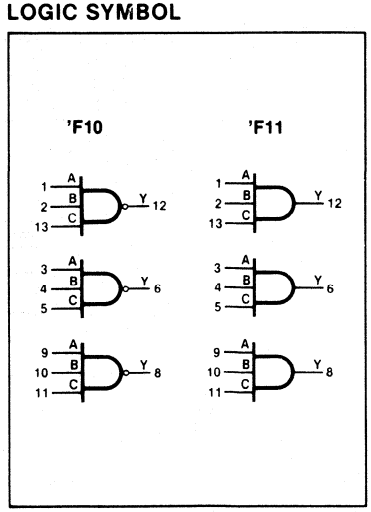
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

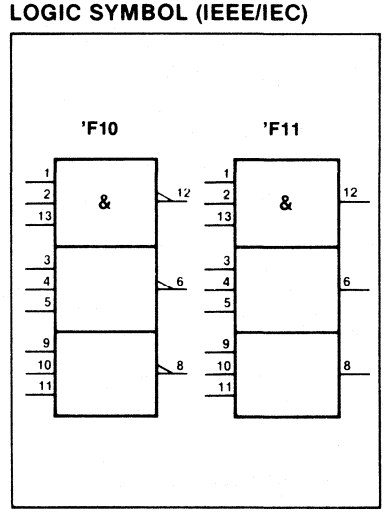
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F10, 11			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V			−60	−75	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH	'F10		1.8	2.1	mA
			I_{CCL} Outputs LOW			6.0	7.7	mA
			I_{CCH} Outputs HIGH	'F11		4.7	6.2	mA
			I_{CCL} Outputs LOW			7.2	9.7	mA

NOTES

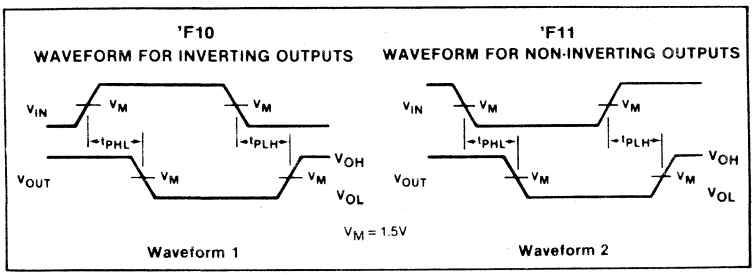
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. 'F10 measure I_{CCH} with V_{IN} = GND and I_{CCL} with V_{IN} = 4.5V.
   'F11 measure I_{CCH} with V_{IN} = 4.5V and I_{CCL} with V_{IN} = GND.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

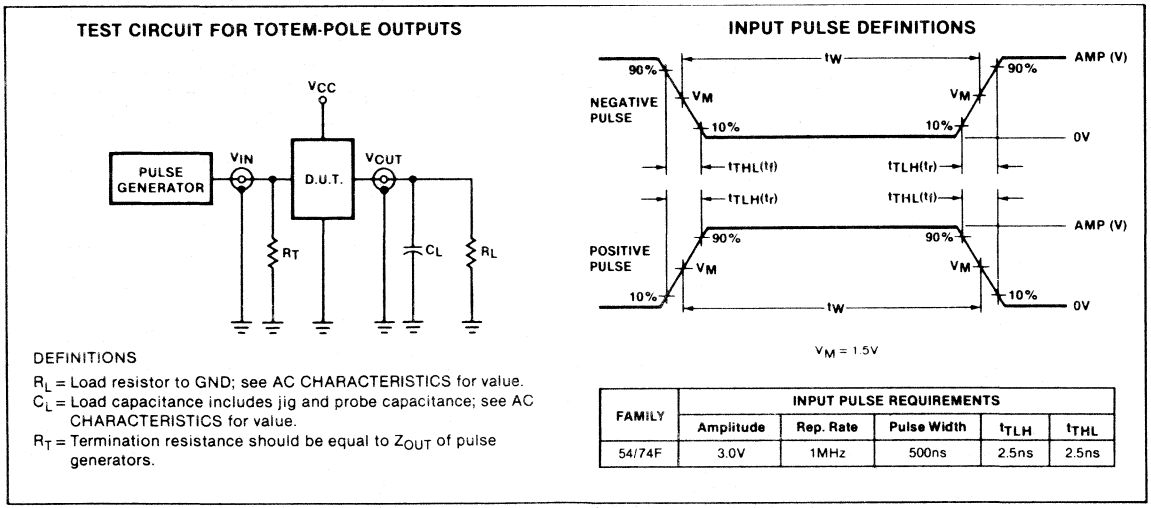
PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1 'F10	2.4	3.7	5.0	2.0	7.0	2.4	6.0	ns
t_{PHL}		2.0	3.2	4.3	1.5	6.5	2.0	5.3	
t_{PLH} Propagation delay	Waveform 2 'F11	3.0	4.2	5.6	2.5	7.5	3.0	6.6	ns
t_{PHL}		2.5	4.1	5.5	2.0	7.5	2.5	6.5	

NOTE
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

SCHMITT TRIGGER — FAST 54/74F13

Dual 4-Input NAND Schmitt Trigger

DESCRIPTION

The F13 contains two 4-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

Each circuit contains a 4-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than V_{T+MAX}, the gate will respond in the transitions of the other input as shown in Waveform 1.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F13	7.8ns	5.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74F13N	
Plastic SO	N74F13D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

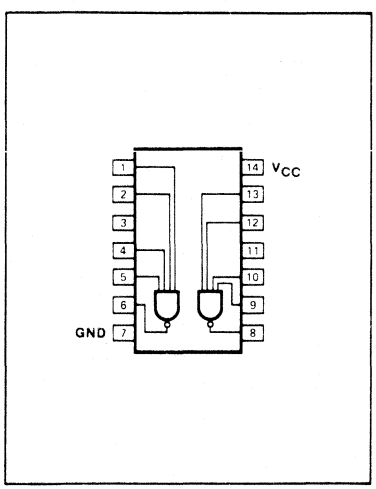
H = HIGH voltage level
L = LOW voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

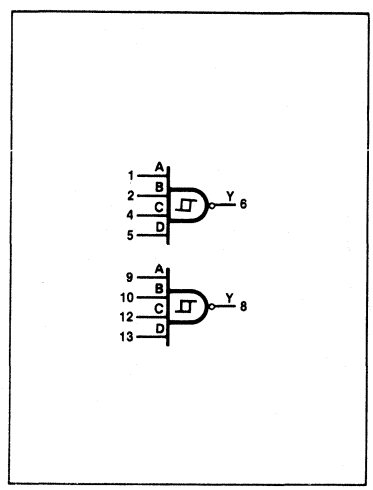
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A,B,C,D	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

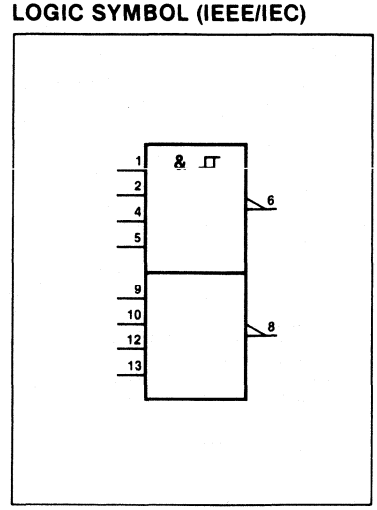
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



SCHMITT TRIGGER FAST 54/74F13

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F13			UNIT
				Min	Typ[2]	Max	
V_{T+}	Positive-going threshold	V_{CC} = 5.0V		1.5	1.7	2.0	V
V_{T-}	Negative-going threshold	V_{CC} = 5.0V		0.5	0.9	1.1	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5.0V		0.4	0.8		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_I = V_{T-MIN}, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_I = V_{T+MAX}, I_{OL} = MAX			0.3	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			− 0.73	− 1.2	V
I_{T+}	Input current at positive-going threshold	V_{CC} = 5.0V, V_I = V_{T+}			0		μA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5.0V, V_I = V_{T-}			− 350		μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			− 0.2	− 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		− 60	− 120	− 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		4.5	8.5	mA
			I_{CCL} Outputs LOW		7.0	10.0	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH}, V_{IN} = GND. I_{CCL}, V_{IN} = 4.5V.

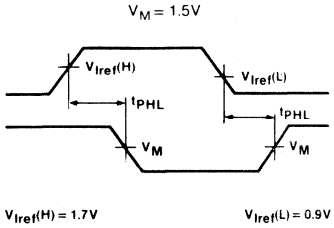
5

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F			54F		74F		UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1	4.0 9.0	5.5 11.0	7.0 13.5	3 9	11 16.5	4.0 9.0	8.0 13.5	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

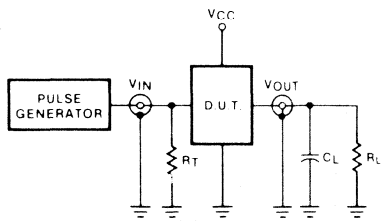
AC WAVEFORM



Waveform 1

TEST CIRCUITS AND WAVEFORMS

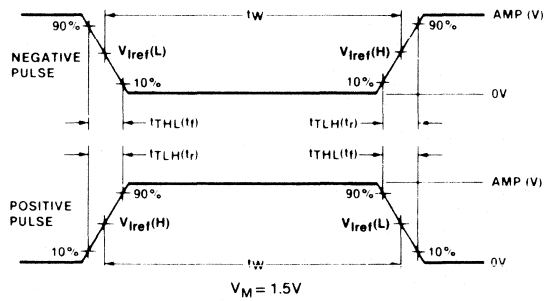
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

SCHMITT TRIGGER — FAST 54/74F14

Hex Inverter Schmitt Trigger

DESCRIPTION

The 'F14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F14	5.0 ns	18 mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F14N	
Plastic SO	N74F14D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

FUNCTION TABLE

INPUT	OUTPUT
A	Y
0	1
1	0

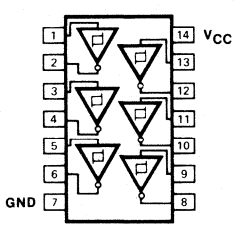
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	50/33	1.0mA/20mA

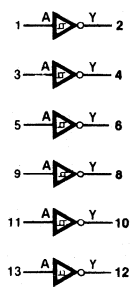
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

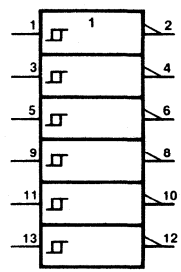
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



SCHMITT TRIGGER FAST 54/74F14

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F14			UNIT
				Min	Typ[2]	Max	
V_{T+}	Positive-going threshold	V_{CC} = 5.0V		1.4	1.7	2.0	V
V_{T-}	Negative-going threshold	V_{CC} = 5.0V		0.5	0.9	1.1	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5.0V		0.4	0.8		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_I = V_{T-MIN}, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_I = V_{T+MAX}, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_{T+}	Input current at positive-going threshold	V_{CC} = 5.0V, V_I = V_{T+}			0.0		μA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5.0V, V_I = V_{T-}			175		μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.2	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−135	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		13	22	mA
			I_{CCL} Outputs LOW		23	32	mA

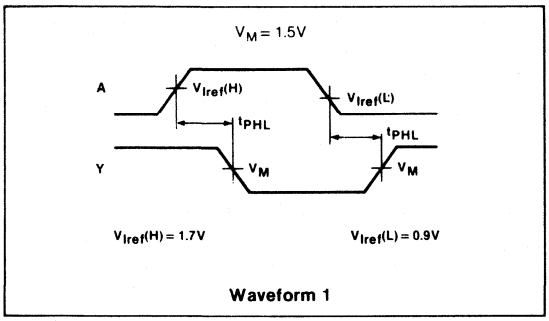
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH}, V_{IN} = GND; I_{CCL}, V_{IN} = 4.5V.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1	2.5 3.5	4.6 5.5	6.5 7.5	2.0 3.0	9.0 10.0	2.5 3.0	7.5 8.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

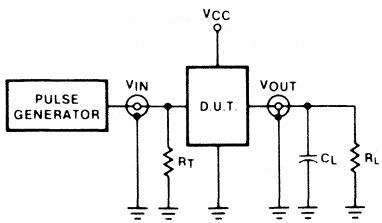
AC WAVEFORM



Waveform 1

TEST CIRCUITS AND WAVEFORMS

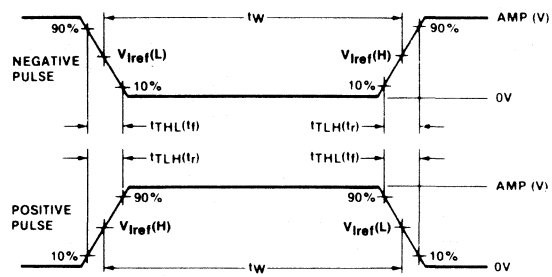
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

Dual Four-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F20	3.5ns	2.2mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74F20N	
Plastic SO	N74F20D	
Ceramic DIP		S54F20F
Ceramic LLCC		S54F20G

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

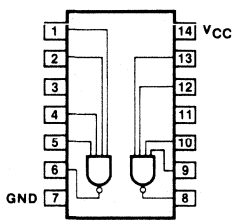
H = HIGH voltage level
L = LOW voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

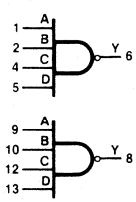
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A, B, C, D	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

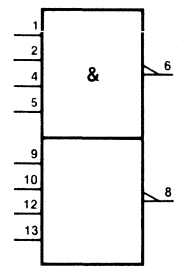
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

5

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F20			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V			−60	−85	−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	V_{IN} = GND		0.9	1.4	mA
			I_{CCL}	V_{IN} = 4.5V		3.4	5.1	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

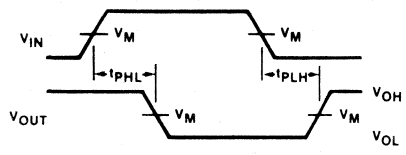
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1	2.4 2.0	3.7 3.2	5.0 4.3	2.0 1.5	7.0 6.5	2.4 2.0	6.0 5.3	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS

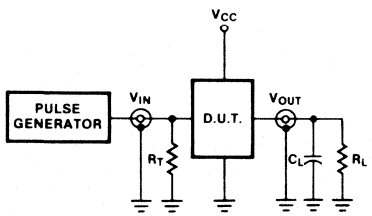


$V_M = 1.5V$

Waveform 1

TEST CIRCUITS AND WAVEFORMS

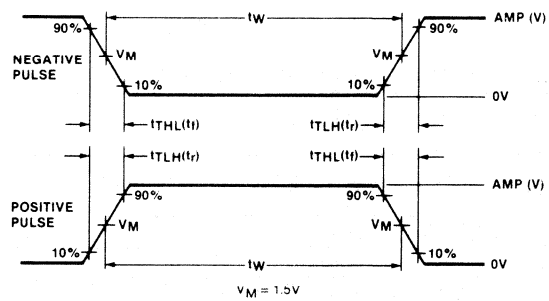
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Quad Two-Input OR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F32	4.1ns	8.2mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F32N	
Plastic SO	N74F32D	
Ceramic DIP		S54F32F
Ceramic LLCC		S54F32G

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH voltage level
L = LOW voltage level

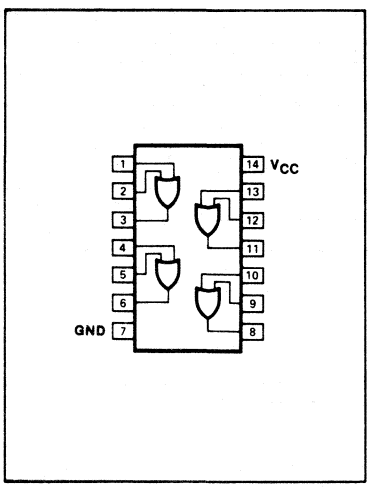
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A, B	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	50/33	1.0mA/20mA

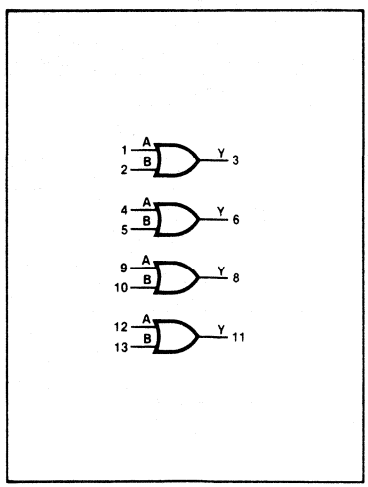
Note:
One (1.0) FAST unit load (U.L.) is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

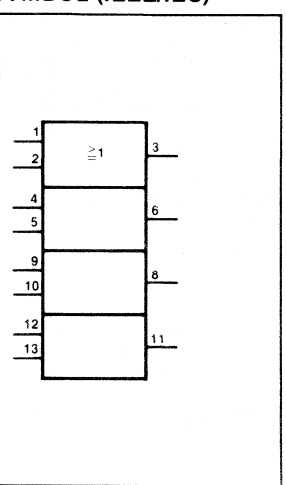
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F32			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		−60	−90	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		6.1	9.2	mA
			I_{CCL} Output LOW		10.3	15.5	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH}, V_{IN} = 4.5V; I_{CCL}, V_{IN} = GND.

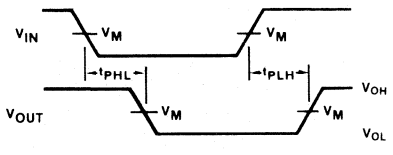
AC CHARACTERISTICS

PARAMETER	TEST CONDITIONS	54/74F			54F		74F		UNIT
		$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			T_A, V_{CC} Mil, $C_L = 50pF$, $R_L = 500\Omega$		T_A, V_{CC} Com'l, $C_L = 50pF$, $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL}	Waveform 1	3.0 3.0	4.2 4.0	5.6 5.3	3.0 2.5	7.5 7.5	3.0 3.0	6.6 6.3	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORM

WAVEFORM FOR NON-INVERTING OUTPUTS

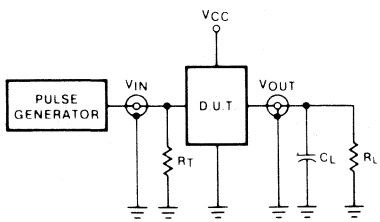


$V_M = 1.5V$

Waveform 1

TEST CIRCUITS AND WAVEFORMS

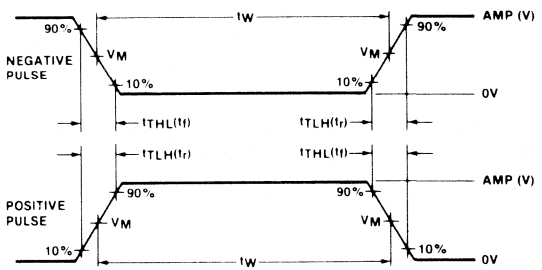
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

BUFFER

FAST 54/74F37

Preliminary

Quad Two-Input NAND Buffer

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F37	3.5ns	18mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74F37N	
Plastic SO	N74F37D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

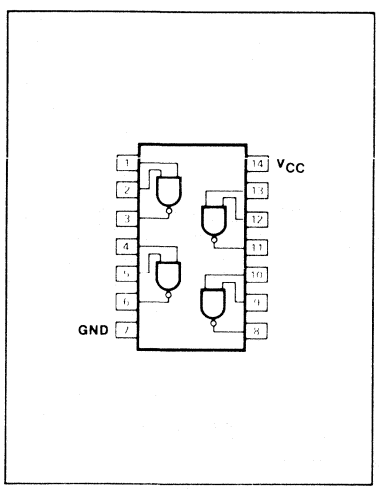
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

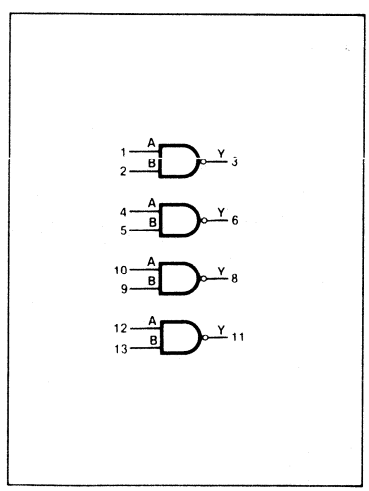
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A, B	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

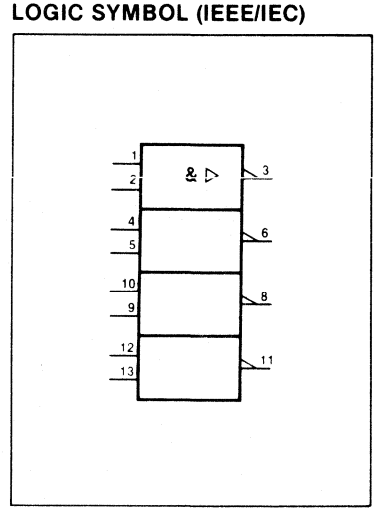
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



BUFFER FAST 54/74F37

Preliminary

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	128	128	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−3	mA
I_{OL}	LOW-level output current	Mil			48	mA
		Com'l			64	mA
T_A	Operating free-air temperature	Mil'l	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F37			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	Mil				V
				Com'l		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	2	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	V_{IN} = GND				mA
			I_{CCL}	V_{IN} = 4.5V			22	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

BUFFER

FAST 54/74F37

Preliminary

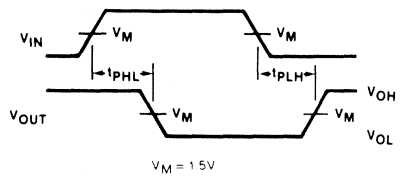
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F			54F		74F		UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1	2.4 1.5	3.7 3.2	5.0 4.3	2.0 1.5	7.0 6.5	2.4 2.0	6.0 6.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS

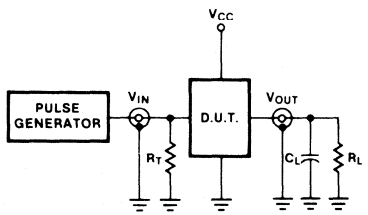


$V_M = 1.5V$

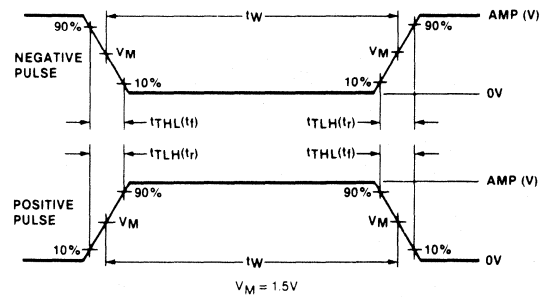
Waveform 1

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



$V_M = 1.5V$

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Preliminary

Quad Two-Input NAND Buffer (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F38	5.5ns	18mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74F38N	
Plastic SO	N74F38D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

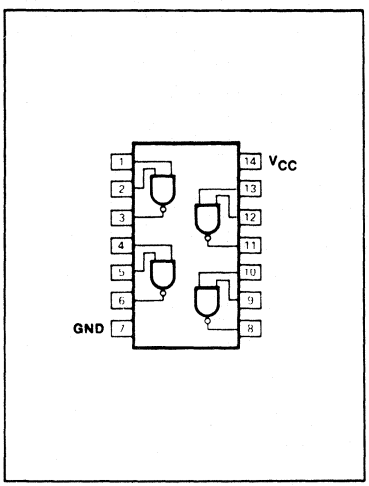
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A, B	Inputs	1.0/1.0	20μA/0.6mA
Y	Output	150/106.7	3.0mA/64mA

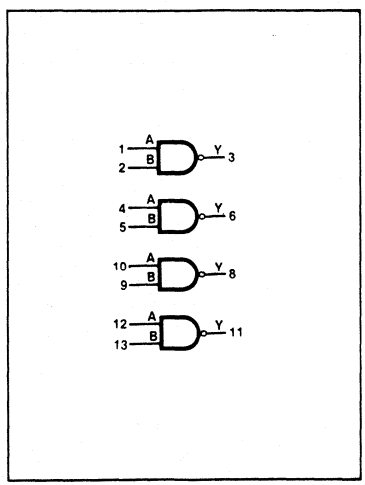
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

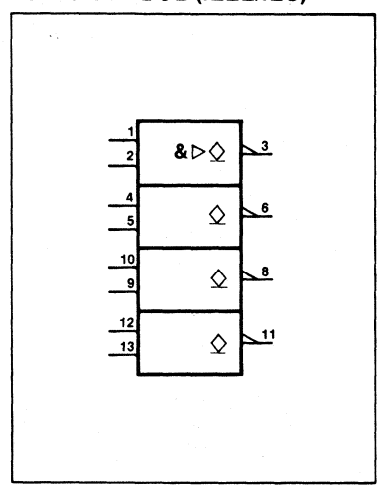
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Preliminary

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	128	128	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−3	mA
I_{OL}	LOW-level output current	Mil			48	mA
		Com'l			64	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F38			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	Mil				V
				Com'l		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	2	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	V_{IN} = GND			22	mA
			I_{CCL}	V_{IN} = 4.5V			22	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Preliminary

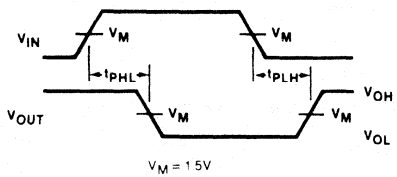
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F			54F		74F		UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1							9 6	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS

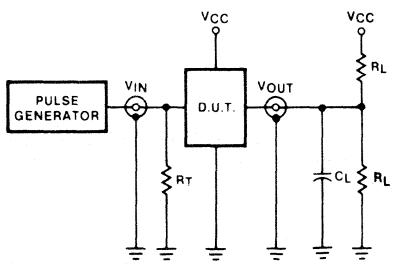


$V_M = 1.5V$

Waveform 1

TEST CIRCUITS AND WAVEFORMS

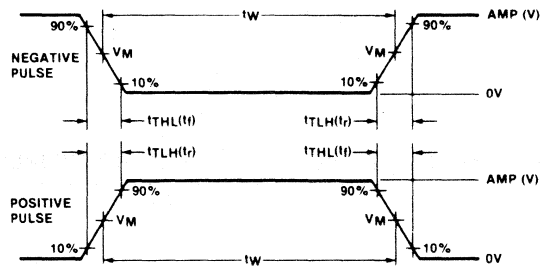
TEST CIRCUIT FOR OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

BUFFER

FAST 54/74F40

Preliminary

Dual Four-Input NAND Buffer

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F40	3.5ns	16mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74F40N	
Plastic SO	N74F40D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

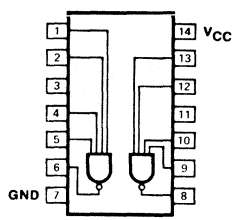
H = HIGH voltage level
L = LOW voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

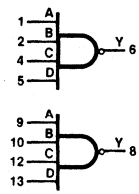
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A,B,C,D	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	150/106.7	3.0mA/64mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

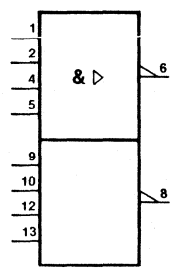
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Preliminary

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	128	128	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				-3	mA
I_{OL}	LOW-level output current	Mil			48	mA
		Com'l			64	
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

5

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F40			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{IL} = MAX, V_{CC} = MIN, I_{OL} = MAX, V_{IH} = MIN			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	2	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−100		−225	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH				mA
			I_{CCL} Outputs LOW			22	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH}, V_{IN} = GND; I_{CCL}, V_{IN} = Open.

BUFFER

FAST 54/74F40

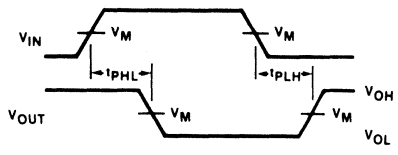
Preliminary

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1	2.4 1.5	3.7 3.2	5.0 4.3	2.0 1.5	7.0 6.5	2.4 2.0	6.0 6.0	ns

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS

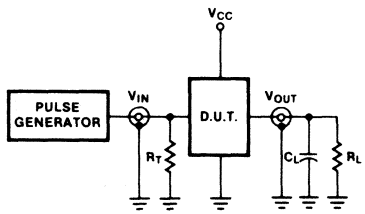


$V_M = 1.5V$

Waveform 1

TEST CIRCUITS AND WAVEFORMS

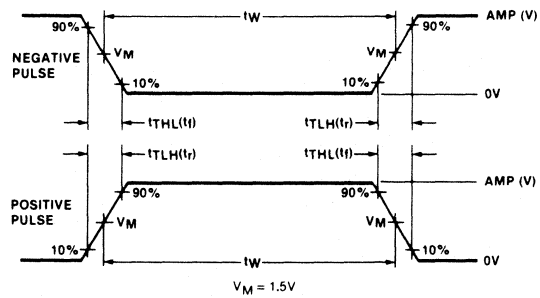
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Four-Two-Three-Two-Input AND-OR-Invert Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F64	4.0ns	2.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F64N	
Plastic SO	N74F64D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

FUNCTION TABLE

INPUTS											OUTPUT
A	B	C	D	E	F	G	H	J	K	L	Y
H	H	X	X	X	X	X	X	X	X	X	L
X	X	H	H	H	H	X	X	X	X	X	L
X	X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	X	H	H	L
All other combinations											H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

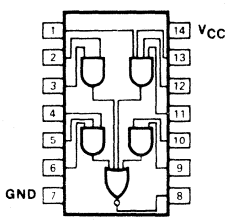
5

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

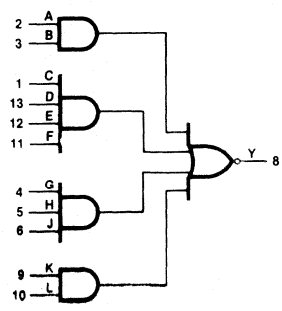
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A-L	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

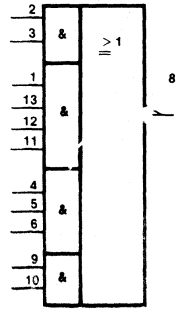
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1.0	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F64			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				− 0.73	− 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				− 0.4	− 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V			− 60	− 80	− 150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	V_{IN} = GND		1.9	2.8	mA
			I_{CCL}	V_{IN} = 4.5V		3.1	4.7	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

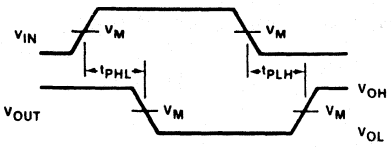
AC CHARACTERISTICS

PARAMETER	TEST CONDITIONS	54/74F			54F		74F		UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} Address to output	Waveform 1	2.5 2.0	4.6 3.2	6.0 4.5	2.5 1.5	8.0 6.5	2.5 2.0	7.0 5.5	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



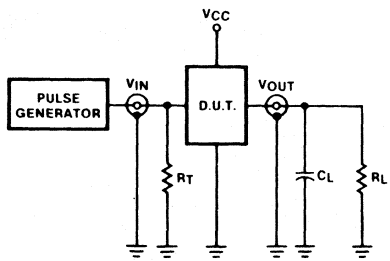
$V_M = 1.5V$

Waveform 1

5

TEST CIRCUITS AND WAVEFORMS

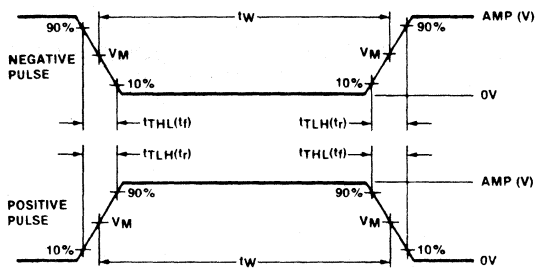
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FLIP-FLOP

FAST 54/74F74

Dual D-Type Flip-Flop

DESCRIPTION

The 'F74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs, and complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-LOW inputs and operate independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. The D inputs must be stable one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F74	125MHz	11.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F74N	
Plastic SO	N74F74D	
Ceramic DIP		S54F74F
Ceramic LLCC		S54F74G

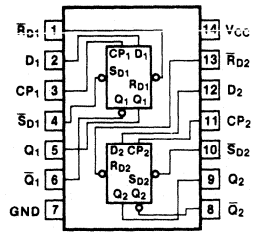
NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

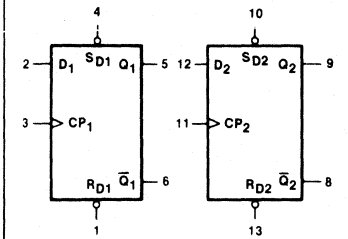
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
D_1, D_2	Data Inputs	1.0/1.0	20μA/0.6mA
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0	20μA/0.6mA
$\overline{R}_{D1}$, $\overline{R}_{D2}$	Reset Inputs (Active LOW)	1.0/3.0	20μA/1.8mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Set Inputs (Active LOW)	1.0/3.0	20μA/1.8mA
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

Note:
One (1.0) FAST unit load (U.L.) is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

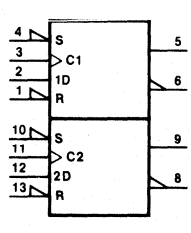
PIN CONFIGURATION



LOGIC SYMBOL

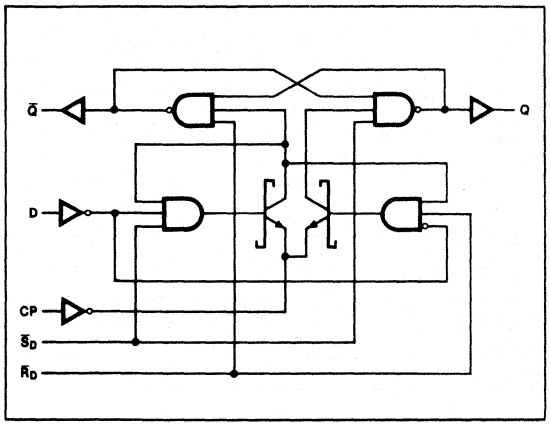


LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOP — FAST 54/74F74

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	L	H
Undetermined[a]	L	L	X	X	H	H
Load "1" (Set)	H	H	↑	h	H	L
Load "0" (Reset)	H	H	↑	l	L	H

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time *prior* to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

NOTE
(a) Both outputs will be HIGH if both $\overline{S}_D$ and $\overline{R}_D$ go LOW simultaneously.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F74 Min	54/74F74 Typ[2]	54/74F74 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V	All inputs		1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	D, CP inputs		−0.4	−0.6	mA
			$\overline{R}_D$, $\overline{S}_D$ inputs		−1.3	−1.8	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		−60	−85	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			11.5	16	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may rise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the Clock inputs grounded and all outputs open, with the Q and $\overline{Q}$ outputs HIGH in turn.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} = Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} = Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	125		80		100		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1	3.8 4.4	5.3 6.2	6.8 8.0	3.5 3.7	8.5 10.5	3.8 4.4	7.8 9.2	ns
t_{PLH} t_{PHL}	Propagation delay Set or Reset to output	Waveform 2	3.2 3.5	4.6 7.0	6.1 9.0	3.2 3.5	8.0 11.5	3.2 3.5	7.1 10.5	ns

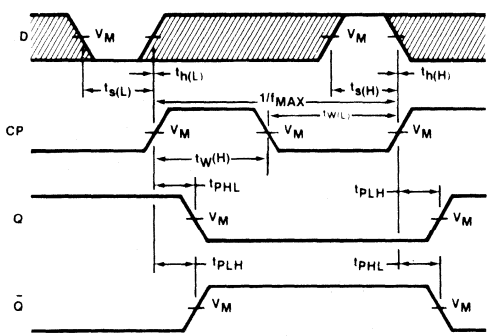
NOTE
Subtract 0.2ns from minimum values for SO package.

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			54F T_A, V_{CC} = Mil, $C_L = 50pF$, $R_L = 500\Omega$		74F T_A, V_{CC} = Com'l, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_S (H) t_S (L)	Setup time HIGH or LOW, Data to Clock	Waveform 1	2.0 3.0			3.0 4.0		2.0 3.0		ns
t_h (H) t_h (L)	Hold time HIGH or LOW, Data to clock	Waveform 1	1.0 1.0			2.0 2.0		1.0 1.0		ns
t_W (H) t_W (L)	Clock pulse width, HIGH or LOW	Waveform 1	4.0 5.0			4.0 6.0		4.0 5.0		ns
t_W (L)	$\overline{R}_D$ or $\overline{S}_D$ pulse width, LOW	Waveform 2	4.0			4.0		4.0		ns
t_{rec}	Recovery time, $\overline{R}_D$ or $\overline{S}_D$ to Clock	Waveform 3	2.0			3.0		2.0		ns

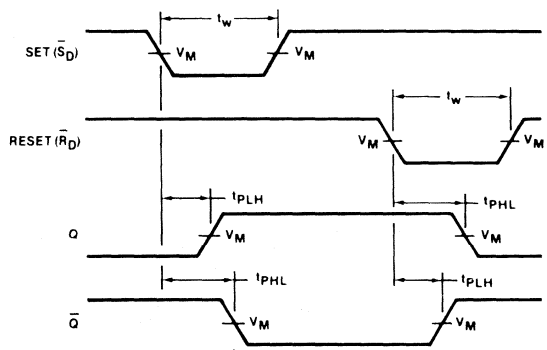
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, DATA SETUP AND HOLD TIMES, CLOCK PULSE WIDTH



Waveform 1

SET AND RESET TO OUTPUT DELAYS, SET AND RESET PULSE WIDTHS

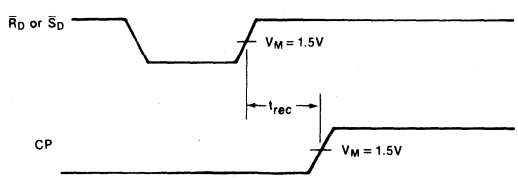


Waveform 2

$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

RECOVERY TIME

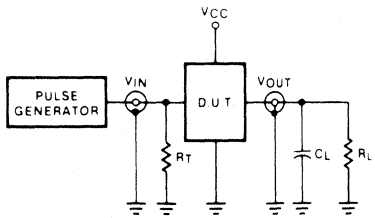


Waveform 3

5

TEST CIRCUITS AND WAVEFORMS

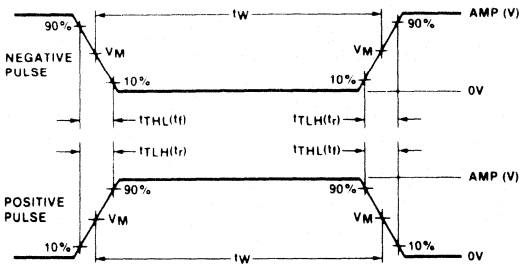
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

COMPARATOR FAST 54/74F85

Preliminary

4-Bit Magnitude Comparator

- **High Impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Magnitude comparison of any binary words**
- **Serial or parallel expansion without extra gating**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F85		40mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74F85N	
Plastic SO	N74F85D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A_0–A_3) and (B_0–B_3), where A_3 and B_3 are the most significant bits.

The operation of the 'F85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme.

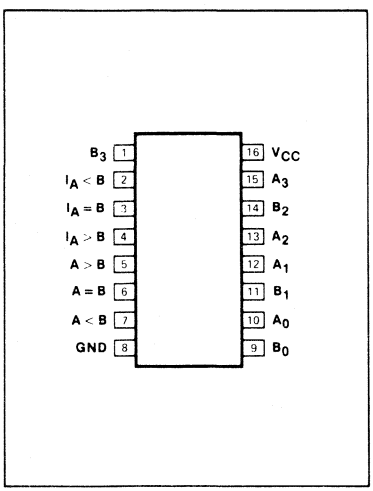
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A_0–A_3	Inputs	1.0/0.033	20μA/20μA
B_0–B_3	Inputs	1.0/0.033	20μA/20μA
$I_A<B$, $I_A=B$ $I_A>B$	Inputs	1.0/0.033	20μA/20μA
A>B, A=B A<B	Outputs	50/33	1.0mA/20mA

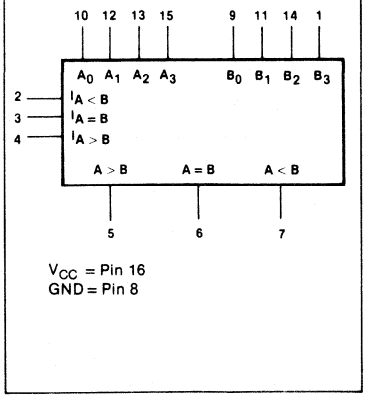
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

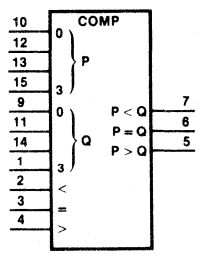
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



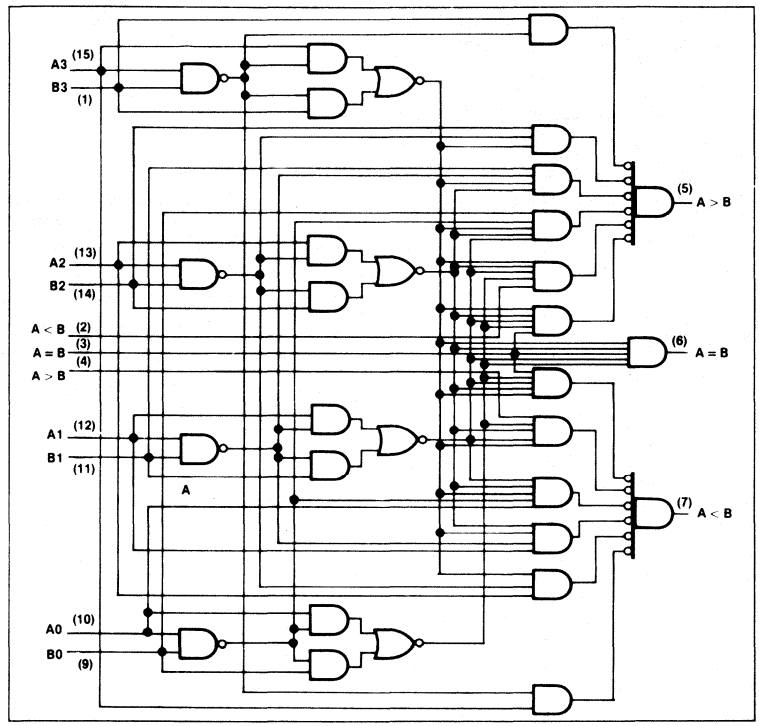
COMPARATOR FAST 54/74F85

Preliminary

The expansion inputs $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A > B, A = B and A < B outputs of the least significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$ = LOW, $I_{A=B}$ = HIGH, and $I_{A<B}$ = LOW.

The parallel expansion scheme shown in Figure A demonstrates the most efficient general use of these comparators. In the parallel expansion scheme, the expansion inputs can be used as a fifth input bit position except on the least significant device which must be connected as in the serial scheme. The expansion inputs are used by labeling $I_{A>B}$ as an "A" input, $I_{A<B}$ as a "B" input and setting $I_{A=B}$ LOW. The 'F85 can be used as a 5-bit comparator only when the outputs are used to drive the (A_0-A_3) and (B_0-B_3) inputs of another 'F85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

LOGIC DIAGRAM



FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A>B	A<B	A=B
$A_3 > B_3$	X	X	X	X	X	X	H	L	L
$A_3 < B_3$	X	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	X	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	H	L	L	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

COMPARATOR

FAST 54/74F85

Preliminary

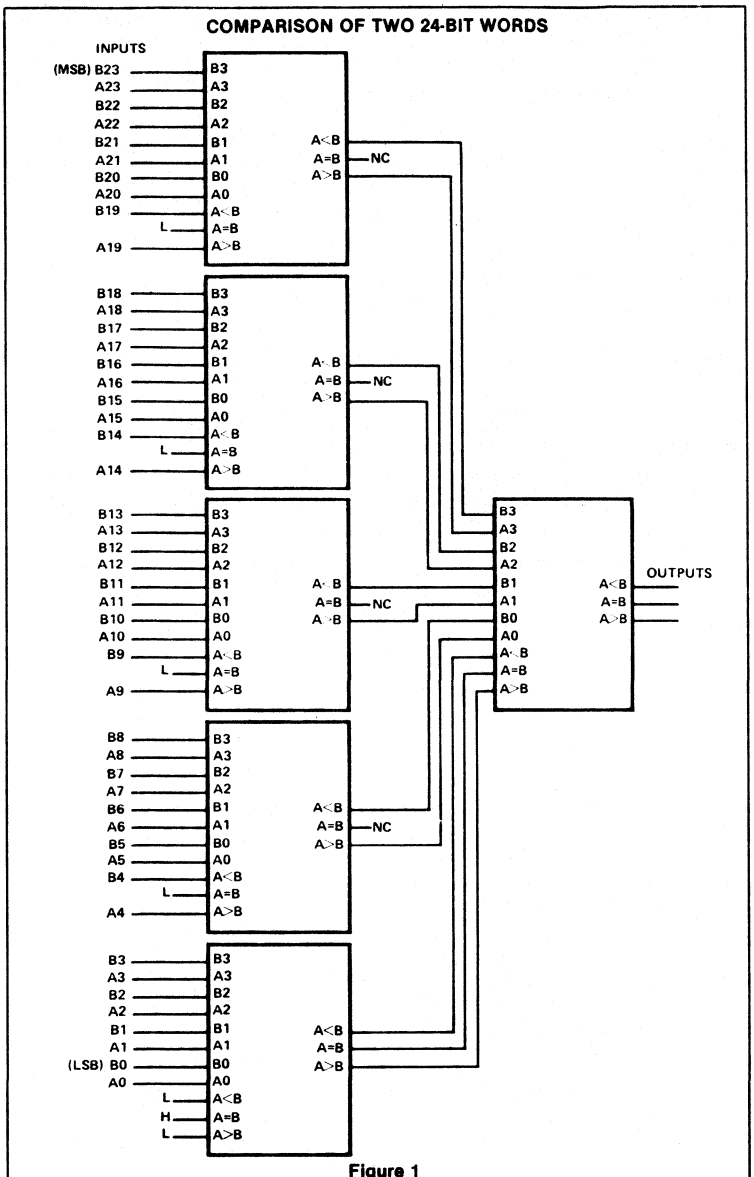


Figure 1

TABLE 1.

WORD LENGTH	NUMBER OF PACKAGES	TYPICAL SPEEDS 54/74F
1-4 Bits	1	12ns
5-25 Bits	2-6	22ns
25-120 Bits	8-31	34ns

5

COMPARATOR FAST 54/74F85

Preliminary

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperatuer range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F85			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−20	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−85	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			40	47	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open, A = B grounded, and all other inputs grounded.

COMPARATOR FAST 54/74F85

Preliminary

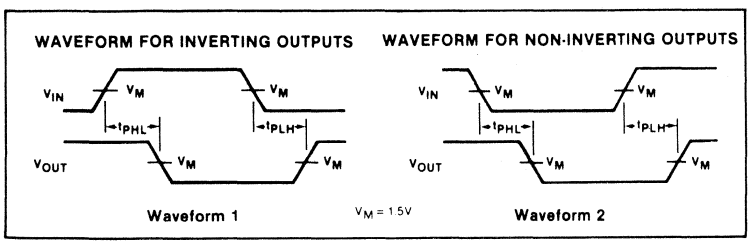
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F			54F		74F		UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B input to A < B, A> output	Waveform 1 3 logic levels						5 5	16 16	ns
t_{PLH} t_{PHL}	Propagation delay A or B input to A = B output	Waveform 2 4 logic levels						5 5	16 13	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A<B}$ and $I_{A=B}$ input to A > B output	Waveform 1 1 logic level						2 2	9 8	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A=B}$ input to A = B output	Waveform 2 2 logic levels						2 2	8 8	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A>B}$ and $I_{A=B}$ input to A < B output	Waveform 1 1 logic level						2 2	9 8	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

5

AC WAVEFORMS

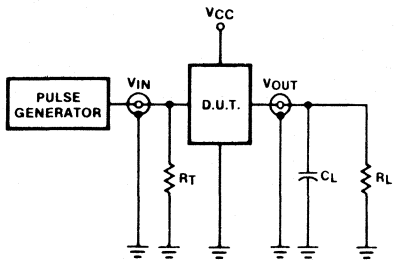


COMPARATOR FAST 54/74F85

Preliminary

TEST CIRCUITS AND WAVEFORMS

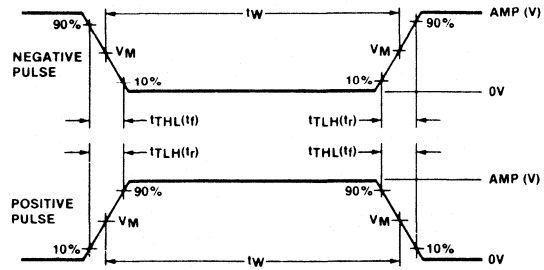
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Quad Two-Input Exclusive-OR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F86	4.3ns	16.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F86N	
Plastic SO	N74F86D	
Ceramic DIP		S54F86F
Ceramic LLCC		S54F86W

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

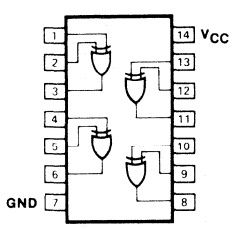
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A, B	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	50/33	1.0mA/20mA

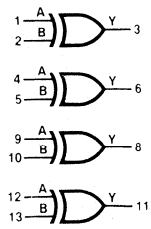
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

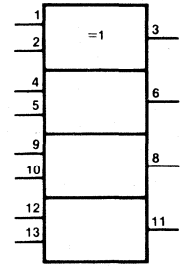
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F86			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		15	23	mA
			I_{CCL} Outputs LOW		18	28	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH}: V_{IN} = GND; I_{CCL}: V_{IN} = 4.5V.

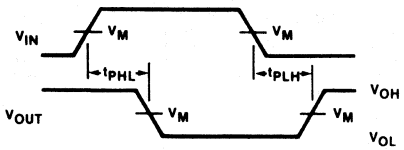
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Other input LOW	3.0	4.0	5.5	3.0	7.0	3.0	6.5	ns
t_{PHL}	A or B to output	Waveform 2	3.0	4.2	5.5	2.6	8.0	3.0	6.5	
t_{PLH}	Propagation delay	Other input HIGH	3.5	5.3	7.0	3.5	8.5	3.5	8.0	ns
t_{PHL}	A or B to output	Waveform 1	3.0	4.7	6.5	3.0	8.0	3.0	7.5	

NOTE
Subtract 0.2ns from minimum values for SO package.

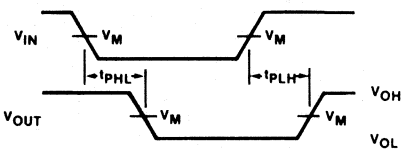
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS

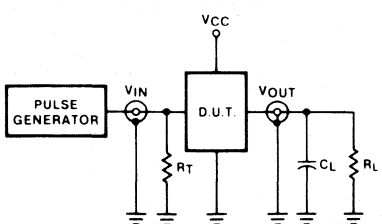


Waveform 2

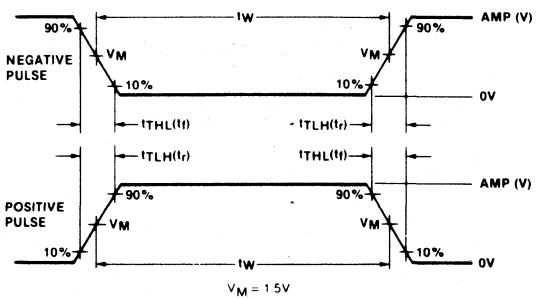
$V_M = 1.5V$

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



$V_M = 1.5V$

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop

DESCRIPTION

The 'F109 is a dual positive edge-triggered J$\overline{K}$-type flip-flop featuring individual J, $\overline{K}$, Clock, Set and Reset inputs; also complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-LOW inputs and operate independently of the Clock input.

The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the Mode Select-Truth Table. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition of the positive-going pulse.

The J and $\overline{K}$ inputs must be stable just one setup time prior to the LOW-to-HIGH transition of the Clock for predictable operation. The J$\overline{K}$ design allows operation as a D flip-flop by tying the J and $\overline{K}$ inputs together.

Although the Clock input is level sensitive, the positive transition of the Clock pulse between the 0.8V and 2.0V levels should be equal to or less than the Clock to output delay time for reliable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F109	125MHz	12.3mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F109N	
Plastic SO	N74F109D	
Ceramic DIP		S54F109F
Ceramic LLCC		S54F109G

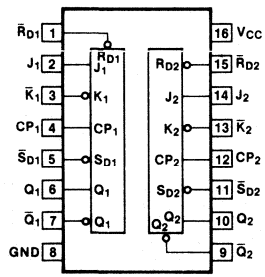
NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

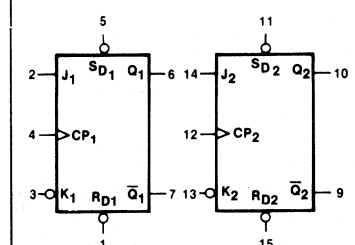
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
J_1, J_2, $\overline{K}_1$, $\overline{K}_2$	Data Inputs	1.0/1.0	20μA/0.6mA
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0	20μA/0.6mA
$\overline{R}_{D1}$, $\overline{R}_{D2}$	Reset Inputs (Active LOW)	1.0/3.0	20μA/1.8mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Set Inputs (Active LOW)	1.0/3.0	20μA/1.8mA
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

Note:
One (1.0) FAST unit load (U.L.) is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

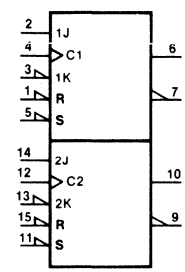
PIN CONFIGURATION



LOGIC SYMBOL

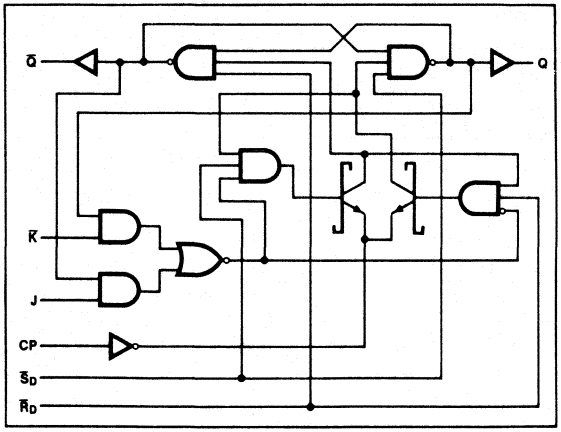


LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOP — FAST 54/74F109

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (Note)	L	L	X	X	X	H	H
Toggle	H	H	↓	h	l	$\overline{q}$	q
Load "0" (Reset)	H	H	↓	l	l	L	H
Load "1" (Set)	H	H	↓	h	h	H	L
Hold "no change"	H	H	↓	l	h	q	$\overline{q}$

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition.
l = LOW voltage level one setup time prior to the LOW-to-HIGH Clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH Clock transition.
↓ = LOW-to-HIGH Clock transition.

NOTE
Both outputs will be HIGH if both $\overline{S}_D$ and $\overline{R}_D$ go LOW simultaneously.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F109 Min	54/74F109 Typ[2]	54/74F109 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OH} = MAX, V_{IL} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			− 0.73	− 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V	J, $\overline{K}$, CP inputs		1	20	μA
			$\overline{S}_D$, $\overline{R}_D$ Inputs		1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	J, $\overline{K}$, CP inputs		− 0.4	− 0.6	mA
			$\overline{S}_D$, $\overline{R}_D$ Inputs		− 1.3	− 1.8	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		− 60	− 85	− 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			12.3	17	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs HIGH in turn.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} = Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} = Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	90	125		80		90		MHz
t_{PLH}	Propagation delay Clock to output	Waveform 1	3.8	5.3	7.0	3.8	9.0	3.8	8.0	ns
t_{PHL}			4.4	6.2	8.0	4.4	10.5	4.4	9.2	
t_{PLH}	Propagation delay Set or Reset to output	Waveform 2	3.2	5.2	7.0	2.8	9.0	3.2	8.0	ns
t_{PHL}			3.5	7.0	9.0	3.5	11.5	3.5	10.5	

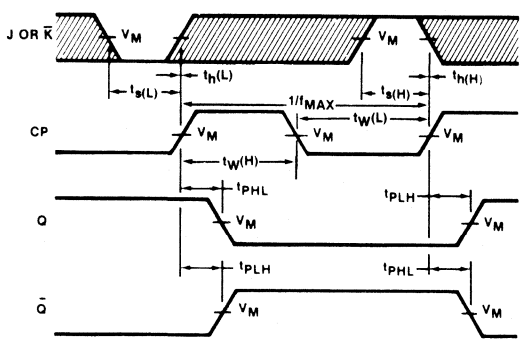
NOTE
Subtract 0.2ns from minimum values for SO package.

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			54F T_A, V_{CC} = Mil, $C_L = 50pF$, $R_L = 500\Omega$		74F T_A, V_{CC} = Com'l, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_s (H) t_s (L)	Setup time HIGH or LOW, J or $\overline{K}$ to Clock	Waveform 1	3.0 3.0			3.0 3.0		3.0 3.0		ns
t_h (H) t_h (L)	Hold time, HIGH or LOW, J or $\overline{K}$ to clock	Waveform 1	1.0 1.0			1.0 1.0		1.0 1.0		ns
t_w (H) t_w (L)	Clock pulse width, HIGH or LOW	Waveform 1	4.0 5.0			4.0 5.0		4.0 5.0		ns
t_w (L)	Set or Reset pulse width, LOW	Waveform 2	4.0			4.0		4.0		ns
t_{rec}	Recovery time, Set or Reset to Clock	Waveform 3	2.0			2.0		2.0		ns

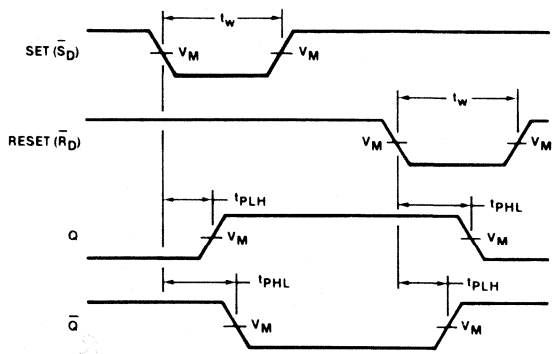
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, DATA SETUP AND HOLD TIMES, CLOCK PULSE WIDTH



Waveform 1

SET AND RESET TO OUTPUT DELAYS, SET AND RESET PULSE WIDTHS

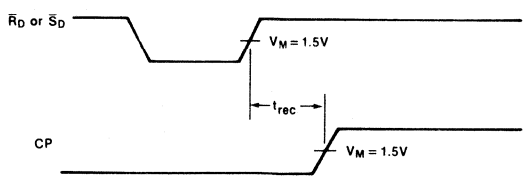


Waveform 2

$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

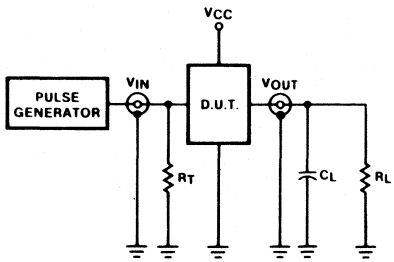
RECOVERY TIME



Waveform 3

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



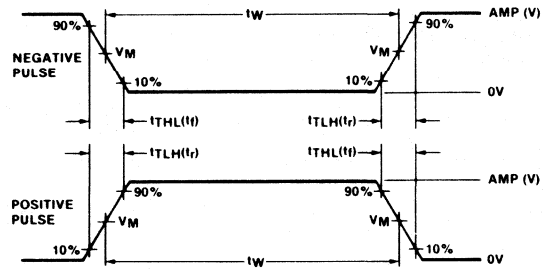
DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FLIP-FLOP

FAST 54/74F112

Preview

Dual J-K Negative Edge-Triggered Flip-Flop

DESCRIPTION

The 'F112 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Clock, Set and Reset inputs. The Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, when LOW, set or reset the outputs as shown in the Function Table regardless of the levels at the other inputs.

A HIGH level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is HIGH and the flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F112		15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74F112N	
Plastic SO	N74F112D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

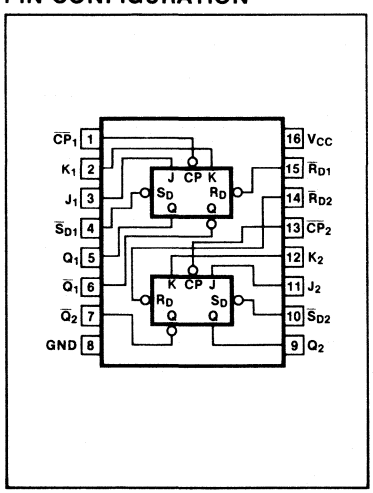
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
J_1, J_2, K_1, K_2	Data Inputs	1.0/1.0	20μA/0.6mA
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	1.0/4.0	20μA/2.4mA
$\overline{R}_{D1}$, $\overline{R}_{D2}$	Reset Input (Active LOW)	1.0/5	20μA/3.0mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Input (Active LOW)	1.0/5	20μA/3.0mA
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

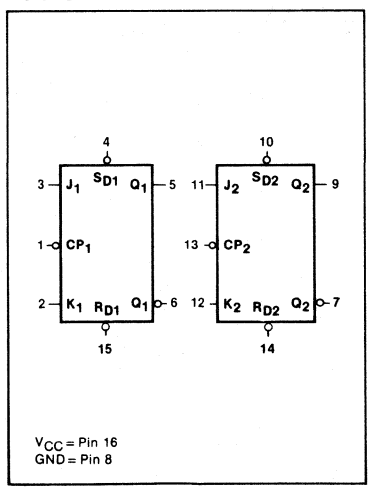
NOTE
One (1.0) FAST unit load is defined as 20μA in the HIGH state and 0.6mA in the LOW state.

5

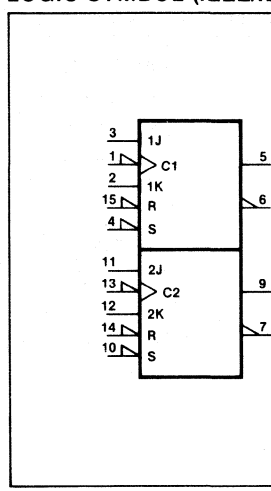
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

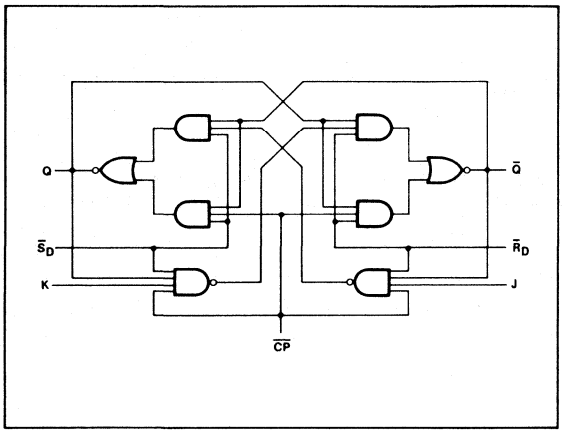


FLIP-FLOP

FAST 54/74F112

Preview

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Clock transition.
X = Don't care.
↓ = HIGH-to-LOW Clock transition.

NOTE
Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{R}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go HIGH simultaneously.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1.0	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

FLIP-FLOP

FAST 54/74F112

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F112			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 7.0V	J, K Inputs			100	μA
				$\overline{R}_D$, $\overline{S}_D$ Inputs			100	μA
				$\overline{CP}$ Inputs			100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.7V	J, K Inputs			20	μA
				$\overline{R}_D$, $\overline{S}_D$ Inputs			20	μA
				$\overline{CP}$ Inputs			20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.5V	J, K Inputs			−0.6	mA
				$\overline{R}_D$, $\overline{S}_D$ Inputs			−3.0	mA
				$\overline{CP}$ Inputs			−2.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				12	19	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs HIGH in turn.

5

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F			54F		74F		UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A, V_{CC} = Mil, C_L = 50pF, R_L = 500Ω		T_A, V_{CC} = Com'l, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	100							MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1	3.3 3.3		7.7 7.7					ns
t_{PLH} t_{PHL}	Propagation delay S_D or R_D to output	Waveform 2	3.0 3.3		7.0 7.7					ns

NOTE
Subtract 0.2ns from minimum values for SO package.

FLIP-FLOP

FAST 54/74F112

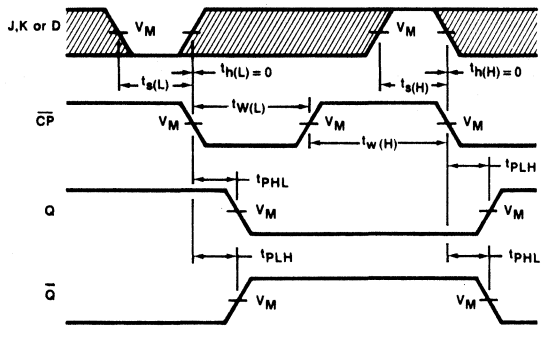
Preview

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			54F T_A, V_{CC} = Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} = Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_W(H)$	Clock pulse width (HIGH)	Waveform 1	5.0							ns
$t_W(L)$	Clock pulse width (LOW)	Waveform 1	5.0							ns
$t_W(L)$	Set or Reset pulse width (LOW)	Waveform 2	5.0							ns
t_s	Setup time J or K to Clock	Waveform 1	3.0							ns
t_h	Hold time J or K to Clock	Waveform 1	0.0							ns

AC WAVEFORMS

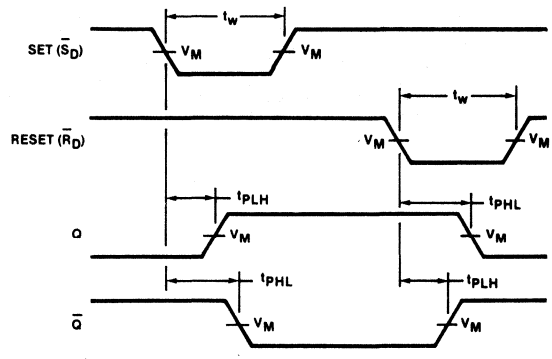
CLOCK TO OUTPUT DELAYS, DATA SETUP AND HOLD TIMES, CLOCK PULSE WIDTH



The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 1

SET AND RESET TO OUTPUT DELAYS, SET AND RESET PULSE WIDTHS



Waveform 2

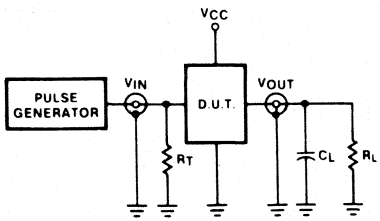
FLIP-FLOP

FAST 54/74F112

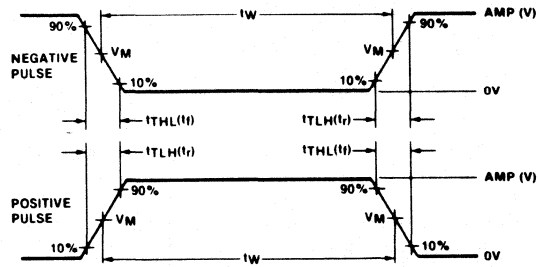
Preview

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



$V_M = 1.5V$

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

FLIP-FLOP

FAST 54/74F113

Preview

Dual J-K Negative Edge-Triggered Flip-Flop Without Reset

DESCRIPTION

The 'F113 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Set and Clock inputs. The asynchronous Set ($\overline{S}_D$) input, when LOW, forces the outputs to the steady state levels as shown in the Function Table regardless of the levels at the other inputs.

A HIGH level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is HIGH and the flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F113		12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F113N	
Plastic SO	N74F113D	
Ceramic DIP		
Ceramic LLCC		

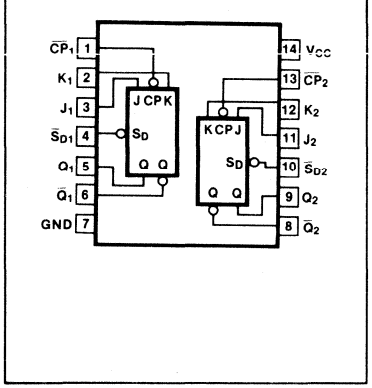
NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

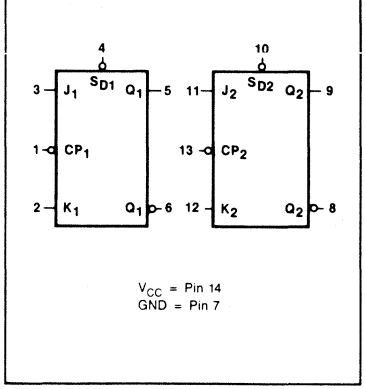
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
J_1, J_2, K_1, K_2	Data Inputs	1.0/1.0	20μA/0.6mA
$\overline{CP}_1$, $\overline{CP}_2$	Clock pulse inputs (active falling edge)	1.0/4.0	20μA/2.4mA
$\overline{S}_{D2}$, $\overline{S}_{D2}$	Direct set inputs (active low)	1.0/5	20μA/3.0mA
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as 20μA in the HIGH state and 0.6mA in the LOW state.

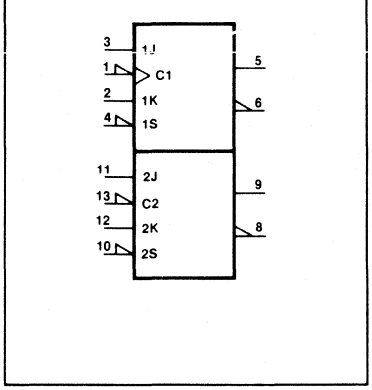
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

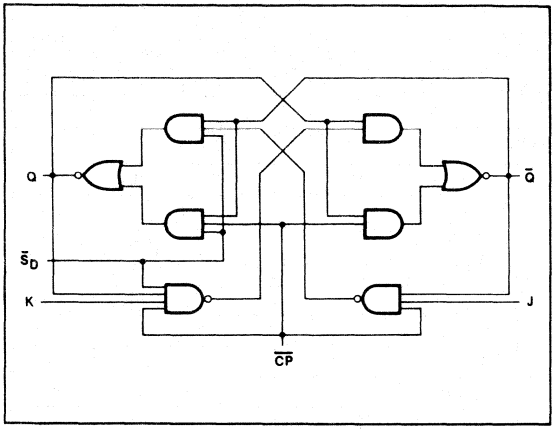


FLIP-FLOP

FAST 54/74F113

Preview

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	X	X	X	H	L
Toggle	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	↓	l	h	L	H
Load "1" (Set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Clock transition.
X = Don't care.
↓ = HIGH-to-LOW Clock transition.

Asynchronous Input:
LOW input to $\overline{S}_D$ sets Q to HIGH level
Set is independent of clock

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

5

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

FLIP-FLOP

FAST 54/74F113

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F113			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OH} = MAX, V_{IL} = MAX		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				− 0.73	− 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 7.0V	J, K Inputs			100	μA
				$\overline{S}_D$ Inputs			100	μA
				$\overline{CP}$ Inputs			100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.7V	J, K Inputs			20	μA
				$\overline{S}_D$ Inputs			20	μA
				$\overline{CP}$ Inputs			20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.5V	J, K Inputs			− 0.6	mA
				$\overline{S}_D$ Inputs			− 3.0	mA
				$\overline{CP}$ Inputs			− 2.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			− 60		− 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				12	19	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs HIGH in turn.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			54F T_A, V_{CC} Mil C_L = 50pF R_L = 500Ω		74F T_A, V_{CC} Com'l C_L = 50pF R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	Waveform 1	100							MHz
t_{PLH}	Propagation Delay	Waveform 1	3.3		7.7					ns
t_{PHL}	Clock to Output		3.3		7.7					
t_{PLH}	Propagation Delay	Waveform 2	3.0		7.0					ns
t_{PHL}	Set to Output		3.3		7.7					

NOTE
Subtract 0.2ns from minimum values for SO package.

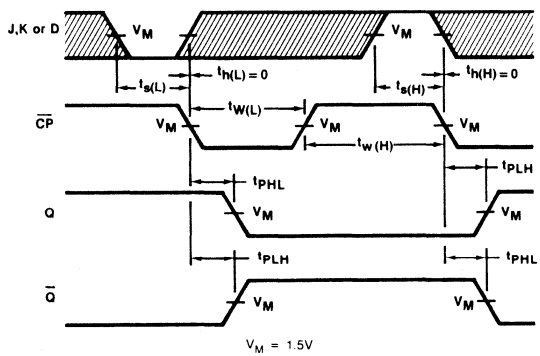
Preview

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_W(H)$	Clock pulse width (HIGH)	Waveform 1	5.0							ns
$t_W(L)$	Clock pulse width (LOW)	Waveform 1	5.0							ns
$t_W(L)$	Set pulse width (LOW)	Waveform 2	5.0							ns
t_s	Setup time J or K to clock	Waveform 1	3.0							ns
t_h	Hold time J or K to clock	Waveform 1	0.0							ns

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, DATA SETUP AND HOLD TIMES, CLOCK PULSE WIDTH

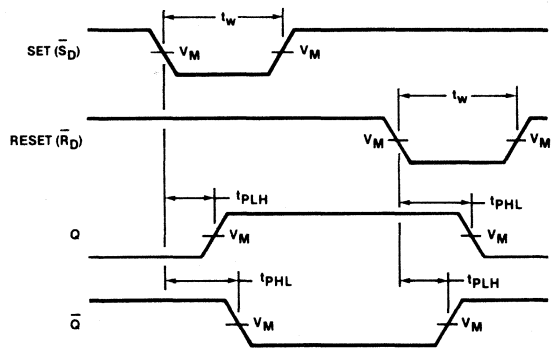


$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 1

SET AND RESET TO OUTPUT DELAYS, SET AND RESET PULSE WIDTHS



$V_M = 1.5V$

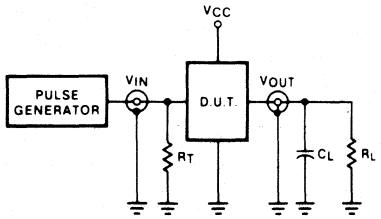
Waveform 2

5

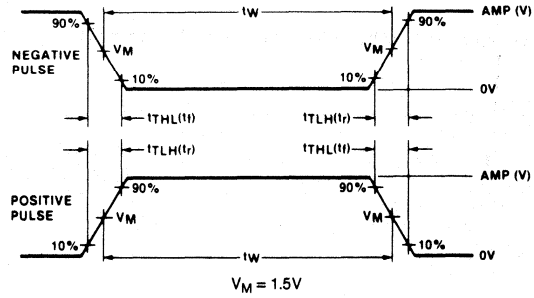
Preview

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



V_M = 1.5V

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FLIP-FLOP

FAST 54/74F114

Preview

Dual J-K Negative Edge-Triggered Flip-Flop (With Common Clock and Reset)

DESCRIPTION

The 'F114 is a Dual JK Negative Edge-Triggered Flip-Flop featuring individual J, K, and Set inputs and common Clock and Reset inputs. The Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, when LOW, set or reset the outputs as shown in the Truth Table regardless of the levels at the other inputs.

A HIGH level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is HIGH and the flip-flop will perform acording to the Truth Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F114		12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F114N	
Plastic SO	N74F114D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

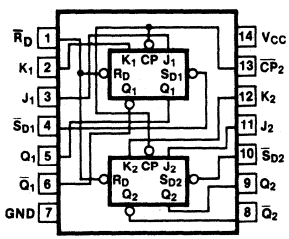
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
J_1, J_2, K_1, K_2	Data Inputs	1.0/1.0	20μA/0.6mA
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	1.0/4.0	20μA/2.4mA
$\overline{R}_D$	Direct Clear Input (Active LOW)	1.0/5.0	20μA/3.0mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	1.0/5.0	20μA/3.0mA
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

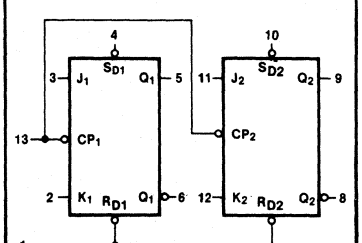
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

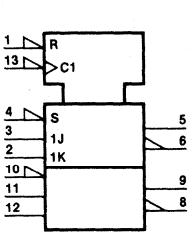
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

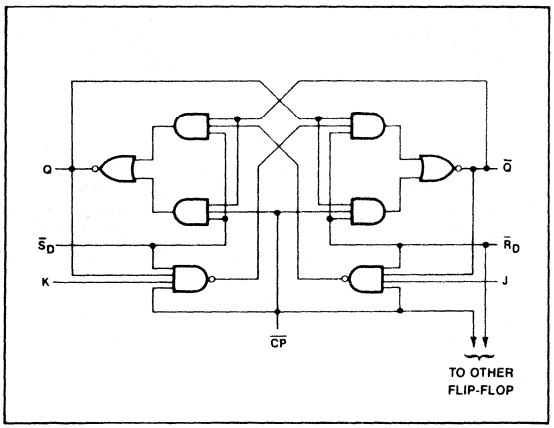


FLIP-FLOP

FAST 54/74F114

Preview

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Clock transition.
X = Don't care.

Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				+ 0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		+ 125	°C
		Com'l	0		70	°C

FLIP-FLOP — FAST 54/74F114

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]				54/74F114 Min	54/74F114 Typ[2]	54/74F114 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OH} = MAX, V_{IL} = MAX		Mil		2.5	3.4		V
				Com'l		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX					0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					− 0.73	− 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 7.0V	J, K Inputs				100	μA
				$\overline{R}_D$, $\overline{S}_D$ Inputs				100	μA
				$\overline{CP}$ Inputs				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.7V	J, K Inputs				20	μA
				$\overline{R}_D$, $\overline{S}_D$ Inputs				20	μA
				$\overline{CP}$ Inputs				20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.5V	J, K Inputs				− 0.6	mA
				$\overline{R}_D$, $\overline{S}_D$ Inputs				− 3.0	mA
				$\overline{CP}$ Inputs				− 2.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX				− 60		− 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX					12	19	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs HIGH in turn.

5

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω Min	Typ	Max	54F T_A, V_{CC} Mil C_L = 50pF R_L = 500Ω Min	Max	74F T_A, V_{CC} Com'l C_L = 50pF R_L = 500Ω Min	Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	100							MHz
t_{PLH}	Propagation delay	Waveform 1	3.3		7.7					ns
t_{PHL}	Clock to Output		3.3		7.7					
t_{PLH}	Propagation delay	Waveform 2	3.0		7.0					ns
t_{PHL}	S_D or R_D to Output		3.3		7.7					

NOTE
Subtract 0.2ns from minimum values for SO package.

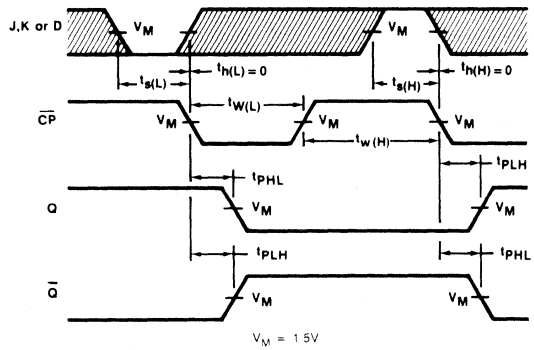
Preview

AC SETUP REQUIREMENTS

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
$t_W(H)$ Clock pulse width (HIGH)	Waveform 1	5.0							ns
$t_W(L)$ Clock pulse width (LOW)	Waveform 1	5.0							ns
$t_W(L)$ Set or Reset pulse width (LOW)	Waveform 2	5.0							ns
t_s Setup time J or K to Clock	Waveform 1	3.0							ns
t_h Hold time J or K to Clock	Waveform 1	0.0							ns

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, DATA SETUP AND HOLD TIMES, CLOCK PULSE WIDTH

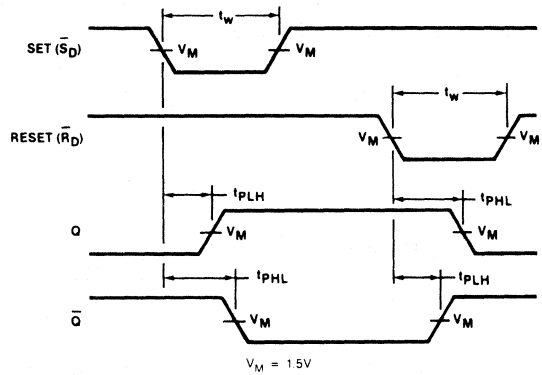


$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 1

SET AND RESET TO OUTPUT DELAYS, SET AND RESET PULSE WIDTHS



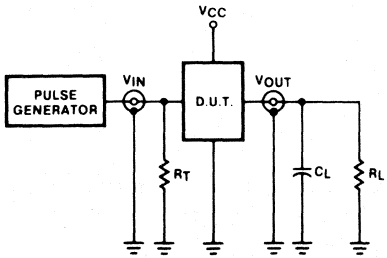
$V_M = 1.5V$

Waveform 2

Preview

TEST CIRCUITS AND WAVEFORMS

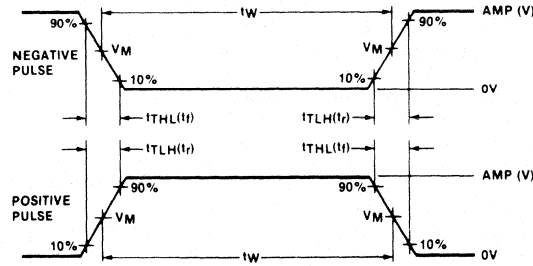
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

SCHMITT TRIGGER — FAST 54/74F132

Quad 2-Input NAND Schmitt Trigger

DESCRIPTION

The 'F132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than V_{T+MAX}, the gate will respond in the transitions of the other input as shown in Waveform 1.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F132	6.3ns	13mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74F132N	
Plastic SO	N74F132D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

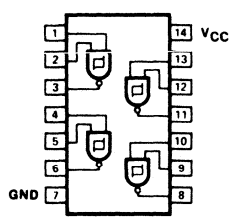
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

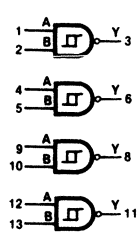
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A, B	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

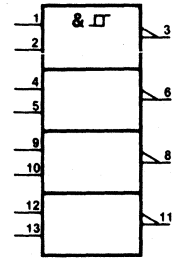
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



SCHMITT TRIGGER — FAST 54/74F132

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

	PARAMETER	TEST CONDITIONS[1]		54/74F132			UNIT
				Min	Typ[2]	Max	
V_{T+}	Positive-going threshold	V_{CC} = 5.0V		1.5	1.7	2.0	V
V_{T-}	Negative-going threshold	V_{CC} = 5.0V		0.5	0.9	1.1	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5.0V		0.4	0.8		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_T, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, $V_{T+\,MAX}$, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			− 0.73	− 1.2	V
I_{T+}	Input current at positive-going threshold	V_{CC} = 5.0V, V_I = V_{T+}			0.0		μA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5.0V, V_I = V_{T-}			− 350		μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			− 0.4	− 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		− 60	− 120	− 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		8.5	12	mA
			I_{CCL} Outputs LOW		13.0	19.5	mA

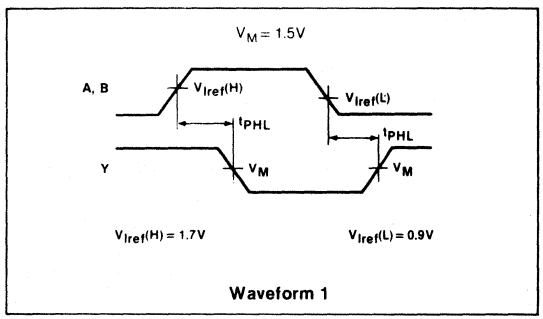
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH}, V_{IN} = GND; I_{CCL}, V_{IN} = 4.5V.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL}	Waveform 1	4.0 5.5	5.5 7.0	7.0 8.5	3 5.5	13 13.5	3.5 5	8.5 8.5	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

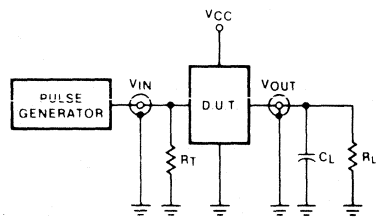
AC WAVEFORM



Waveform 1

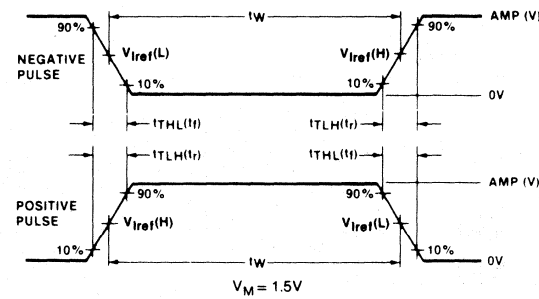
TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DECODER/DEMULTIPLEXER — FAST 54/74F138

1-Of-8 Decoder/Demultiplexer

- **Demultiplexing capability**
- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**
- **High speed replacement for Intel 3205**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F138	5.8ns	13mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F138N	
Plastic SO	N74F138D	
Ceramic DIP		S54F138F
Ceramic LLCC		S54F138G

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F138 decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled, provides eight mutually exclusive, active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The device features three Enable inputs; two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 'F138's and one inverter.

The device can be used as an eight output demultiplexer by using one of the active LOW Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active HIGH or active LOW state.

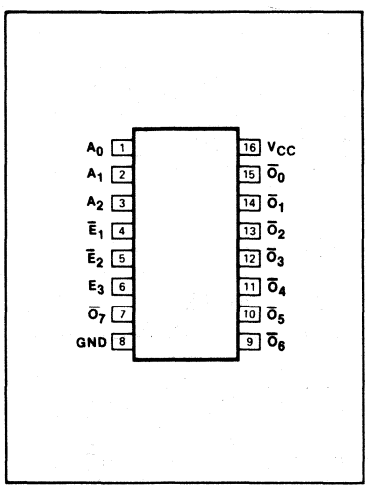
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A_0-A_2	Address Inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_1$-$\overline{E}_2$	Enable Inputs (Active LOW)	1.0/1.0	20μA/0.6mA
E_3	Enable Input (Active HIGH)	1.0/1.0	20μA/0.6mA
$\overline{O}_0$-$\overline{O}_7$	Outputs (Active LOW)	50/33	1.0mA/20mA

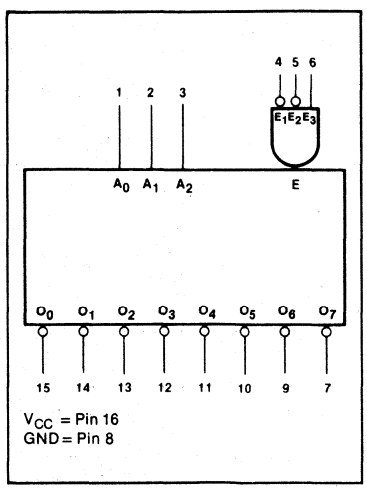
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

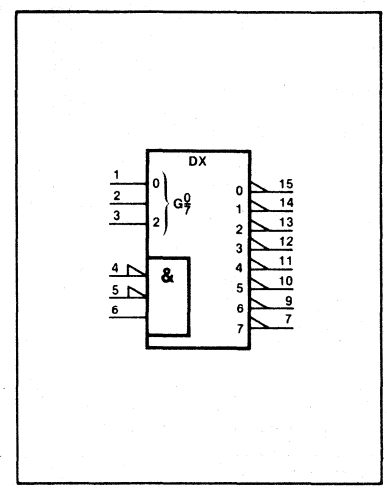
PIN CONFIGURATION



LOGIC SYMBOL

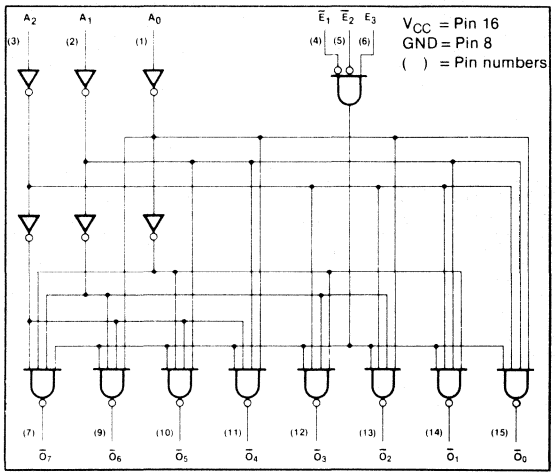


LOGIC SYMBOL (IEEE/IEC)



DECODER/DEMULTIPLEXER FAST 54/74F138

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

NOTES
H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

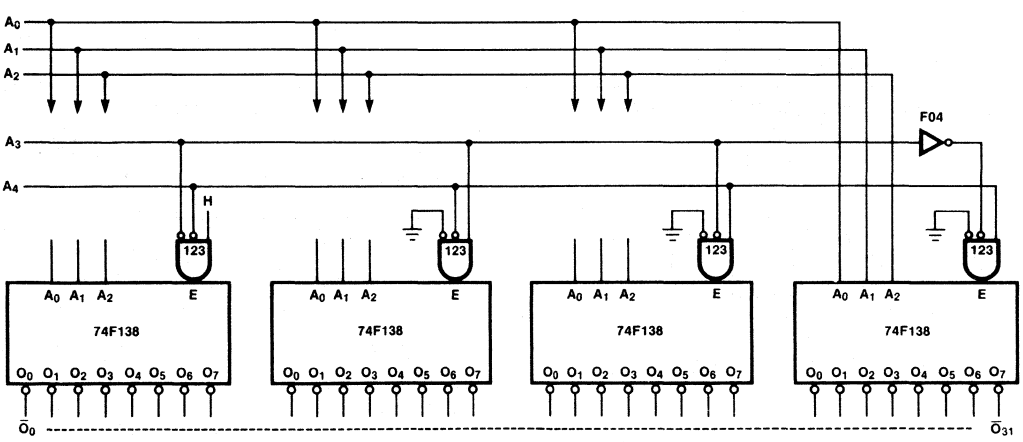
PARAMETER		TEST CONDITIONS[1]		54/74F138 Min	54/74F138 Typ[2]	54/74F138 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			– 0.73	– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			– 0.4	– 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		– 60	– 90	– 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		13	20	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. To measure I_{CC}, outputs must be open, V_{IN} on all inputs = 4.5V.

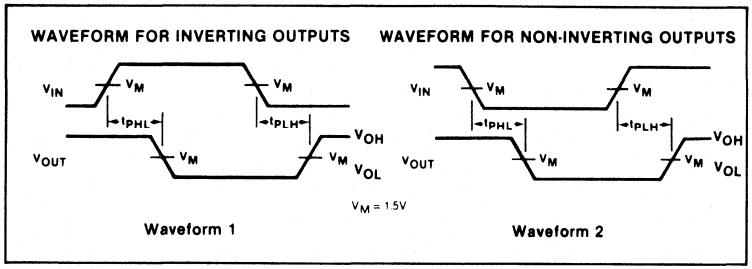
APPLICATION

5

EXPANSION TO 1-OF-32 DECODING



AC WAVEFORMS



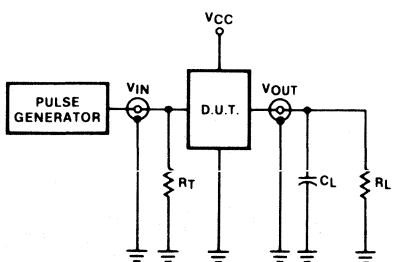
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} Address to output	Waveforms 1 and 2	3.5 4.0	5.6 6.1	7.0 8.0	2.9 3.5	12.0 9.5	3.5 4.0	8.0 9.0	ns
t_{PLH} Propagation delay t_{PHL} E_1 or E_2 to output	Waveform 2	3.5 3.0	5.4 5.3	7.0 7.0	3.0 3.0	11.0 8.0	3.5 3.0	8.0 7.5	ns
t_{PLH} Propagation delay t_{PHL} E_3 to output	Waveform 1	4.0 3.5	6.2 5.6	8.0 7.5	4.0 3.5	12.5 8.5	4.0 3.5	9.0 8.5	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

TEST CIRCUITS AND WAVEFORMS

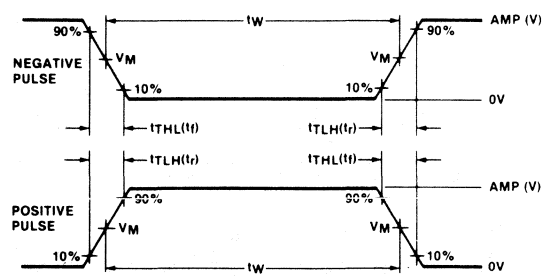
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



VM = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DECODER/DEMULTIPLEXER — FAST 54/74F139

Dual 1-of-4 Decoder/Demultiplexer

- **Demultiplexing capability**
- **Two independent 1-of-4 decoders**
- **Multifunction capability**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F139	5.3ns	13mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F139N	
Plastic SO	N74F139D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F139 is a high-speed, dual 1-of-4 decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (A_0, A_1) and providing four mutually exclusive active LOW outputs ($\overline{0}$–$\overline{3}$). Each decoder has an active LOW Enable ($\overline{E}$). When $\overline{E}$ is HIGH, every output is forced HIGH. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

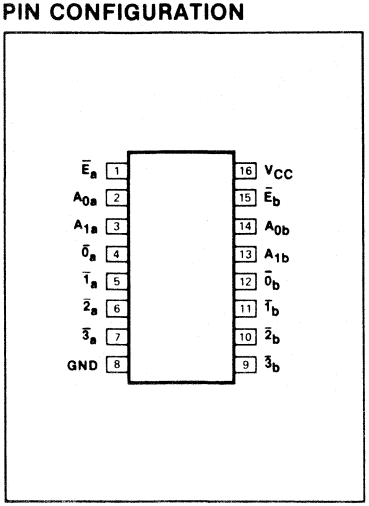
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
All	Inputs	1.0/1.0	20μA/0.6mA
$\overline{0}_a$-$\overline{3}_a$, $\overline{0}_b$-$\overline{3}_b$	Outputs	50/33	1.0mA/20mA

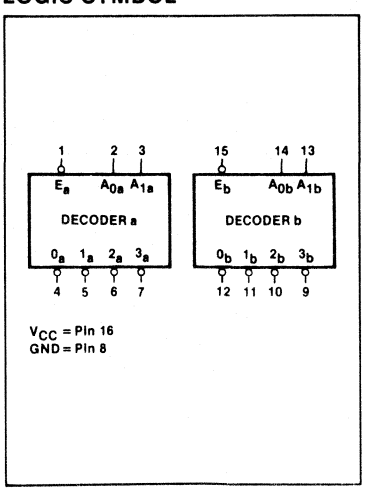
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

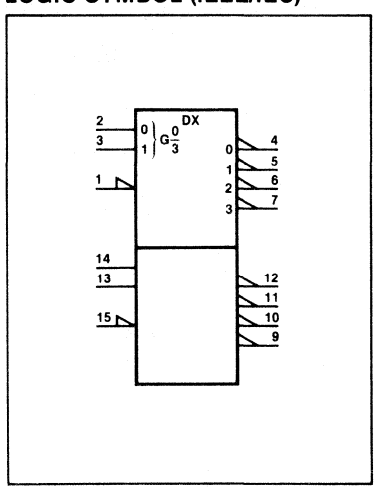
PIN CONFIGURATION



LOGIC SYMBOL

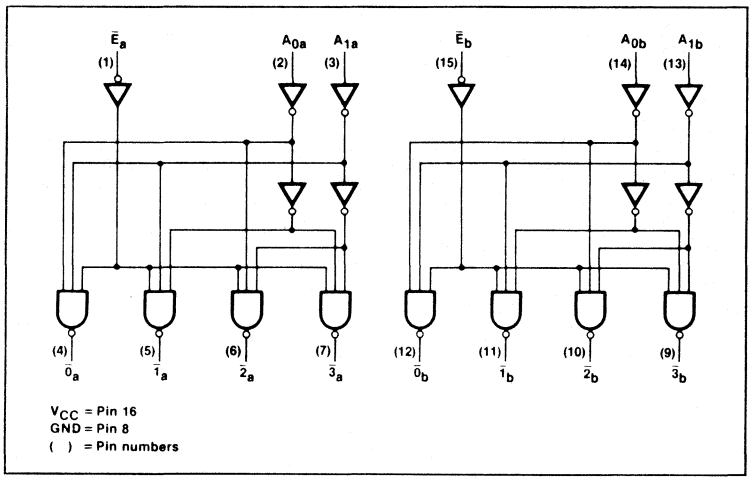


LOGIC SYMBOL (IEEE/IEC)



DECODER/DEMULTIPLEXER FAST 54/74F139

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

FUNCTION TABLE

INPUTS			OUTPUTS			
$\bar{E}$	A_0	A_1	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F139 Min	54/74F139 Typ[2]	54/74F139 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			− 0.73	− 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			− 0.4	− 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		− 60	− 90	− 150	mA
I_{CC}	Supply current (total)[4]	V_{CC} = MAX			13	20	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. To measure I_{CC}, outputs should be enabled and open.

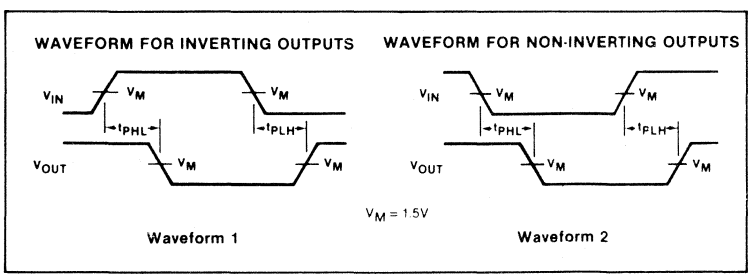
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

5

PARAMETER		TEST CONDITIONS	54/74F T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			54F T_A, V_{CC} Mil C_L = 50pF R_L = 500Ω		74F T_A, V_{CC} Com'l C_L = 50pF R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveforms 1 and 2	3.5	5.3	7.0	2.5	9.5	3.0	8.0	ns
t_{PHL}	A_0 or A_1 to $\overline{O}_n$		4.0	6.1	8.0	3.5	9.5	4.0	9.0	
t_{PLH}	Propagation delay	Waveform 2	3.5	5.4	7.0	3.0	9.0	3.5	8.0	ns
t_{PHL}	$\overline{E}_n$ to $\overline{O}_n$		3.0	4.7	6.5	2.5	8.0	3.0	7.5	

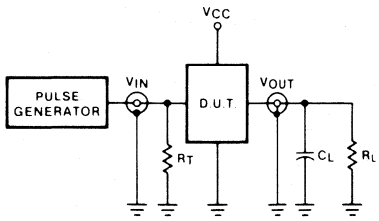
NOTE
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS

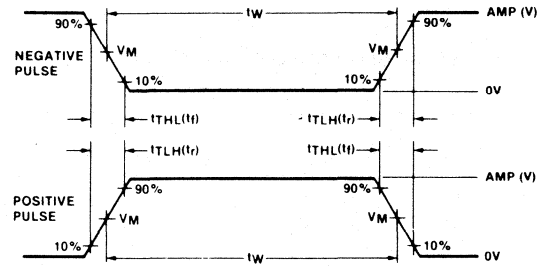
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

ENCODER — FAST 54/74F148

Preview

8-Input Priority Encoder

- Code conversions
- Multi-channel D/A converter
- Decimal-to-BCD converter
- Cascading for priority encoding of "N"bits
- Input Enable capability
- Priority encoding—automatic selection of highest priority input line
- Output Enable—active LOW when all inputs HIGH
- Group Signal output—active when any input is LOW

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F148		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F148N	
Plastic SO	N74F148D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{I}_0$-$\overline{I}_7$	Priority Inputs (Active LOW)	1.0/1.0	20μA/0.6mA
EI	Enable Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{EO}$	Enable Output (Active LOW)	50/33	1.0mA/20mA
$\overline{GS}$	Group Select Output (Active LOW)	50/33	1.0mA/20mA
$\overline{A}_0$-$\overline{A}_2$	Address Outputs (Active LOW)	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

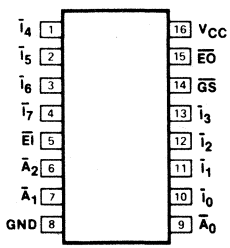
DESCRIPTION

The 'F148 8-input priority encoder accepts data from eight active-LOW inputs and provides a binary representation on the three active-LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\overline{I}_7$ having the highest priority.

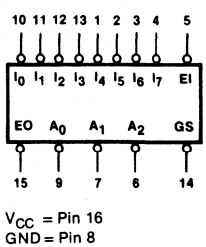
A HIGH on the Enable Input ($\overline{EI}$) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs.

A Group Signal ($\overline{GS}$) output and an Enable Output ($\overline{EO}$) are provided with the three data outputs. The $\overline{GS}$ is active-LOW when any input is LOW; this indicates when any input is active. The $\overline{EO}$ is active-LOW when all inputs are HIGH. Using the Enable Output along with the Enable Input allows priority encoding of N input signals. Both $\overline{EO}$ and $\overline{GS}$ are active-HIGH when the Enable Input is HIGH.

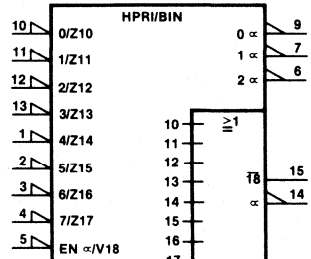
PIN CONFIGURATION



LOGIC SYMBOL



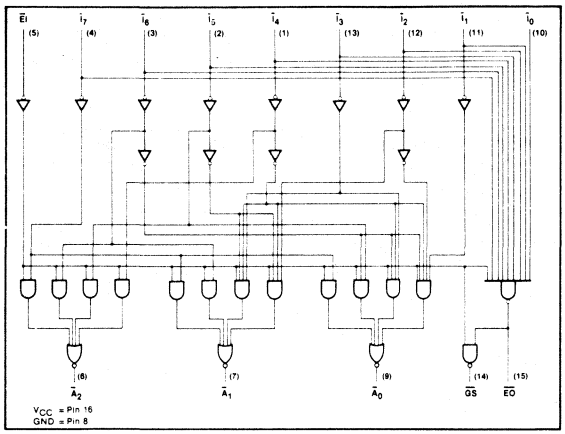
LOGIC SYMBOL (IEEE/IEC)



ENCODER FAST 54/74F148

Preview

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS									OUTPUTS				
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	$\overline{GS}$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F148			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			− 0.73	− 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			− 0.4	− 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		− 60	− 80	− 150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX				35	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

5

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F			54F		74F		UNIT
		T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} $\overline{I}_n$ input to $\overline{A}_n$ outputs	Waveform 2	3.5 4.0	7.0 8.0	9.0 10.5			3.5 4.0	10.0 12.0	ns
t_{PLH} Propagation delay t_{PHL} $\overline{I}_n$ input to $\overline{EO}$ output	Waveform 1	2.5 2.5	5.0 5.5	6.5 7.5			2.5 2.5	7.5 8.5	ns
t_{PLH} Propagation delay t_{PHL} $\overline{I}_n$ input to $\overline{GS}$ output	Waveform 2	3.0 3.0	7.0 7.0	10.5 10.5			3.0 2.0	10.0 9.0	ns
t_{PLH} Propagation delay t_{PHL} $\overline{EI}$ input to $\overline{A}_n$ outputs	Waveform 2	3.5 3.0	6.5 6.0	8.5 8.0			3.5 3.0	9.5 9.0	ns
t_{PLH} Propagation delay t_{PHL} $\overline{EI}$ input to $\overline{GS}$ output	Waveform 2	3.0 4.5	5.5 8.0	7.0 10.5			3.0 4.5	8.0 12.0	ns
t_{PLH} Propagation delay t_{PHL} $\overline{EI}$ input to $\overline{EO}$ output	Waveform 2	2.5 3.0	5.0 6.0	7.0 7.5			2.5 3.0	8.0 8.5	ns

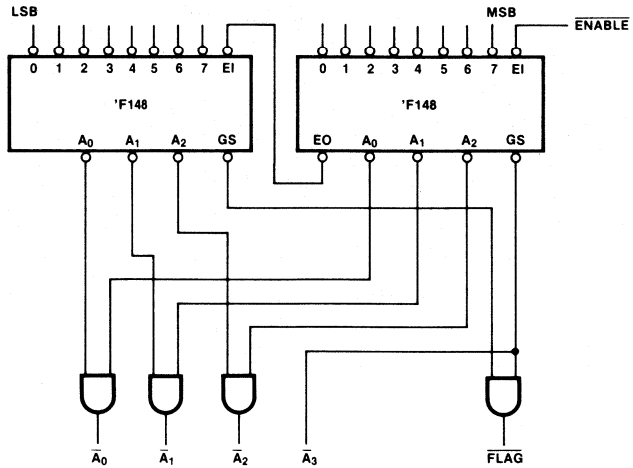
NOTE
Subtract 0.2ns from minimum values for SO package.

ENCODER FAST 54/74F148

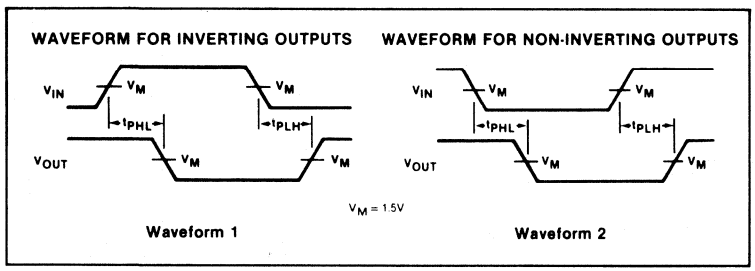
Preview

APPLICATION

16-INPUT PRIORITY ENCODER



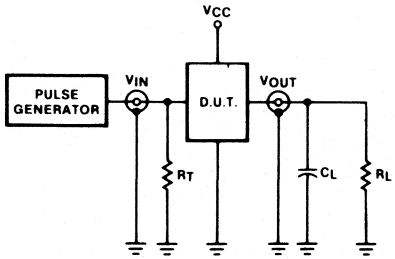
AC WAVEFORMS



Preview

TEST CIRCUITS AND WAVEFORMS

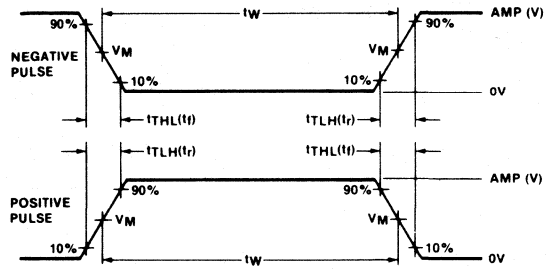
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

MULTIPLEXER

FAST 54/74F151

Preliminary

8-Input Multiplexer

- **Multifunction capability**
- **Complementary outputs**
- **See 'F251 for 3-state version**

TYPE	TYPICAL PROPAGATION DELAY (Enable to Y)	TYPICAL SUPPLY CURRENT (Total)
74F151		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to + 70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = − 55°C to + 125°C
Plastic DIP	N74F151N	
Plastic SO	N74F151D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F151 is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. True (Y) and Complement ($\overline{Y}$) outputs are both provided. The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, the $\overline{Y}$ output is HIGH and the Y output is LOW, regardless of all other inputs. The logic function provided at the output is:

$$Y = \overline{E} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

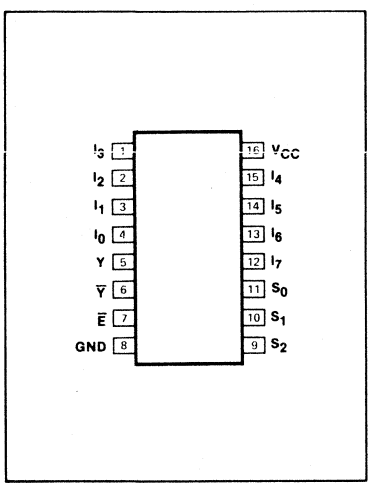
In one package the 'F151 provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and its negation with correct manipulation.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

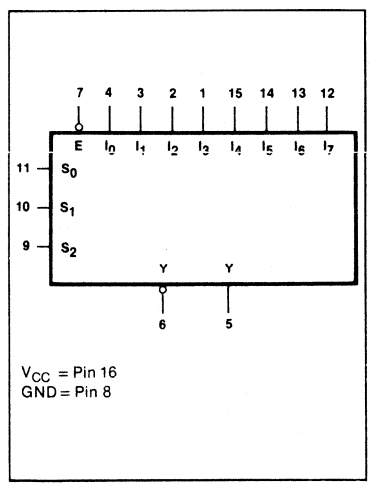
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
I_0-I_7	Data Inputs	1.0/1.0	20μA/0.6mA
S_0-S_2	Select Inputs	1.0/1.0	20μA/0.6mA
$\overline{E}$	Enable Input (Active Low)	1.0/1.0	20μA/0.6mA
Y, $\overline{Y}$	Data Output, Data Output Inverted	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

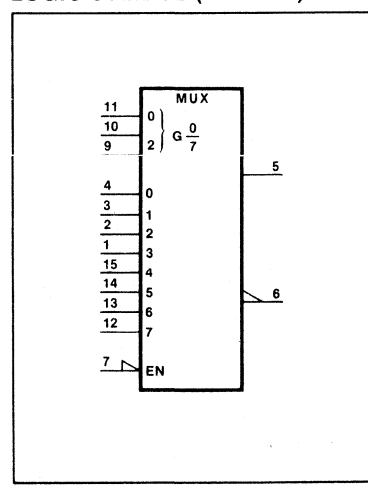
PIN CONFIGURATION



LOGIC SYMBOL



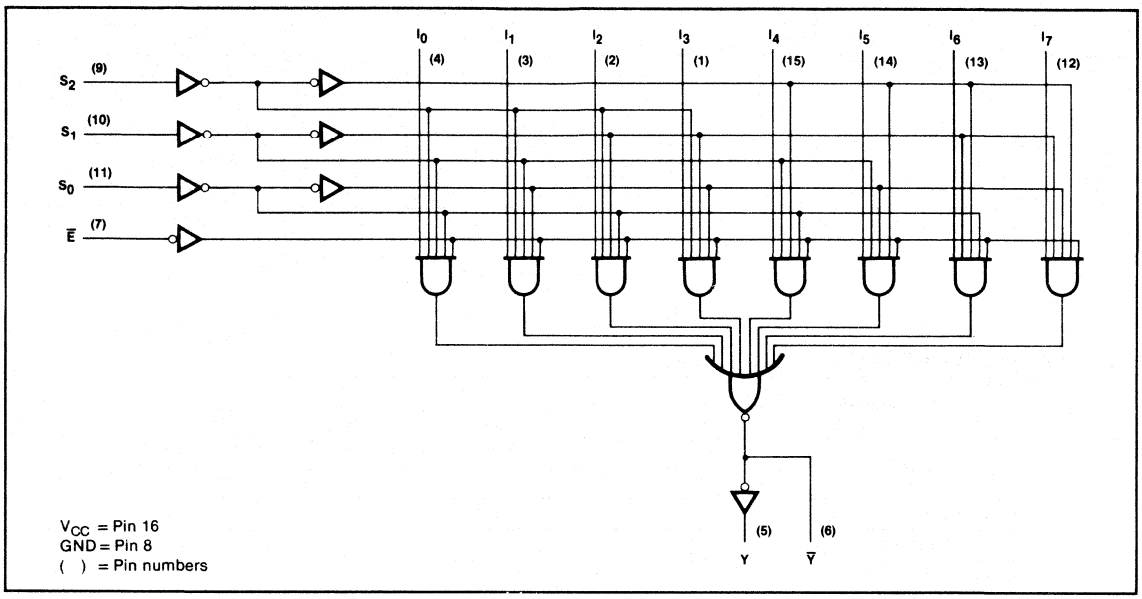
LOGIC SYMBOL (IEEE/IEC)



MULTIPLEXER FAST 54/74F151

Preliminary

LOGIC DIAGRAM



5

FUNCTION TABLE

INPUTS												OUTPUTS	
$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

MULTIPLEXER FAST 54/74F151

Preliminary

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			− 0.73	− 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			− 0.4	− 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		− 60	− 80	− 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				21	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with all inputs at 4.5V and outputs open.

MULTIPLEXER FAST 54/74F151

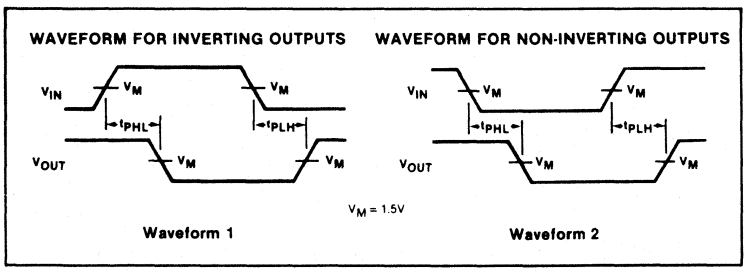
Preliminary

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

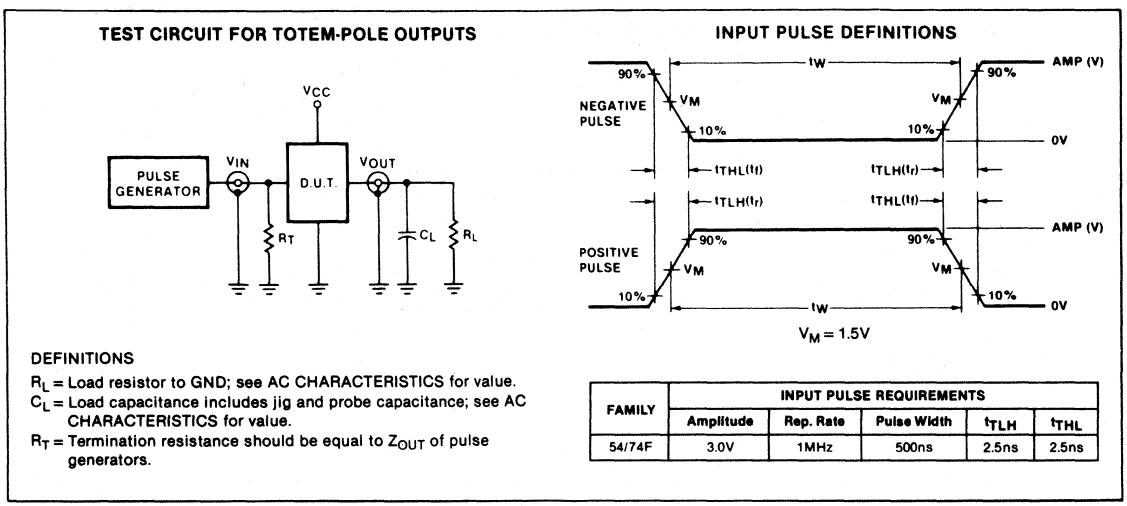
PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Select to Y output	Waveform 2	4.5 3.2		8.0 6.1					
t_{PLH} t_{PHL}	Propagation delay Select to $\overline{Y}$ output	Waveform 1	4.5 5.0		13 9.0					
t_{PLH} t_{PHL}	Propagation delay Enable to Y output	Waveform 1	3.4 4.5		6.1 8.5					
t_{PLH} t_{PHL}	Propagation delay Enable to $\overline{Y}$ output	Waveform 2	5.0 3.8		9.5 7.0					
t_{PLH} t_{PHL}	Propagation delay Data to Y output	Waveform 2	3.0 2.0		5.7 4.0					
t_{PLH} t_{PHL}	Propagation delay Data to $\overline{Y}$ output	Waveform 1	4.0 3.7		9.5 6.5					

NOTE
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

MULTIPLEXER

FAST 54/74F153

Preview

Dual 4-Line to 1-Line Multiplexer

- **Non-inverting outputs**
- **Separate Enable for each section**
- **Common Select inputs**
- **See 'F253 for 3-State version**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F153		

DESCRIPTION

The 'F153 is a dual 4-input multiplexer that can select 2 bits of data from up to four sources under control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. Outputs (Y_a, Y_b) are forced LOW when the corresponding Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH.

The device is the logical implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Y_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$Y_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0$$

The '153 can be used to move data to a common output bus from a group of registers. The state of the Select inputs would determine the particular register from which the data came. An alternative application is as a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F153N	
Plastic SO	N74F153D	
Ceramic DIP		S54F153F
Ceramic LLCC		S54F153G

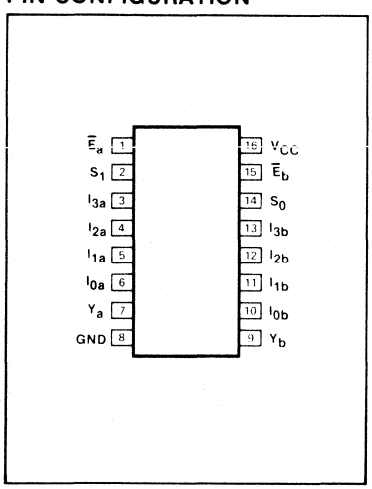
NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

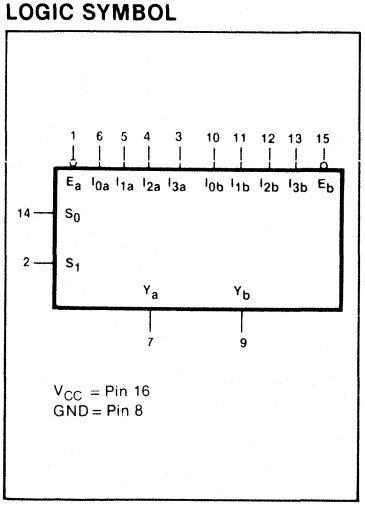
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
I_{0a}–I_{3a}	Side A data inputs	1.0/1.0	20μA/0.6mA
I_{0b}–I_{3b}	Side B data inputs	1.0/1.0	20μA/0.6mA
S_0, S_1	Common select inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_a$	Side A enable input (active low)	1.0/1.0	20μA/0.6mA
$\overline{E}_b$	Side B enable input (active low)	1.0/1.0	20μA/0.6mA
Y_a	Side A output	50/33	1.0mA/20mA
Y_b	Side B output	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

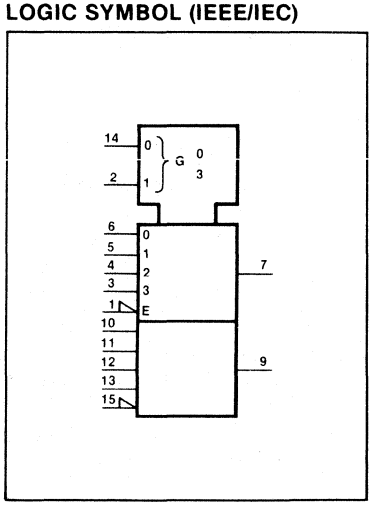
PIN CONFIGURATION



LOGIC SYMBOL



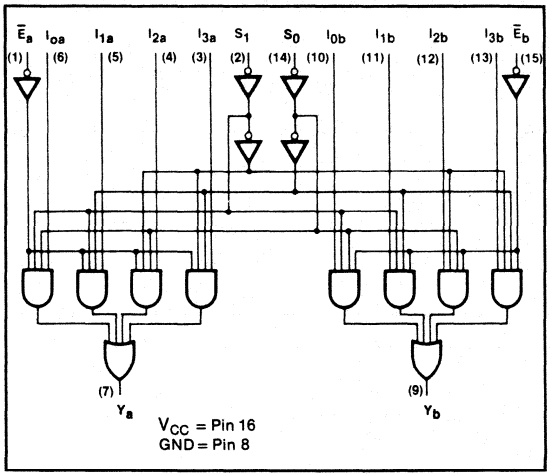
LOGIC SYMBOL (IEEE/IEC)



MULTIPLEXER FAST 54/74F153

Preview

LOGIC DIAGRAM



FUNCTION TABLE

SELECTS INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Y
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

5

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

MULTIPLEXER FAST 54/74F153

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F153 Min	54/74F153 Typ[2]	54/74F153 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			− 0.73	− 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			− 0.4	− 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		− 60	− 80	− 150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, V_{IN} = GND				20	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

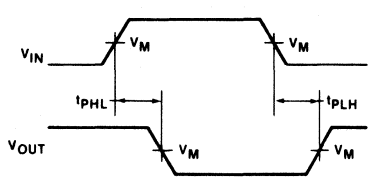
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 2	5.5 4.0	8.1 7.0	10.5 9.0	5.0 3.5	14 11	5.5 4.0	12 10.5	ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1	5.0 4.0	7.1 5.7	9.0 7.0	4.5 3.5	11.5 9.0	5.0 4.0	10.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2	4.0 3.0	5.3 5.1	7.0 6.5	3.5 2.5	9.0 8.0	4.0 3.0	8.0 7.5	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

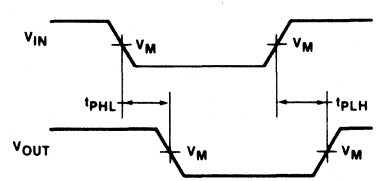
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 2

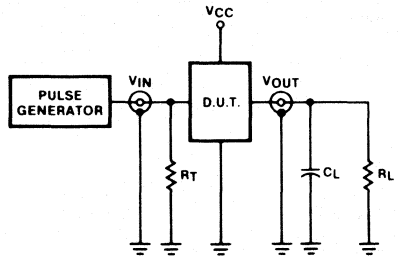
V_M = 1.5V

MULTIPLEXER FAST 54/74F153

Preview

TEST CIRCUITS AND WAVEFORMS

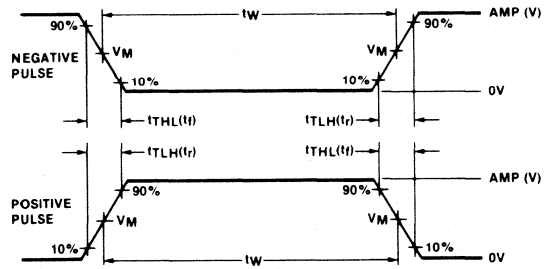
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

'157 Quad 2-Input Data Selector/Multiplexer (Non-Inverted)
'158 Quad 2-Input Data Selector/Multiplexer (Inverted)

DESCRIPTION

The 'F157 is a high-speed quad 2-input multiplexer which selects 4 bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Y) are forced LOW regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the 'F157. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. Logic equations for the outputs are shown below:

$$Y_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$Y_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Y_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$Y_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

The 'F158 is similar but has inverting outputs:

$$\overline{Y}_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$\overline{Y}_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$\overline{Y}_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$\overline{Y}_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F157	4.6ns	15mA
74F158	3.7ns	10mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F157N • N74F158N	
Plastic SO	N74F157D • N74F158D	
Ceramic DIP		S54F157F
Ceramic LLCC		S54F157G

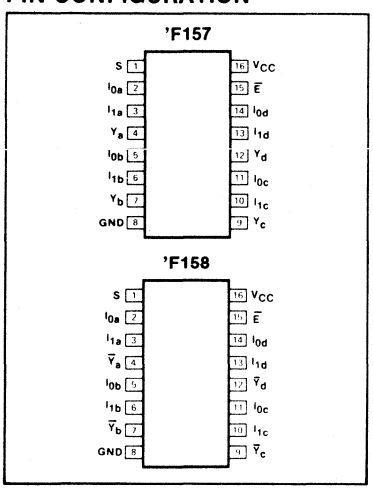
NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

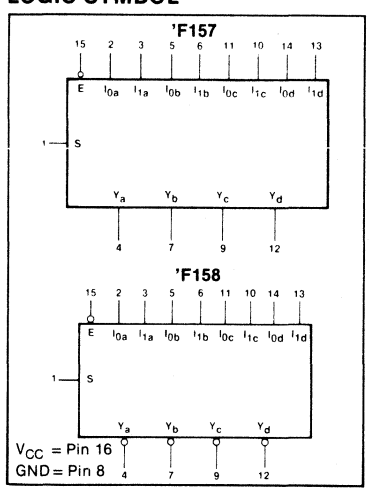
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
All	Inputs	1.0/1.0	20μA/0.6mA
Y_a-Y_d, $\overline{Y}_a$-$\overline{Y}_d$	Outputs	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

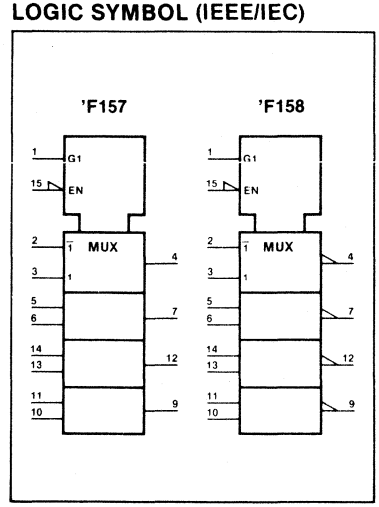
PIN CONFIGURATION



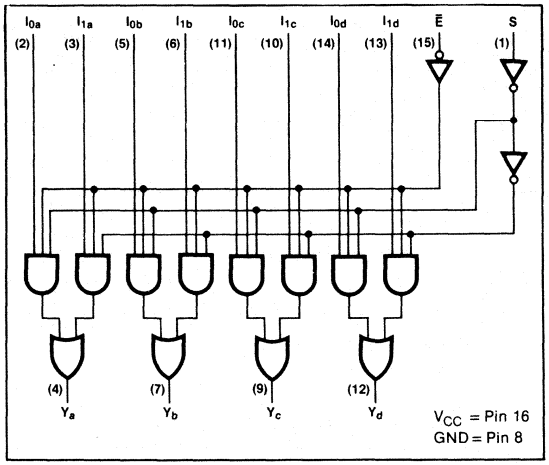
LOGIC SYMBOL



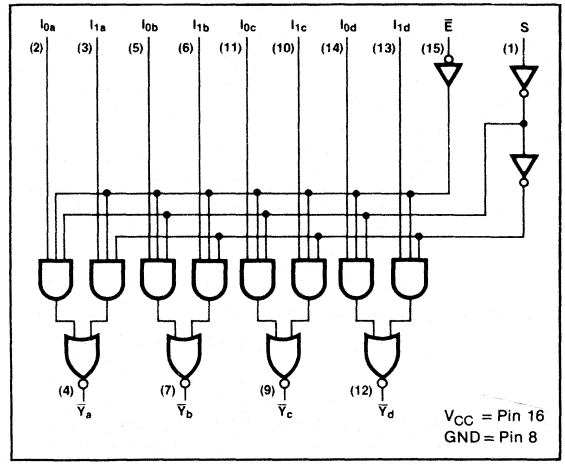
LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM, '157



LOGIC DIAGRAM, '158



FUNCTION TABLE, '157

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

FUNCTION TABLE, '158

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

5

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	– 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F157, 158			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			– 0.73	– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			– 0.4	– 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		– 60	– 80	– 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	'F157		15.0	23.0	mA
			'F158		10.0	15.0	mA

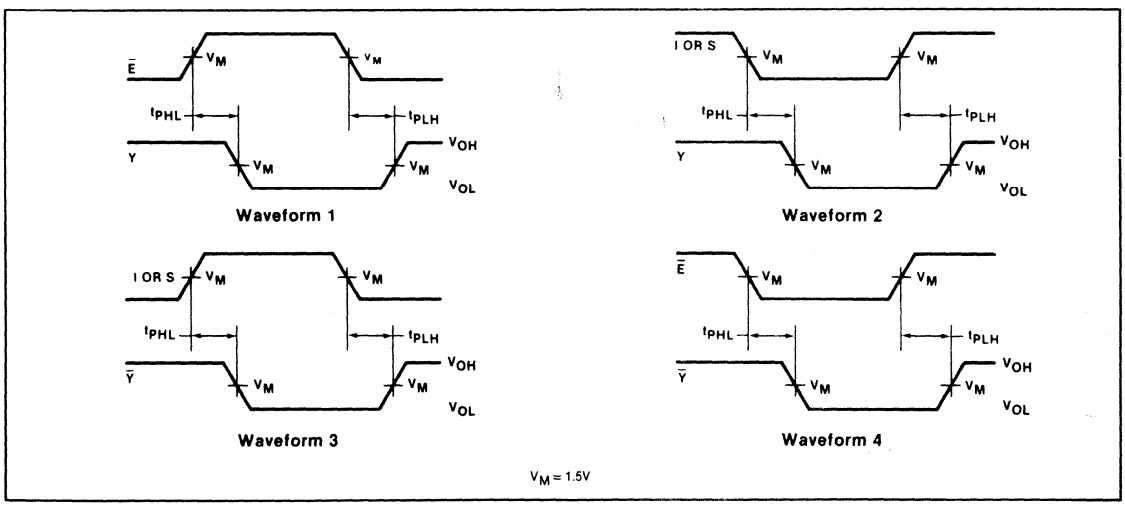
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} = Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} = Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} Data to output	Waveform2, 'F157	3.8 2.5	5.5 4.6	7.0 5.5	3.5 2.5	10.0 7.5	3.8 2.5	8.0 7.0	ns
t_{PLH} Propagation delay t_{PHL} Enable to output	Waveform 1, 'F157	5.0 3.8	7.6 5.3	10.0 7.0	5.0 3.8	15.0 8.5	5.0 3.8	11.5 8.0	ns
t_{PLH} Propagation delay t_{PHL} Select to output	Waveform 2, 'F157	4.5 3.5	10.1 6.3	13.0 8.0	3.5 3.5	17.0 11.5	4.5 3.5	15.0 9.0	ns
t_{PLH} Propagation delay t_{PHL} Data to output	Waveform 3, 'F158	3.0 2.0	4.4 3.3	5.9 4.5	2.5 2.0	8.5 6.0	3.0 2.0	7.0 5.5	ns
t_{PLH} Propagation delay t_{PHL} Enable to output	Waveform 4, 'F158	4.5 3.5	6.2 6.4	8.0 8.5	4.5 3.5	9.5 9.5	4.5 3.5	9.0 9.5	ns
t_{PLH} Propagation delay t_{PHL} Select to output	Waveform 3, 'F158	4.0 4.0	6.4 6.9	8.5 9.0	4.0 4.0	10.5 10.5	4.0 4.0	9.5 10.5	ns

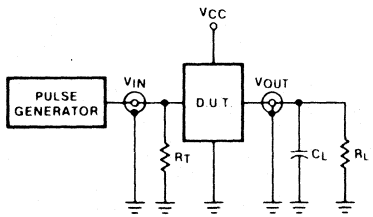
NOTE
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS

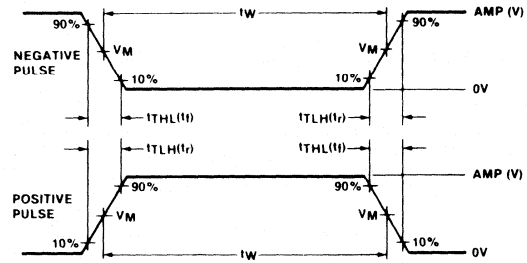


TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



$V_M = 1.5V$

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

COUNTERS FAST 54/74F160A, 54/74F161A, 54/74F162A, 54/74F163A

Preview

'F160A, 'F162A BCD Decade Counter
'F161A, 'F163A 4-Bit Binary Counter

- **Synchronous counting and loading**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Asynchronous reset ('F160A, 'F161A)**
- **Synchronous reset ('F162A, 'F163A)**
- **High-speed synchronous expansion**
- **Typical count rate of 125MHz**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F160A		
74F161A		
74F162A		
74F163A		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F160AN • N74F161AN N74F162AN • N74F163AN	
Plastic SO	N74F160AD • N74F161AD N74F162AD • N74F163AD	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

Synchronous presettable decade ('F160A, 'F162A) and 4-bit ('F161A, 'F163A) counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The Clock input is buffered.

The outputs of the counters may be preset to HIGH or LOW level. A LOW level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0-D_3 inputs to be loaded into the counter on the positive-going edge of the clock (providing that the setup and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

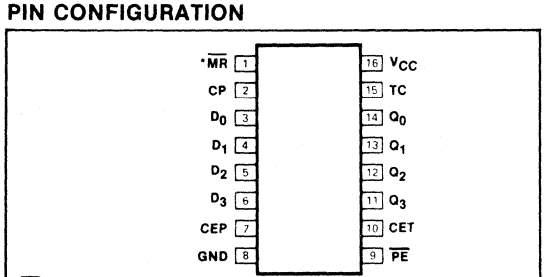
A LOW level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops (Q_0-Q_3) in 'F160A and 'F161A to LOW levels, regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
CEP	Count Enable Parallel Input	1.0/1.0	20μA/0.6mA
CET	Count Enable Trickle Input	1.0/2.0	20μA/1.2mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{SR}$	Synchronous Reset Input (Active LOW)	1.0/2.0	20μA/1.2mA
D_0-D_3	Parallel Data Inputs	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/2.0	20μA/1.2mA
Q_0-Q_3	Flip-Flop Outputs	50/33	1.0mA/20mA
TC	Terminal Count Output	50/33	1.0mA/20mA

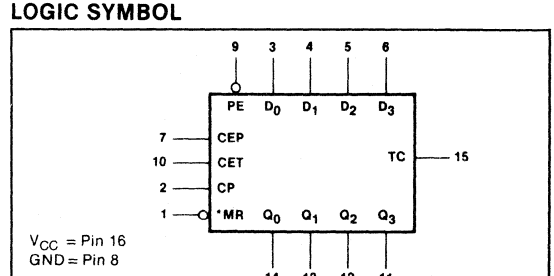
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION



*$\overline{SR}$ for 'F162A and 'F163A

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8
*SR for 'F162A and 'F163A

5

COUNTERS FAST 54/74F160A, 54/74F161A, 54/74F162A, 54/74F163A

Preview

For the 'F163A, the clear function is synchronous. A LOW level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops (Q_0-Q_3) to LOW levels after the next positive-going transition on the Clock (CP) input (providing that the setup and hold requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure A).

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to the HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage (see Figure B).

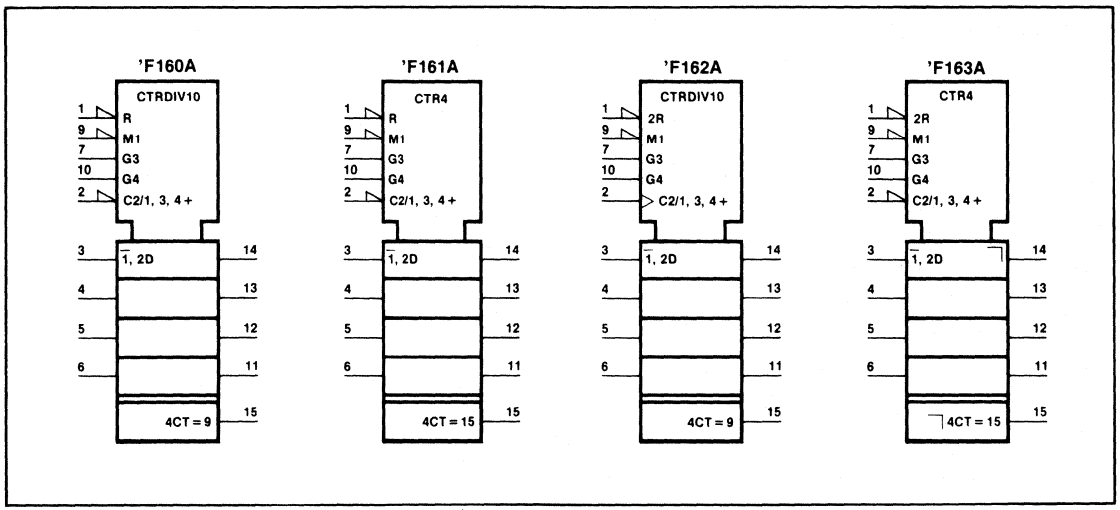
For conventional operation of 'F160A, 'F161A and 'F163A, the following transitions should be avoided:

1. HIGH-to-LOW transition on the CEP or CET input if clock is LOW.
2. LOW-to-HIGH transactions on the Parallel Enable input when CP is LOW, if the count enables and $\overline{MR}$ are HIGH at or before the transition.

For 'F163A there is an additional transition to be avoided:

3. LOW-to-HIGH transiton on the $\overline{MR}$ input when clock is LOW, if the Enable and $\overline{PE}$ inputs are HIGH at or before the transition.

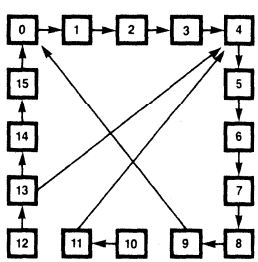
LOGIC SYMBOL (IEEE/IEC)



STATE DIAGRAMS

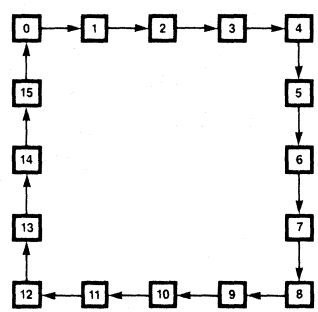
Logic Equations: Count Enable = CEP • CET • PE
$TC = Q_0 \bullet \overline{Q_1} \bullet Q_2 \bullet Q_3 \bullet CET$

'F160A, 'F162A



Logic Equations: Count Enable = CEP • CET • PE
$TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$

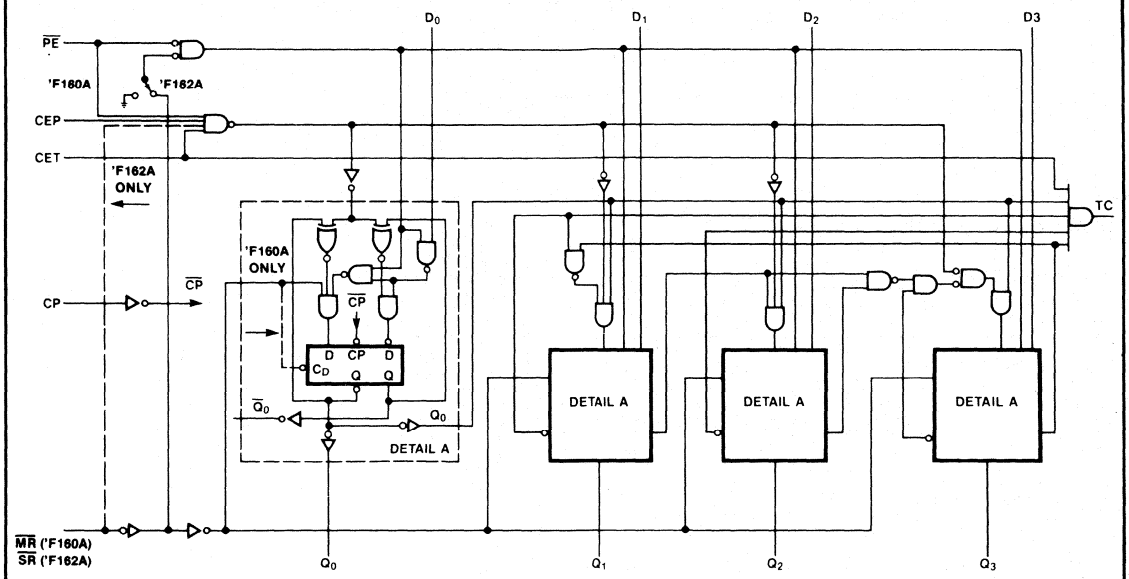
'F161A, 'F163A



COUNTERS FAST 54/74F160A, 54/74F161A, 54/74F162A, 54/74F163A

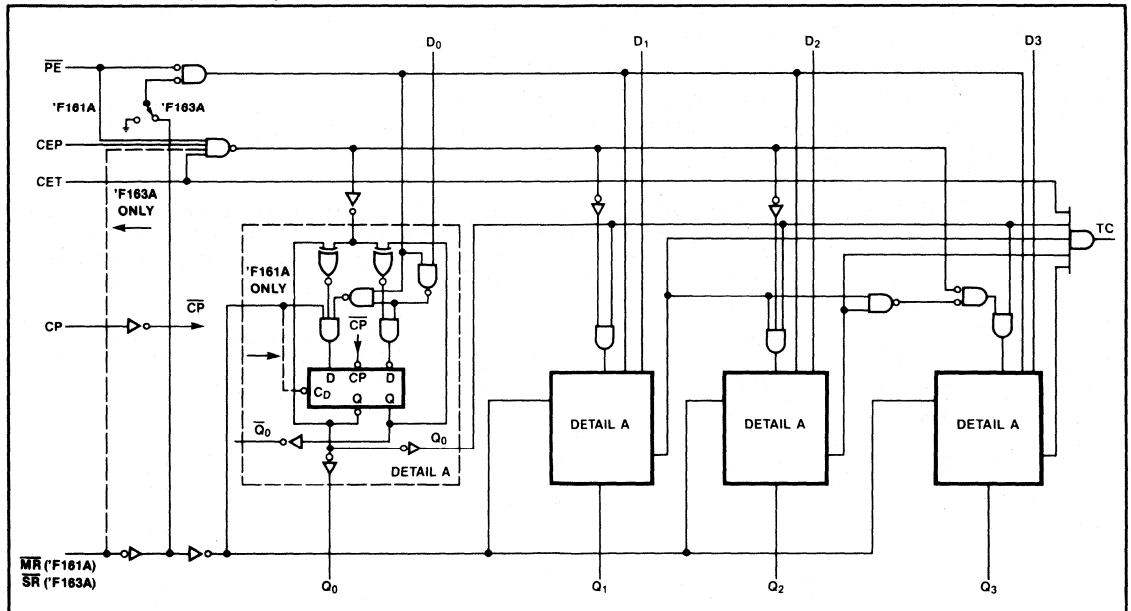
Preview

LOGIC DIAGRAM, 'F160A, 'F162A



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

LOGIC DIAGRAM, 'F161A, 'F163A



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Preview

MODE SELECT—FUNCTION TABLE, 'F160A, 'F161A

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(a)
Count	H	↑	h	h	h(c)	X	count	(a)
Hold (do nothing)	H	X	l(b)	X	h(c)	X	q_n	(a)
	H	X	X	l(b)	h(c)	X	q_n	L

MODE SELECT—FUNCTION TABLE, 'F162A, 'F163A

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (Clear)	l	↑	X	X	X	X	L	L
Parallel Load	h(f)	↑	X	X	l	l	L	L
	h(f)	↑	X	X	l	h	H	(d)
Count	h(f)	↑	h	h	h(f)	X	count	(d)
Hold (do nothing)	h(f)	X	l(e)	X	h(f)	X	q_n	(d)
	h(f)	X	X	l(e)	h(f)	X	q_n	L

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

NOTES
(a) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HHHH for 'F161A and HLLH for 'F160A).
(b) The HIGH-to-LOW transition of CEP or CET on the 'F160A and 'F161A should only occur while CP is HIGH for conventional operation.
(c) The LOW-to-HIGH transition of $\overline{PE}$ on the 'F160A and 'F161A should only occur while CP is HiGH for conventional operation.
(d) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HLLH for 'F162A and HHHH for 'F163A).
(e) The HIGH-to-LOW transition of CEP or CET on the 'F163A should only occur while CP is HIGH for conventional operation.
(f) The LOW-to-HIGH transition of $\overline{PE}$ or $\overline{MR}$ on the 'F163A should only occur while CP is HIGH for conventional operation.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

COUNTERS FAST 54/74F160A, 54/74F161A, 54/74F162A, 54/74F163A

Preview

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	– 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F160A, 'F161A, 'F162A, 'F163A			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	mil			0.5	V
			Com'l		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			– 0.73	– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V	CET, $\overline{SR}$, $\overline{PE}$			0.1	mA
			Other inputs			0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V	CET, $\overline{SR}$, $\overline{PE}$			20	μA
			Other inputs			20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	CET, $\overline{SR}$, $\overline{PE}$			– 1.2	mA
			Other inputs			– 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		– 60		– 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} All outputs HIGH			50	mA
			I_{CCL} All outputs LOW			– 50	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH} is measured with $\overline{PE}$ input HIGH, again with $\overline{PE}$ input LOW, all other inputs HIGH and outputs open. I_{CCL} is measured with Clock input HIGH, again with Clock input LOW, all other inputs LOW and outputs open.

5

COUNTERS FAST 54/74F160A, 54/74F161A, 54/74F162A, 54/74F163A

Preview

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100							MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1, PE = HIGH	3.5 4.5	5.5 7.5	7.5 10			3.5 4.5	8.5 11	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1, PE = LOW	4.0 4.0	6.0 6.0	8.5 8.5			4.0 4.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	Waveform 1	5.0 5.0		14 14			5.0 5.0	15 15	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	Waveform 2	2.5 2.5	4.5 4.5	7.5 7.5			2.5 2.5	8.5 8.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n ('F160A, 'F161A)	Waveform 3	5.5	9.0	12			5.5	13	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

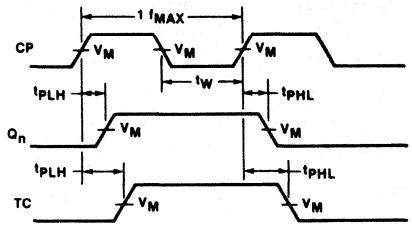
AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW D_n to CP	Waveform 5	5.0 5.0					5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to CP	Waveform 5	2.0 2.0					2.0 2.0		ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW PE or SR to CP	Waveform 5 or 6	11 5.0					11.5 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW PE or SR to CP	Waveform 5 or 6	2.0 0					2.0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW CET or CET to CP	Waveform 4	ii 5.0					11.5 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW CEP or CET ro CP	Waveform 4	2.0 0					2.0 0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width (load), HIGH or LOW	Waveform 1	5.0 5.0					5.0 5.0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width (count), HIGH or LOW	Waveform 1	4.0 6.0					4.0 7.0		ns
$t_w(L)$	$\overline{MR}$ pulse width LOW ('F160A, 'F161A)	Waveform 3	5.0					5.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP ('F160A, 'F161A)	Waveform 3	6.0					5.0		ns

Preview

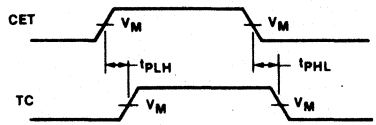
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, MAXIMUM FREQUENCY, AND CLOCK PULSE WIDTH



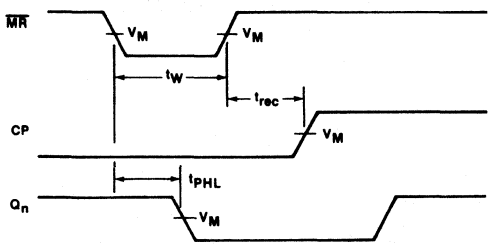
Waveform 1

PROPAGATION DELAYS CET INPUT TO TC OUTPUT



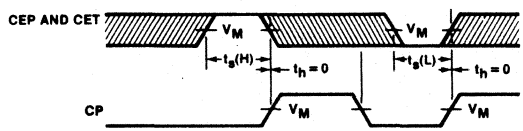
Waveform 2

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME ('F160A, 'F161A)



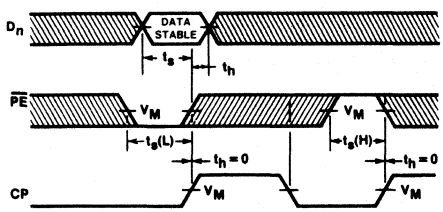
Waveform 3

CEP AND CET SETUP AND HOLD TIMES



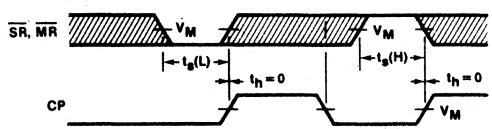
Waveform 4

PARALLEL DATA AND PARALLEL ENABLE SETUP AND HOLD TIMES



Waveform 5

SYNCHRONOUS RESET SETUP, PULSE WIDTH AND HOLD TIMES ('162, '163)



Waveform 6

$V_M = 1.5V$

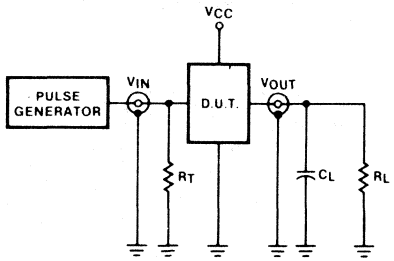
The shaded areas indicate when the input is permitted to change for predictable output performance.

5

Preview

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



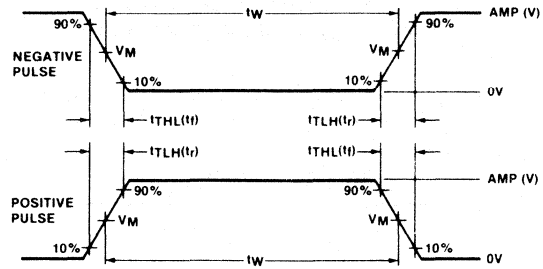
DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

APPLICATION

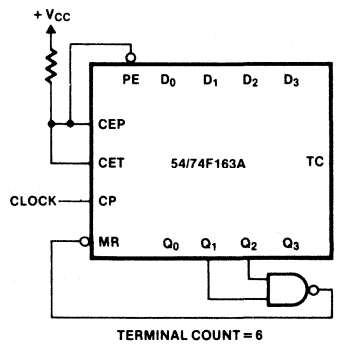


Figure A

SYNCHRONOUS MULTISTAGE COUNTING SCHEME

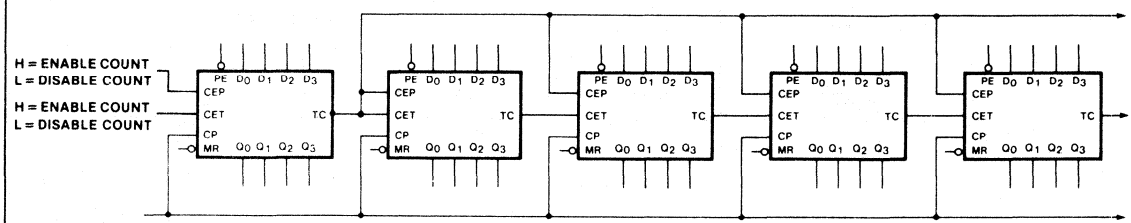


Figure B

SHIFT REGISTER — FAST 54/74F164

Preview

8-Bit Serial-In Parallel-Out Shift Register

- Gated Serial Data inputs
- Typical shift frequency of 90MHz
- Asynchronous Master Reset
- Fully buffered Clock and Data inputs
- Fully synchronous data transfers

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F164	90MHz	33mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F164N	
Plastic SO	N74F164D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (D_{sa} or D_{sb}); either input can be used as an active HIGH enable for data entry though the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the Clock (CP) input, and enters into Q_0 the logical AND of the two Data inputs ($D_{sa} \cdot D_{sb}$) that existed one setup time before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

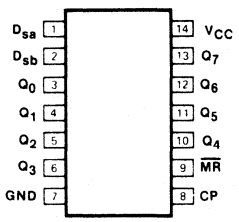
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
D_{sa}, D_{sb}	Data Inputs	1.0/1.0	20μA/0.6mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset Input (Active Low)	1.0/1.0	20μA/0.6mA
Q_0-Q_7	Outputs	50/33	1.0mA/20mA

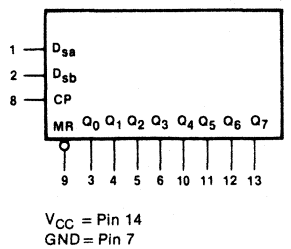
NOTE:
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

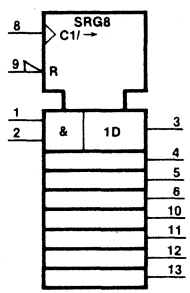
PIN CONFIGURATION



LOGIC SYMBOL



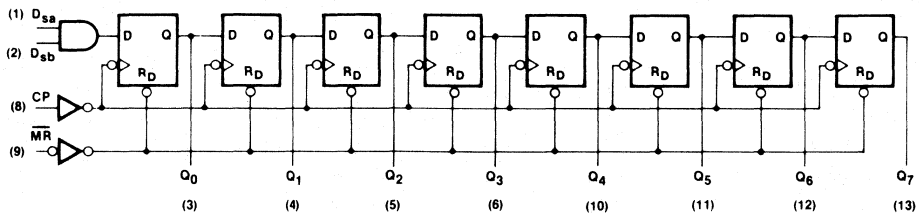
LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTER — FAST 54/74F164

Preview

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS			
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	Q_1	—	Q_7
Reset (Clear)	L	X	X	X	L	L	—	L
Shift	H	↑	l	l	L	q_0	—	q_6
	H	↑	l	h	L	q_0	—	q_6
	H	↑	h	l	L	q_0	—	q_6
	H	↑	h	h	H	q_0	—	q_6

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH Clock transition.
q = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH Clock transition.
X = Don't care.
↑ = LOW-to-HIGH Clock transition.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

SHIFT REGISTER — FAST 54/74F164

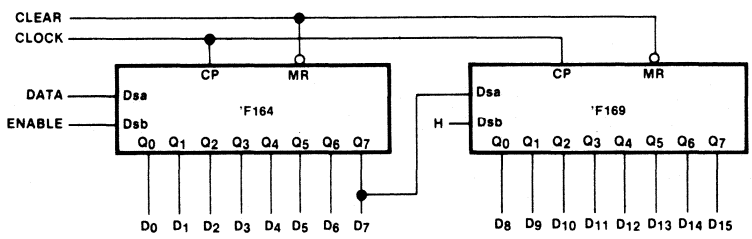
Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F164 Min	54/74F164 Typ[2]	54/74F164 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			– 0.73	– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			– 0.4	– 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		– 60	– 80	– 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			33	50	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the serial inputs grounded, the clock input at 2.4V, and a momentary ground, then 4.5V applied to Master Reset, and all outputs open.

APPLICATION



The 'F164 can be cascaded to form synchronous shift registers of longer length. Here, two devices are combined to form a 16-bit shift register.

Preview

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Shift Frequency	Waveform 1	80	90				80		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	Waveform 1	4.5 5.0	6.0 7.5	8.0 10			4.5 5.0	9.0 11	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	Waveform 2	5.5	10.5	13			8.5	14	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

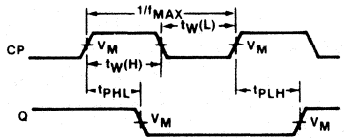
AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_s (H) t_s (L)	Setup Time, HIGH or LOW A or B to CP	Waveform 3	7.0 7.0					7.0 7.0		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW A or B to CP	Waveform 3	1.0 1.0					1.0 1.0		ns
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	Waveform 1	4.0 7.0					4.0 7.0		ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	Waveform 2	7.0					7.0		ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	Waveform 2	7.0					7.0		ns

Preview

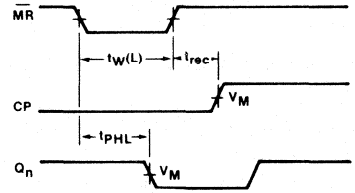
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



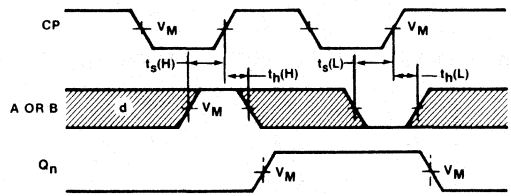
Waveform 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



Waveform 2

DATA SETUP AND HOLD TIMES



$V_M = 1.5V$

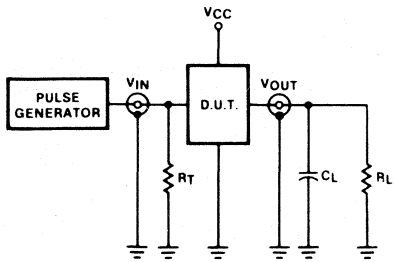
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 3

5

TEST CIRCUITS AND WAVEFORMS

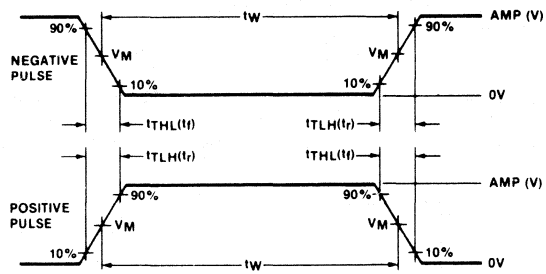
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Preview

- Synchronous counting and loading
- Up/down counting
- Modulo 16 binary counter — 'F169
- BCD decade counter — 'F168
- Two Count Enable inputs for n-bit cascading
- Positive edge-triggered clock
- Built-in lookahead carry capability
- Presettable for programmable operation

'F168 — 4-Bit Up/Down BCD Decade Synchronous Counter
'F169 — 4-Bit Up/Down Binary Synchronous Counter

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F168		50mA
74F169		50mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F168N • N74F169N	
Plastic SO	N74F168D • N74F169D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	1.0/2.0	20μA/1.2mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
D_0-D_3	Parallel Data Inputs	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0	20μA/0.6mA
U/$\overline{D}$	Up-Down Count Control Input	1.0/1.0	20μA/0.6mA
Q_0-Q_3	Flip-Flop Outputs	50/33	1.0mA/20mA
$\overline{TC}$	Terminal Count Output (Active LOW)	50/33	1.0mA/20mA

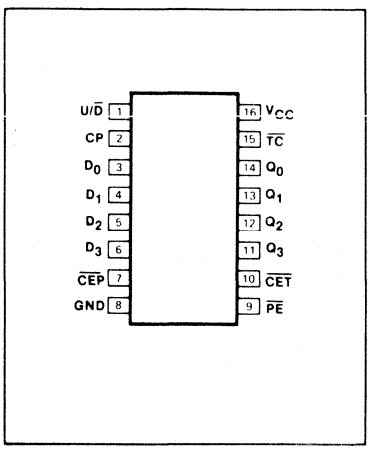
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

DESCRIPTION

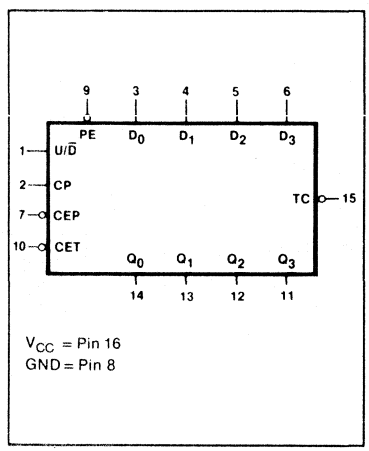
The 'F168 is a synchronous, presettable BCD decade up/down counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the LOW-to-HIGH transition of the clock.

The counter is fully programmable; that is, the outputs may be preset to either level.

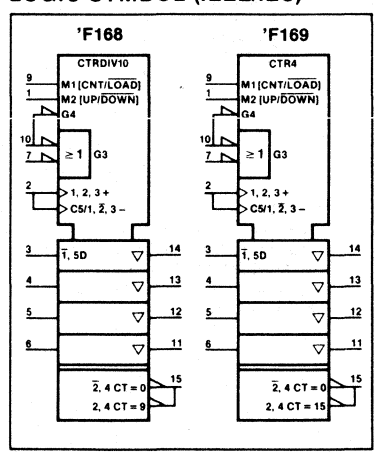
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



COUNTERS

FAST 54/74F168, 54/74F169

Preview

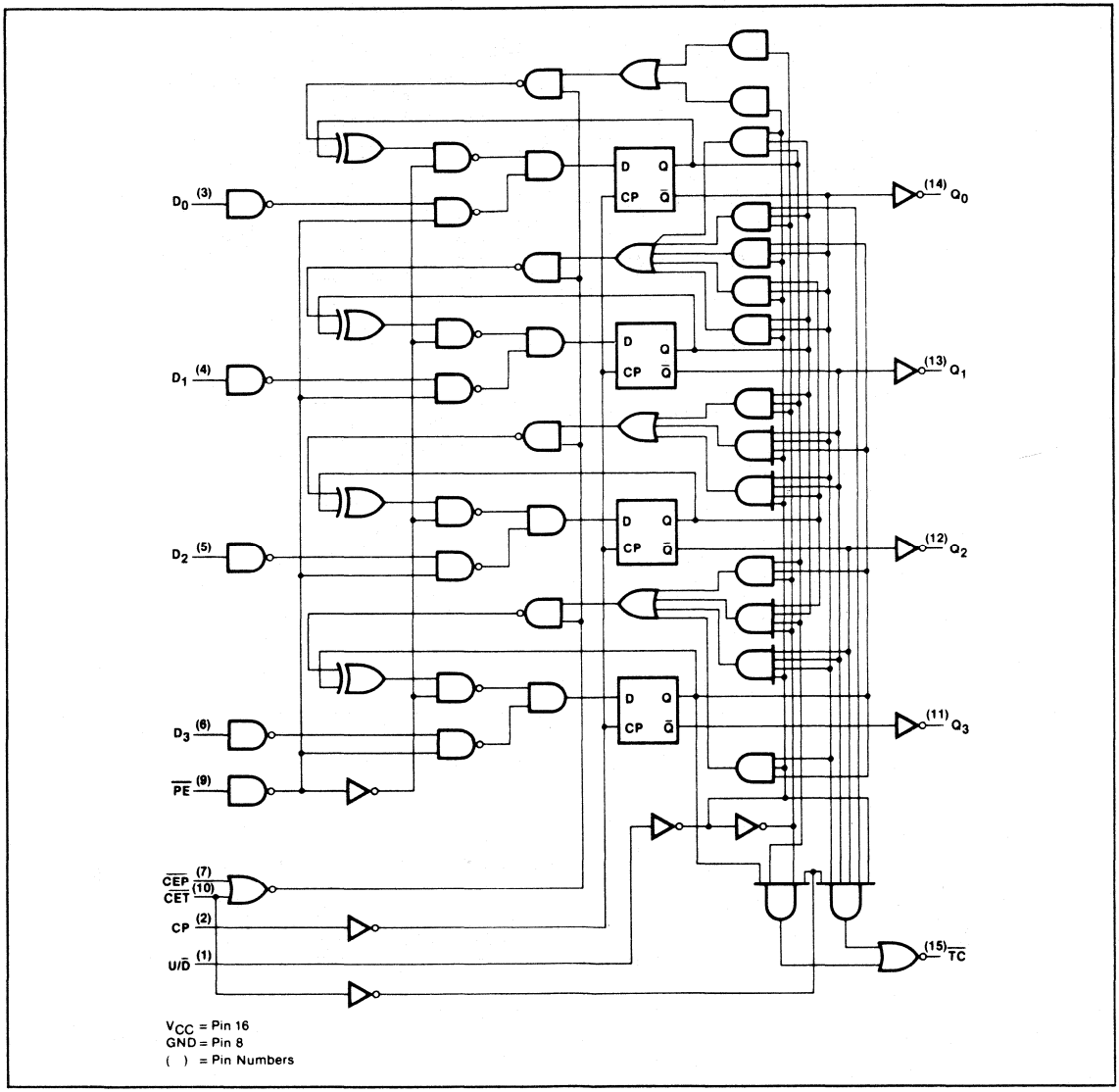
Presetting is synchronous with the clock and takes place regardless of the levels of the Count Enable inputs. A LOW level on the Parallel Enable ($\overline{PE}$) input disables the counter and causes the data at the D_n input to be loaded into the counter on the next LOW-to-HIGH transition of the clock.

The direction of counting is controlled by the Up/Down (U/$\overline{D}$) input; a HIGH will cause the count to increase, a LOW will cause the count to decrease.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs ($\overline{CET}$•$\overline{CEP}$) and a Terminal Count ($\overline{TC}$) output. Both Count Enable inputs must be LOW to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus enabled will produce a LOW output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This LOW level $\overline{TC}$ pulse is used to enable successive cascaded stages. See Figure A for the fast synchronous multistage counting connections.

The 'F169A is identical except that it is a Modulo 16 counter.

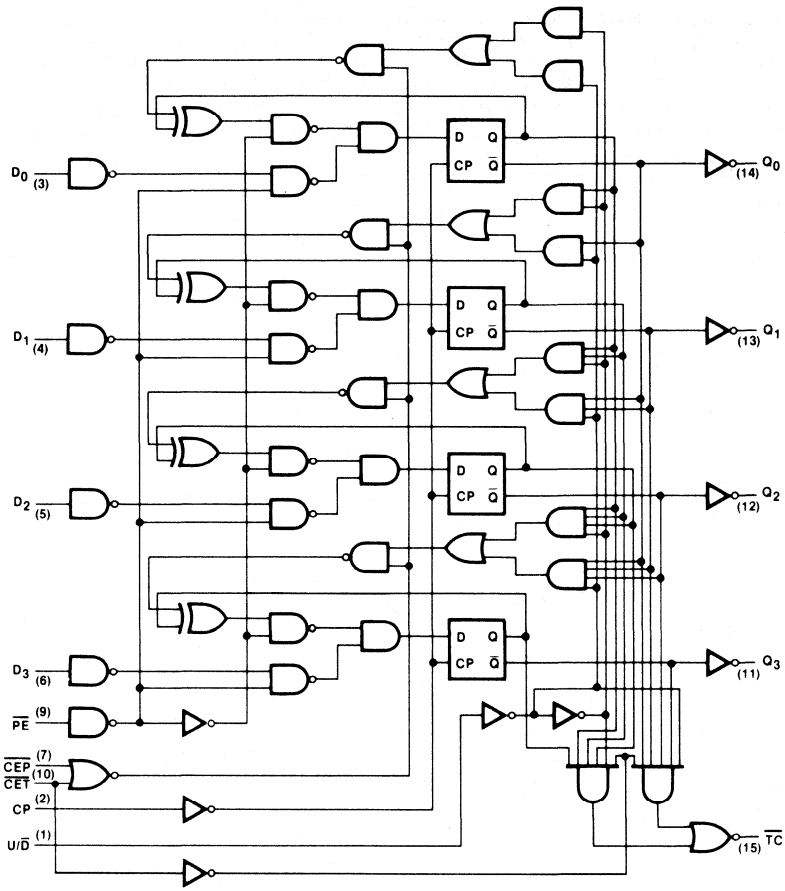
LOGIC DIAGRAM, 'F168



5

Preview

LOGIC DIAGRAM, 'F169



SYNCHRONOUS MULTISTAGE COUNTING SCHEME

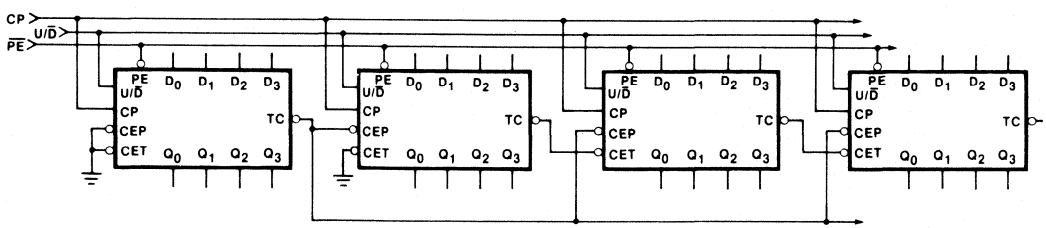


Figure A

Preview

FUNCTIONAL DESCRIPTION

The 'F168 and 'F168 use edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the Clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the D_0-D_3 inputs enter the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH; the U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the Count Down mode or reaches 9 (15 for the 'F169) in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the 'F168 decade counter can also be LOW in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the 'F168 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

1) Count Enable = $\overline{CEP} \cdot \overline{CET} \cdot \overline{PE}$
2) Up: $\overline{TC} = Q_0 \cdot Q_3 \cdot (U/\overline{D}) \cdot \overline{CET}$
3) Down: $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/\overline{D}) \cdot \overline{CET}$

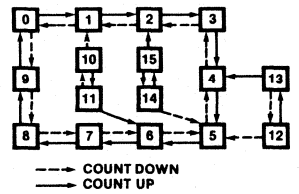
MODE SELECT TABLE

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load ($D_n \rightarrow Q_n$)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

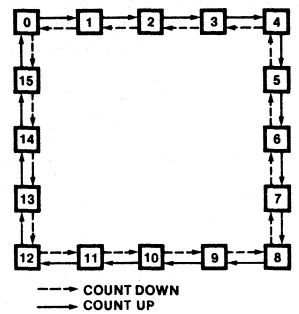
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
X = Don't Care

STATE DIAGRAMS

'F168



'F169



5

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$
Parallel Load	↑	X	X	X	l	l	L	(a)
	↑	X	X	X	l	h	H	(a)
Count Up	↑	h	l	l	h	X	Count Up	(a)
Count Down	↑	l	l	l	h	X	Count Down	(a)
Hold (do nothing)	↑	X	h	X	h	X	q_n	(a)
	↑	X	X	h	h	X	q_n	H

H = HIGH voltage level steady state
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady state
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition

NOTE
a. The $\overline{TC}$ is LOW when $\overline{CET}$ is LOW and the counter is at Terminal Count. Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for '169A. The $\overline{TC}$ is LOW when $\overline{CET}$ is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for '168A.

Preview

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F168, 'F169			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.35	0.5	V
				Com'l		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 7.0V	$\overline{PE}$ input			100	μA
				Other inputs			100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.7V	$\overline{PE}$ input			20	μA
				$\overline{CET}$ input			20	μA
				Other inputs			20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.5V	$\overline{CET}$ input			−1.2	mA
				Other inputs			−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				50	75	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured after applying a momentary 4.5V, then ground to the clock input with all other inputs grounded and outputs open.

Preview

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115				90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$, HIGH or LOW)	Waveform 1	3.0 4.0	6.5 9.0	8.5 11.5			3.0 4.0	9.5 13.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	5.5 4.0	12.0 8.5	15.5 11.0			5.5 4.0	17.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	2.5 2.5	4.5 6.0	6.0 8.0			2.5 2.5	7.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$ ('F168)	Waveform 3	3.5 4.0	8.5 12.5	11.0 16			3.5 4.0	12.5 17.5	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$ ('F169)	Waveform 3	3.5 4.0	8.5 8.0	11.0 10.5			3.5 4.0	12.5 12.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

5

AC SETUP REQUIREMENTS

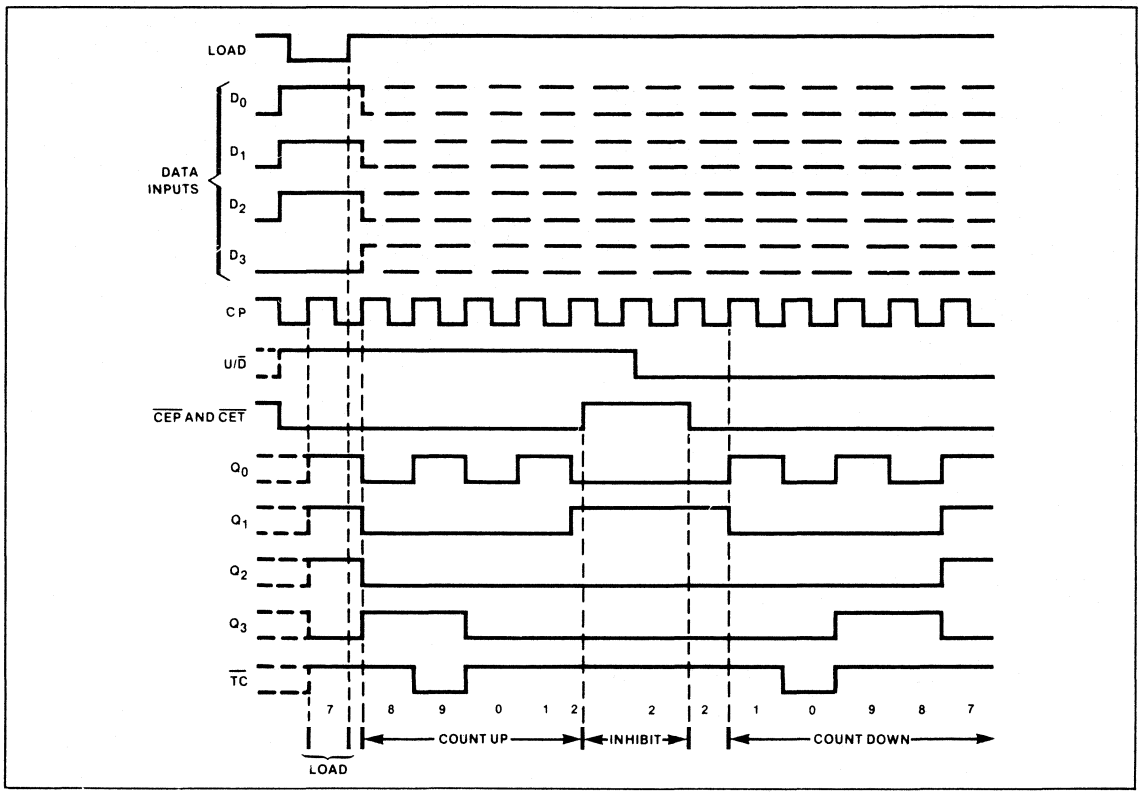
PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW D_n to CP	Waveform 4	4.0 4.0					4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to CP	Waveform 4	3.0 3.0					3.0 3.0		ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	5.0 5.0					5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	0 0					0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW $\overline{PE}$ to CP	Waveform 4	8.0 8.0					11.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{PE}$ to CP	Waveform 4	0 0					0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW U/$\overline{D}$ to CP ('F168)	Waveform 6	11.0 16.5					11.0 16.5		ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW U/$\overline{D}$ to CP ('F169)	Waveform 6	11.0 7.0					11.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW U/$\overline{D}$ to CP	Waveform 6	0 0					0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, HIGH or LOW	Waveform 1	4.0 6.0					4.0 6.0		ns

Preview

WAVEFORM (Typical Load, Count, and Inhibit Sequences)

Illustrated below is the following sequence for the 'F168. The operation of the 'F169 is similar.

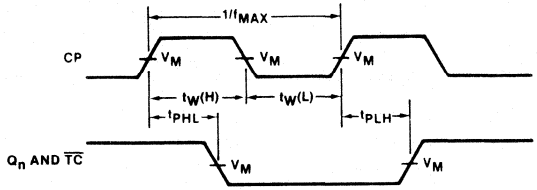
1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



Preview

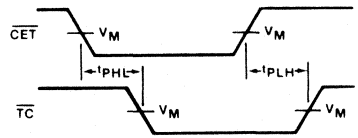
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



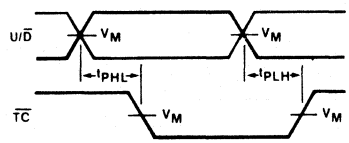
Waveform 1

PROPAGATION DELAYS CET INPUT TO TERMINAL COUNT OUTPUT



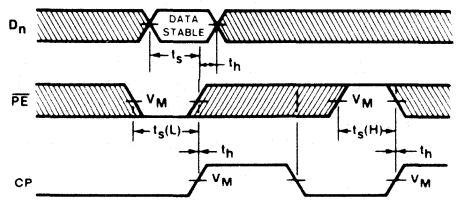
Waveform 2

PROPAGATION DELAYS U/D CONTROL TO TERMINAL COUNT OUTPUT



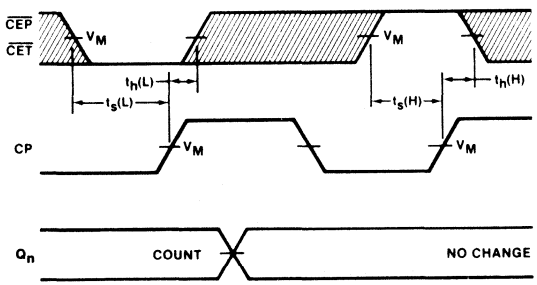
Waveform 3

PARALLEL DATA AND PARALLEL ENABLE SETUP AND HOLD TIMES



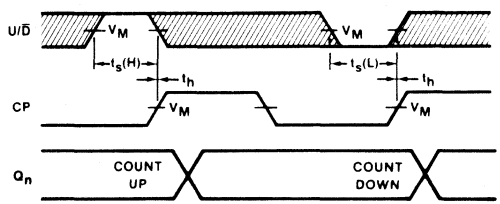
Waveform 4

COUNT ENABLE SETUP AND HOLD TIMES



Waveform 5

UP/DOWN CONTROL SETUP AND HOLD TIMES



Waveform 6

$V_M = 1.5V$

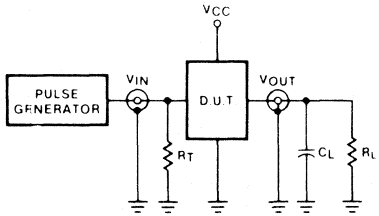
The shaded areas indicate when the input is permitted to change for predictable output performance

5

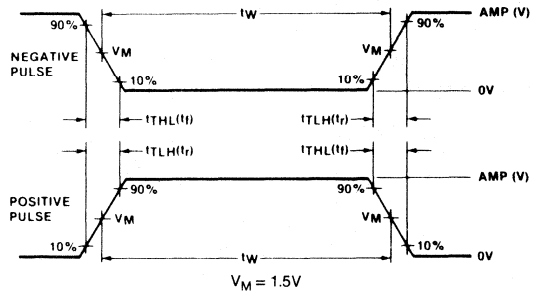
Preview

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

HEX D FLIP-FLOP

FAST 54/74F174

Preview

Hex D Flip-Flop

- **Six edge-triggered D-type flip-flops**
- **Three speed-power ranges available**
- **Buffered common Clock**
- **Buffered, asynchronous Master Reset**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F174	100MHz	30mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F174N	
Plastic SO	N74F174D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F174 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

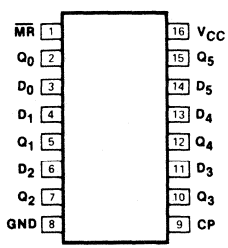
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and master Reset are common to all storage elements.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

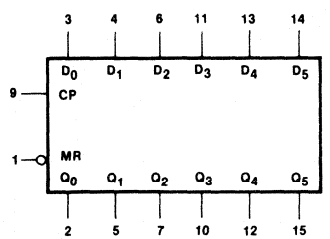
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
D_0-D_5	Data Inputs	1.0/1.0	20μA/0.6mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset Input (Active Low)	1.0/1.0	20μA/0.6mA
Q_0-Q_5	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION

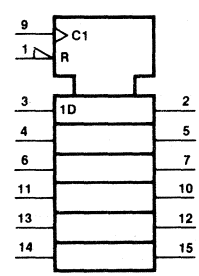


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)

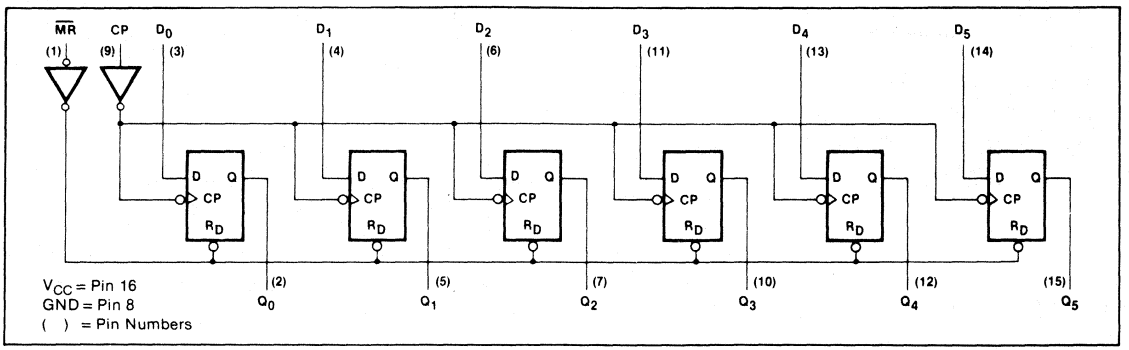


HEX D FLIP-FLOP

FAST 54/74F174

Preview

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = HIGH voltage level steady state
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

HEX D FLIP-FLOP — FAST 54/74F174

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F174 Min	54/74F174 Typ[2]	54/74F174 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			− 0.73	− 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			− 0.4	− 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		− 60	− 80	− 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			30	45	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured after a momentary ground, then 4.5V is applied to clock, with 4.5V applied to all Data and $\overline{MR}$ inputs and all outputs open.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	Waveform 1	80	100				80		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	Waveform 1	3.5 4.5	5.5 7.0	8.0 10			3.5 4.5	9.0 11.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	Waveform 3	5.0	10	14			5.0	15.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_s (H) t_s (L)	Setup Time, HIGH or LOW Dn to CP	Waveform 2	4.0 4.0					4.0 4.0		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW Dn to CP	Waveform 2	0 0					0 0		ns
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	Waveform 1	4.0 6.0					4.0 6.0		ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	Waveform 3	5.0					5.0		ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	Waveform 3	5.0					5.0		ns

5

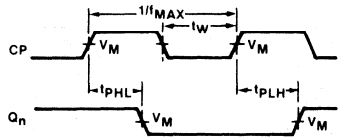
HEX D FLIP-FLOP

FAST 54/74F174

Preview

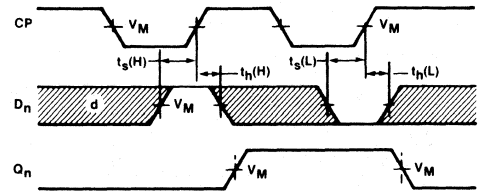
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

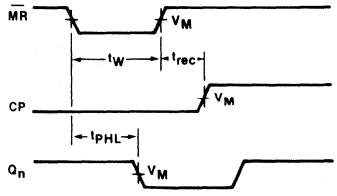
DATA SETUP AND HOLD TIMES



The shaded areas indicate when the input is permitted to change for predictable output performance

Waveform 2

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME

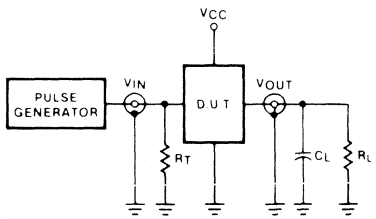


$V_M = 1.5V$

Waveform 3

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



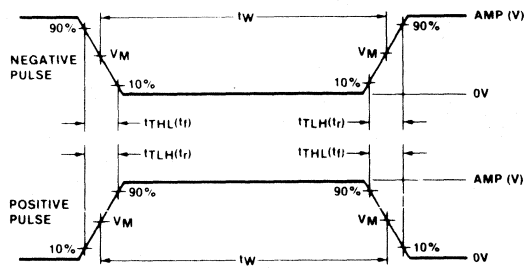
DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

QUAD D FLIP-FLOP — FAST 54/74F175

Preview

Quad D Flip-Flop

- Four edge-triggered D-type flip-flops
- Three speed-power ranges available
- Buffered common Clock
- Buffered, asynchronous Master Reset
- True and complement output

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F175	140MHz	22.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F175N	
Plastic SO	N74F175D	
Ceramic DIP		S54F175F
Ceramic LLCC		S54F175G

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F175 is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where both true and complement outputs are required, and the Clock and Master Reset are common to all storage elements.

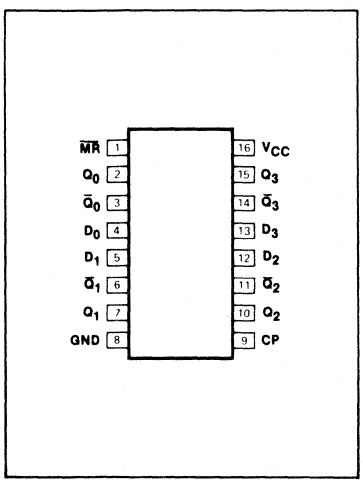
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
D_0-D_3	Data Inputs	1.0/1.0	20μA/0.6mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset Input (Active Low)	1.0/1.0	20μA/0.6mA
Q_0-Q_3	True Outputs	50/33	1.0mA/20mA
$\overline{Q}_0$-$\overline{Q}_3$	Complement Inputs	50/33	1.0mA/20mA

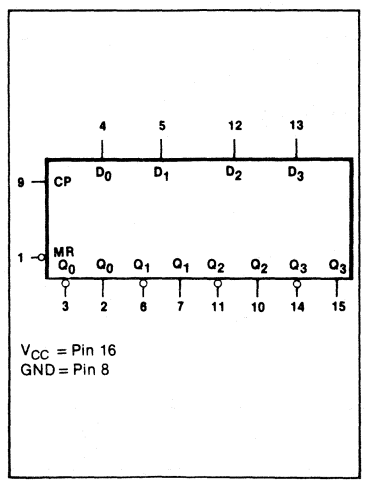
NOTE:
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

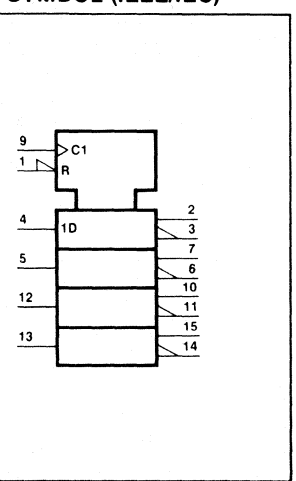
PIN CONFIGURATION



LOGIC SYMBOL



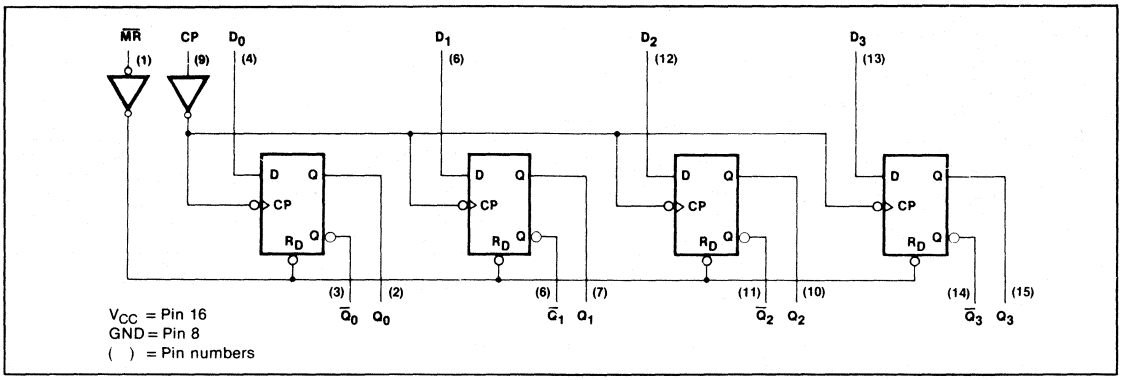
LOGIC SYMBOL (IEEE/IEC)



QUAD D FLIP-FLOP — FAST 54/74F175

Preview

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
Reset (clear)	L	X	X	L	H
Load "1"	H	↑	h	H	L
Load "0"	H	↑	l	L	H

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

QUAD D FLIP-FLOP — FAST 54/74F175

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F/75 Min	54/74F/75 Typ[2]	54/74F/75 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			– 0.73	– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			– 0.4	– 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		– 60	– 80	– 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			22.5	34	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With all outputs open and 4.5V applied to all Data and Master Reset inputs, I_{CC} is measured after a momentary ground, the 4.5V is applied to clock.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	Waveform 1	100	140		100		100		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}_n$	Waveform 1	4.0 4.0	5.0 6.5	6.5 8.5	3.5 4.0	8.5 10.5	4.0 4.0	7.5 9.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	Waveform 3	4.5	9.0	11.5	4.5	15	4.5	13	ns
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	Waveform 3	4.0	6.5	8.0	4.0	10	4.0	9.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_s (H) t_s (L)	Setup Time, HIGH or LOW Dn to CP	Waveform 2	3.0 3.0			3.0 3.0		3.0 3.0		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW Dn to CP	Waveform 2	1.0 1.0			1.0 1.0		1.0 1.0		ns
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	Waveform 1	4.0 5.0			4.0 5.0		4.0 5.0		ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	Waveform 3	5.0			5.0		5.0		ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	Waveform 3	5.0			5.0		5.0		ns

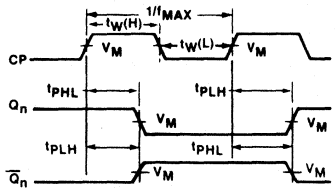
5

QUAD D FLIP-FLOP FAST 54/74F175

Preview

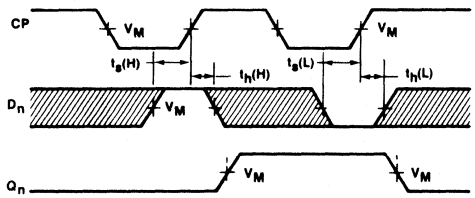
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



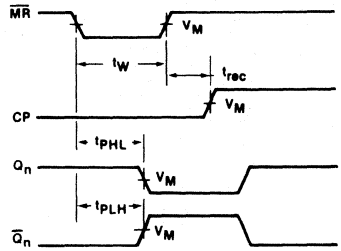
Waveform 1

DATA SET-UP AND HOLD TIMES



Waveform 2

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME



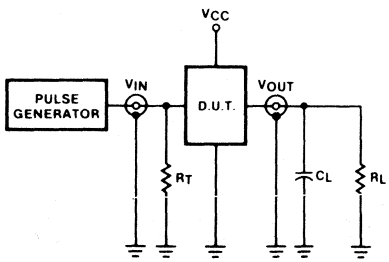
Waveform 3

$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



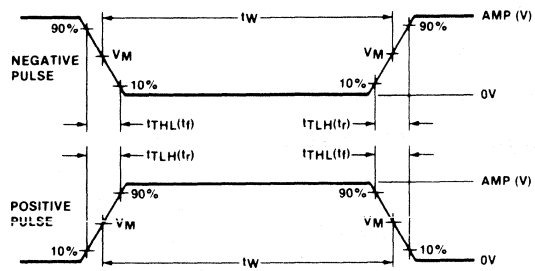
DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

ARITHMETIC LOGIC UNIT — FAST 54/74F181

Preliminary

4-Bit Arithmetic Logic Unit

- **Provides 16 arithmetic operations: ADD, SUBTRACT, COMPARE, DOUBLE, plus 12 other arithmetic operations**
- **Provides all 16 logic operations of two variables: Exclusive-OR, Compare, AND, NAND, NOR, OR, plus 10 other logic operations**
- **Full lookahead carry for high-speed arithmetic operation on long words**
- **40% faster than 'S181 with only 30% 'S181 power consumption**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F181	7.0 ns	43 mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F181N	
Plastic SO	N74F181D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
M	Mode Control Input	1.0/1.0	20μA/0.6mA
$\overline{A}_0$-$\overline{A}_3$, $\overline{B}_0$-$\overline{B}_2$	Operand Inputs	1.0/1.0	20μA/0.6mA
S_0-S_3	Function Select Inputs	1.0/1.0	20μA/0.6mA
C_n	Carry Input	1.0/1.0	20μA/0.6mA
$\overline{F}_0$-$\overline{F}_3$, A = B, C_{n+4}	Outputs	50/33	1.0mA/20mA
$\overline{G}$	Carry Generate Output	50/33	1.0mA/20mA
$\overline{P}$	Carry Propagate Output	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

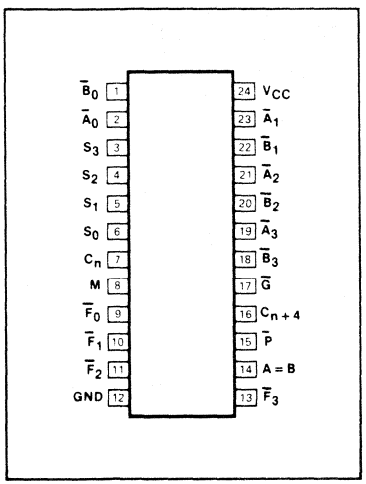
5

DESCRIPTION

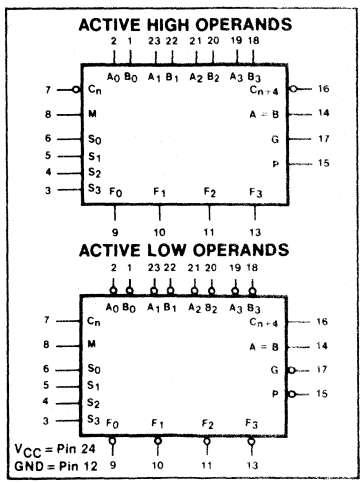
The 'F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0-S_3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed require-

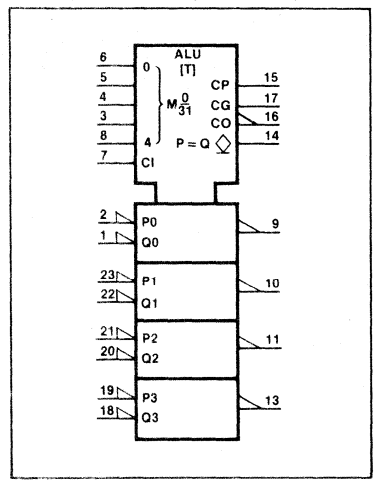
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ARITHMETIC LOGIC UNIT FAST 54/74F181

Preliminary

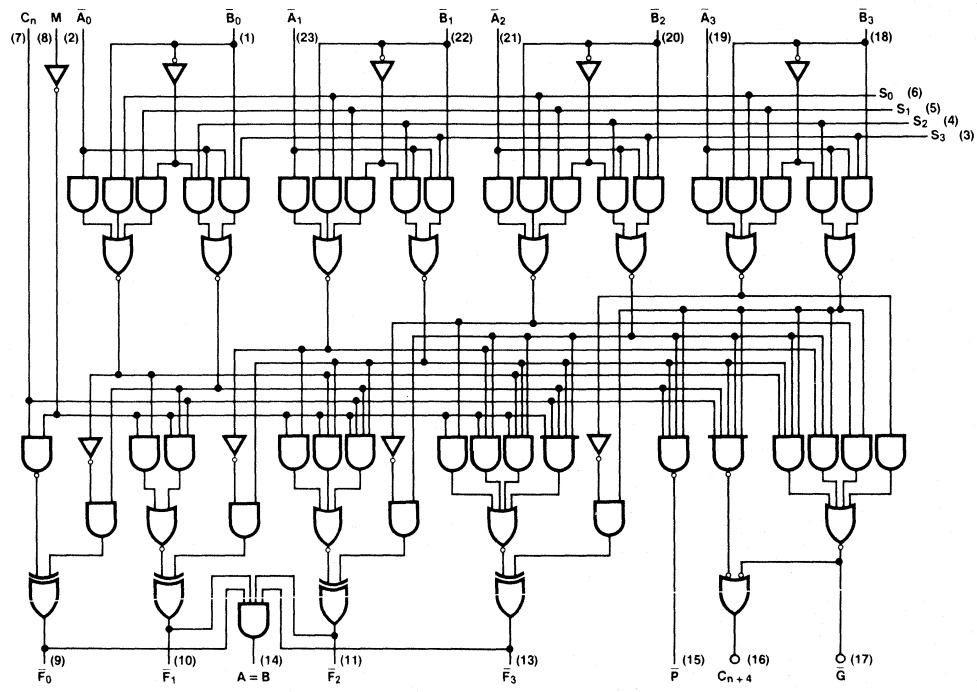
ments are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with the '182 carry lookahead circuit. One carry lookahead package is required for each group of four '181 devices. Carry lookahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than 4 bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12
( ) = Pin numbers
Pin 14 is O.C.

ARITHMETIC LOGIC UNIT — FAST 54/74F181

Preliminary

MODE SELECT—FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE HIGH INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A
L	L	L	H	$\overline{A+B}$	A + B
L	L	H	L	$\overline{A}B$	A + $\overline{B}$
L	L	H	H	Logical 0	minus 1
L	H	L	L	$\overline{AB}$	A plus A$\overline{B}$
L	H	L	H	$\overline{B}$	(A + B) plus A$\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	A$\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}+B$	A plus AB
H	L	L	H	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	(A + $\overline{B}$) plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	Logical 1	A plus A*
H	H	L	H	A + $\overline{B}$	(A + B) plus A
H	H	H	L	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A minus 1

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)
L	L	L	L	$\overline{A}$	A minus 1
L	L	L	H	$\overline{AB}$	AB minus 1
L	L	H	L	$\overline{A}+B$	A$\overline{B}$ minus 1
L	L	H	H	Logical 1	minus 1
L	H	L	L	$\overline{A+B}$	A plus (A + $\overline{B}$)
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	$\overline{A+B}$	A + $\overline{B}$
H	L	L	L	$\overline{A}B$	A plus (A + B)
H	L	L	H	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	A$\overline{B}$ plus (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	Logical 0	A plus A*
H	H	L	H	A$\overline{B}$	AB plus A
H	H	H	L	AB	A$\overline{B}$ plus A
H	H	H	H	A	A

L = LOW voltage
H = HIGH voltage level
*Each bit is shifted to the next more significant position.
**Arithmetic operations expressed in 2s complement notation.

5

SUM MODE TEST TABLE I

FUNCTION INPUTS: $S_0 = S_3 = 4.5V$, $S_1 = S_2 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

ARITHMETIC LOGIC UNIT — FAST 54/74F181

Preliminary

DIFF MODE TEST TABLE II

FUNCTION INPUTS: $S_1 = S_2 = 4.5V$, $S_0 = S_3 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 1	− 30 to + 1	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

ARITHMETIC LOGIC UNIT — FAST 54/74F181

Preliminary

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	– 55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]				54/74F181			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX		Mil	2.5	3.4		V
					Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX					0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 0.73	– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = + 7.0V					5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.7V	Mode input			1	20	μA
				A or B inputs			1	20	μA
				S inputs			1	20	μA
				Carry input			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.5V	Mode input				0.6	mA
				A or B inputs				0.6	mA
				S inputs				0.6	mA
				Carry input				0.6	mA
I_{OH}	HIGH-level output current	V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 4.5V, A = B only						250	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX Any output except A = B				– 60	– 80	– 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Note 4a				65	mA
				Note 4b				65	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with the following conditions: a. S_0 through S_3, M, and A inputs are at 4.5V, other inputs grounded, all outputs open; b. S_0 through S_3 and M inputs are a 4.5V, other inputs grounded, all outputs open.

5

ARITHMETIC LOGIC UNIT — FAST 54/74F181

Preliminary

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic".)

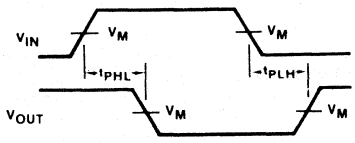
PARAMETER	TEST CONDITIONS	54F/74F T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF			54F T_A, V_{CC} = Mil, C_L = 50pF		74F T_A, V_{CC} = Com, C_L = 50pF		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	M = 0V, Sum or Diff Mode	3.0	6.4	8.5	3.0	12.5	3.0	9.5	ns
t_{PHL} C_n to C_{n+4}	see Waveform 2 and Tables I and II	3.0	6.1	8.0	3.0	11.5	3.0	9.0	
t_{PLH} Propagation delay	M = 0V, Sum or Diff Mode	3.0	6.7	8.5	3.0	12.0	3.0	9.5	ns
t_{PHL} C_n to $\overline{F}$ outputs	see Waveform 2 and Tables I and II	3.0	6.5	8.5	3.0	12.0	3.0	9.5	
t_{PLH} Propagation delay	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V	3.0	5.7	7.5	3.0	10.5	3.0	8.5	ns
t_{PHL} $\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output	Sum Mode, see Waveform 2 and Table I	3.0	5.8	7.5	3.0	10.5	3.0	8.5	
t_{PLH} Propagation delay	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V	3.0	6.5	8.5	3.0	12	3.0	9.5	ns
t_{PHL} $\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output	Diff Mode, see Waveform 3 and Table II	3.0	7.3	9.5	3.0	13.5	3.0	10.5	
t_{PLH} Propagation delay	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V	3.0	5.0	7.0	3.0	10	3.0	8.0	ns
t_{PHL} $\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output	Sum Mode, see Waveform 2 and Table I	3.0	5.5	7.5	3.0	10.5	3.0	8.5	
t_{PLH} Propagation delay	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V	4.0	5.8	7.5	4.0	10.5	4.0	8.5	ns
t_{PHL} $\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output	Diff Mode, see Waveform 3 and Table II	4.0	6.5	8.5	4.0	12	4.0	9.5	
t_{PLH} Propagation delay	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V	4.0	7.0	9.0	4.0	12.5	4.0	10	ns
t_{PHL} $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	Sum Mode, see Waveform 2 and Table I	4.0	7.2	10	4.0	14	4.0	10	
t_{PLH} Propagation delay	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V	4.5	8.2	11	4.5	15.5	4.5	12	ns
t_{PHL} $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	Diff Mode, see Waveform 3 and Table II	4.5	5.0	11	4.5	15.5	4.5	12	
t_{PLH} Propagation delay	M = 4.5V, Logic Mode	4.0	6.0	9	4.0	12.5	4.5	13	ns
t_{PHL} $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	see Waveform 2 and Table III	4.0	6.0	10	4.0	19	4.5	13	
t_{PLH} Propagation delay	M = 0V, S_0 = S_3 = 4.5V, S_1 = S_2 = 0V	7.0	10	13	7.0	18	7.0	14	ns
t_{PHL} $\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output	Sum Mode, see Waveform 1 and Table I	7.0	9.4	12	7.0	17	7.0	13	
t_{PLH} Propagation delay	M = 0V, S_0 = S_3 = 0V, S_1 = S_2 = 4.5V	7.0	10.8	14	7.0	19.5	7.0	15	ns
t_{PHL} $\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output	Diff Mode, see Waveform 4 and Table II	7.0	10	13	7.0	18	7.0	14	
t_{PLH} Propagation delay	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V	11	18.5	27	11	35	11	29	ns
t_{PHL} $\overline{A}$ or $\overline{B}$ inputs to A=B output	Diff Mode, see Waveform 3 and Table II	7.0	9.8	12.5	7.0	17.5	7.0	13.5	
t_{PLH} Propagation delay	Sam Mode, see Waveforms 1 and 2	4.0	8.0	10.5	7.0	15.5	4.0	11.5	ns
t_{PHL} Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$		4.0	7.8	10	4.0	14	4.0	11	
t_{PLH} Propagation delay	Diff Mode, see Waveforms 1 and 2	4.5	9.4	12	4.5	17	4.5	13	ns
t_{PHL} Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$		4.5	9.4	12	4.5	17	4.5	13	

NOTE
Subtract 0.2ns from minimum values for SO package.

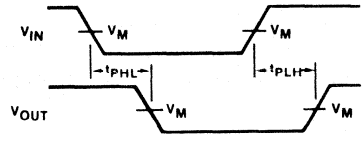
ARITHMETIC LOGIC UNIT — FAST 54/74F181

Preliminary

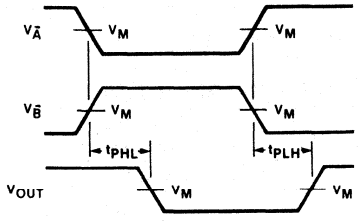
AC WAVEFORMS



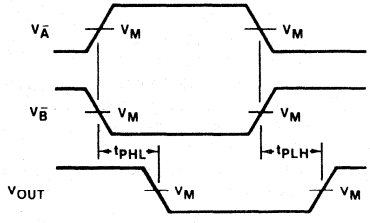
Waveform 1



Waveform 2



Waveform 3



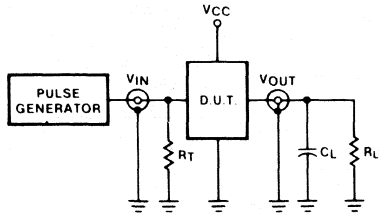
Waveform 4

$V_M = 1.5V$

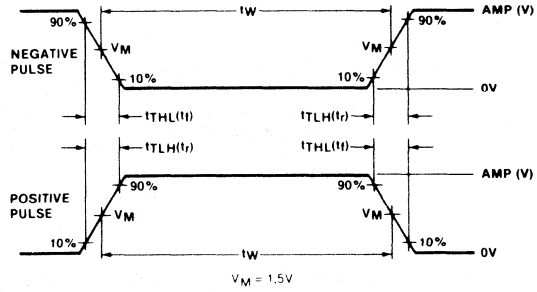
5

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



$V_M = 1.5V$

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

CARRY LOOKAHEAD GENERATOR — FAST 54/74F182

Preview

Carry Lookahead Generator

- **Provides carry lookahead across a group of four ALU's**
- **Multi-level lookahead for high-speed arithmetic operation over long word lengths**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F182		21mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F182N	
Plastic SO	N74F182D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F182 carry lookahead generator accepts up to four pairs of active LOW Carry Propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and Carry Generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active HIGH Carry input (C_n) and provides anticipated active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The 'F182 also has active LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0 C_n$$

$$C_{n+y} = G_1 + P_1 G_0 = P_1 P_0 C_n$$

$$C_{n+z} = G_2 + P_2 G_1 + P_2 P_2 G_0 + P_2 P_1 P_0 C_n$$

$$\overline{G} = \overline{G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0}$$

$$\overline{P} = \overline{P_3 P_2 P_1 P_0}$$

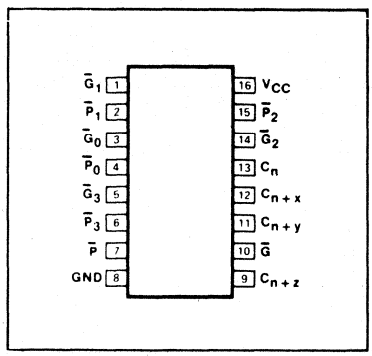
The 'F182 can also be used with binary ALU's in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry lookahead generator are identical in both cases.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

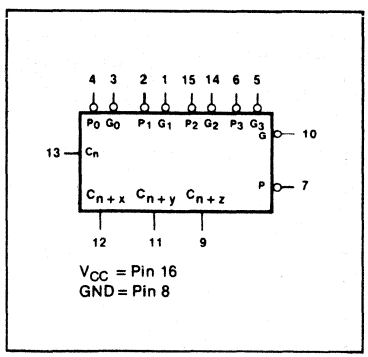
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
Cn	Carry Input	1.0/2.0	20μA/1.2 mA
$\overline{G}_0$,$\overline{G}_2$	Carry Generate Inputs (Active LOW)	1.0/14.0	20μA/8.4mA
$\overline{G}_1$	Carry Generate Input (Active LOW)	1.0/16.0	20μA/9.6mA
$\overline{G}_3$	Carry Generate Input (Active LOW)	1.0/8.0	20μA/4.8mA
$\overline{P}_0$,$\overline{P}_1$	Carry Propagate Inputs (Active LOW)	1.0/8.0	20μA/4.8mA
$\overline{P}_2$	Carry Propagate Input (Active LOW)	1.0/6.0	20μA/3.6mA
$\overline{P}_3$	Carry Propagate Input (Active LOW)	1.0/4.0	20μA/2.4mA
C_{n+x} – C_{n+z}	Carry Outputs	50/33	1.0mA/20mA
$\overline{G}$	Carry Generate Output (Active LOW)	50/33	1.0mA/20mA
$\overline{P}$	Carry Propagate Output (Active LOW)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

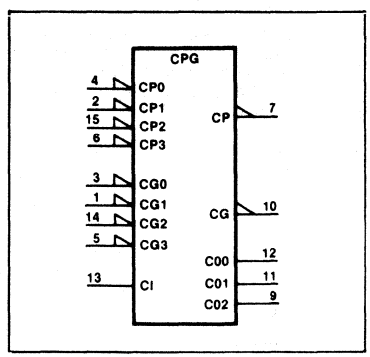
PIN CONFIGURATION



LOGIC SYMBOL



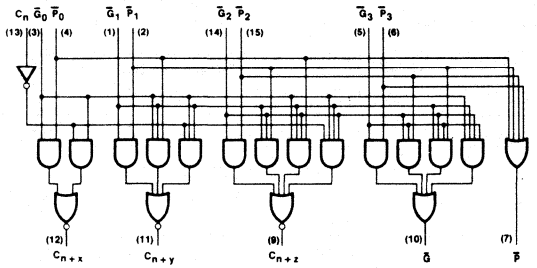
LOGIC SYMBOL (IEEE/IEC)



CARRY LOOKAHEAD GENERATOR — FAST 54/74F182

Preview

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

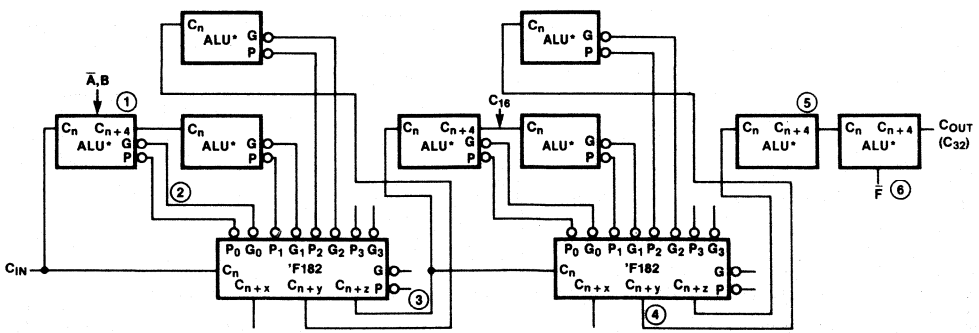
FUNCTION TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	X	H	X	H	X					L		
L	H	X	H	X	L	X					H		
X	X	X	X	X	X	L					H		
X	X	X	X	L	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	X	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	L	L				L	
	L		X	L	X	L	L	L				L	
		H		X		X		X					H
		X		X		H		X					H
		X		X		X		X					H
		X		X		X		H					H
		L		X		L		L					L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

APPLICATION

32-BIT ALU WITH RIPPLE CARRY BETWEEN 16-BIT LOOKAHEAD ALUs



*ALU's may be either 'F181, 'F381 or 2901A.

5

CARRY LOOKAHEAD GENERATOR — FAST 54/74F182

Preview

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F182			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	C_n				−1.2	mA
			$\overline{G}_0$, $\overline{G}_2$				−8.4	mA
			$\overline{G}_1$				−9.6	mA
			$\overline{G}_3$, $\overline{P}_0$, $\overline{P}_1$				−4.8	mA
			$\overline{P}_2$				−3.6	mA
			$\overline{P}_3$				−2.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−60	−80	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		18.4	28	mA
			I_{CCL}	Outputs LOW		23.5	36	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with $\overline{G}_0$, $\overline{G}_1$, and $\overline{G}_2$ inputs at 4.5V; all other inputs grounded and all outputs open.

CARRY LOOKAHEAD GENERATOR — FAST 54/74F182

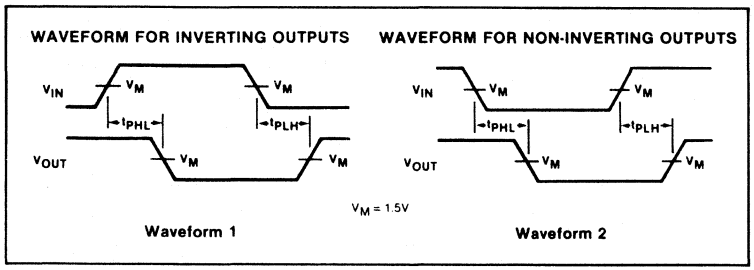
Preview

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

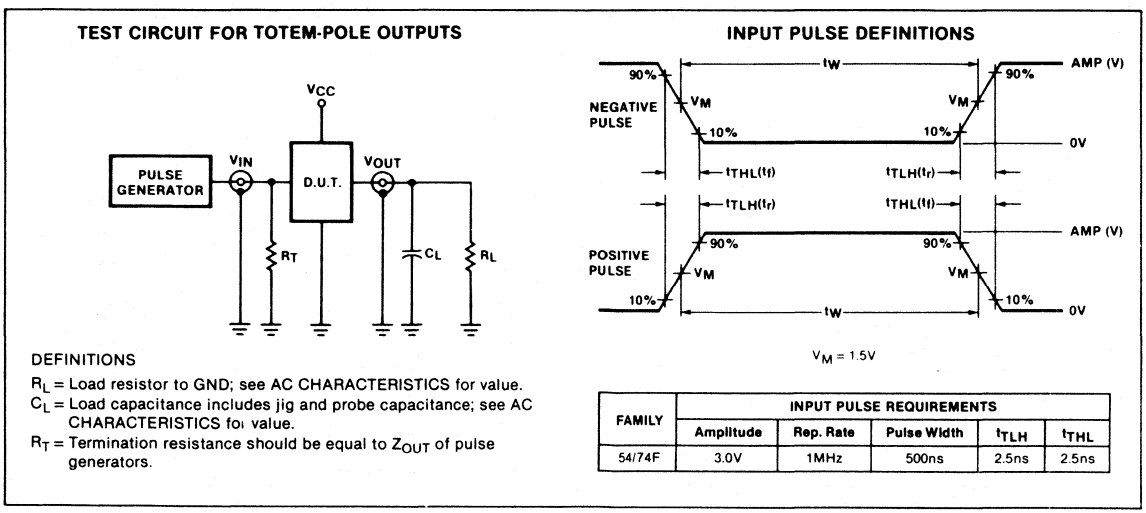
PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} Propagation Delay t_{PHL} C_n to C_{n+x}, C_{n+y}, C_{n+z}	Waveform 2	3.0 3.0	6.6 6.8	8.5 9.0	3.0 3.0	10.5 11	3.0 3.0	9.5 10	ns
t_{PLH} Propagation Delay t_{PHL} $\overline{P}_o$, $\overline{P}_1$ or $\overline{P}_2$ to C_{n+x}, C_{n+y}, C_{n+z}	Waveform 1	2.5 2.0	6.2 3.7	8.0 5.0	2.5 2.0	10.7 6.5	2.5 2.0	9.0 6.0	ns
t_{PLH} Propagation Delay t_{PHL} $\overline{G}_o$, $\overline{G}_1$ or $\overline{G}_2$ to C_{n+x}, C_{n+y}, C_{n+z}	Waveform 1	2.5 2.0	6.5 3.9	8.5 5.2	2.5 2.0	10.5 6.5	2.5 2.0	9.5 6.0	ns
t_{PLH} Propagation Delay t_{PHL} $\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{G}$	Waveform 2	3.0 3.0	7.9 6.0	10.5 8.0	3.0 3.0	12.5 9.5	3.0 3.0	11 9.0	ns
t_{PLH} Propagation Delay t_{PHL} $\overline{G}_n$ to $\overline{G}$	Waveform 2	3.0 3.0	8.3 5.7	10.5 7.5	3.0 3.0	12.5 9.5	3.0 3.0	11.5 8.5	ns
t_{PLH} Propagation Delay t_{PHL} $\overline{P}_n$ to $\overline{P}$	Waveform 2	3.0 2.5	5.7 4.1	7.5 5.5	3.0 2.5	11 7.5	3.0 2.5	8.5 6.5	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

64-BIT RANDOM ACCESS MEMORY (RAM) FAST 54/74F189

Preview

64-Bit Random Access Memory (3-State)

- **3-State outputs for data bus applications**
- **Buffered inputs minimize loading**
- **Address decoding on-chip**
- **Diode clamped inputs minimize ringing**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F189		37mA

DESCRIPTION

The 'F189 is a high-speed, 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-State and are in the high-impedance state whenever the Chip Select (CS) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F189N	
Plastic SO	N74F189D	
Ceramic DIP		
Ceramic LLCC		

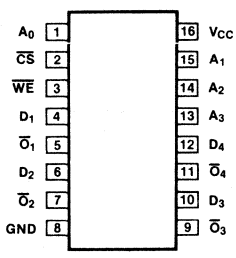
NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

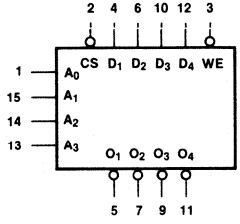
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A_0-A_3	Address Inputs	1.0/1.0	20μA/0.6mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/2.0	20μA/1.2mA
$\overline{WE}$	Write Enable Input (Active LOW)	1.0/2.0	20μA/1.2mA
D_1-D_4	Data Inputs	1.0/1.0	20μA/0.6mA
O_1-O_4	Inverted Data Outputs	50/33.3	1mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION

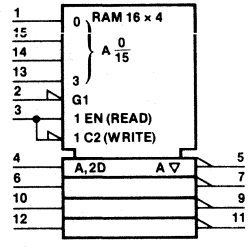


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)



64-BIT RANDOM ACCESS MEMORY (RAM) FAST 54/74F189

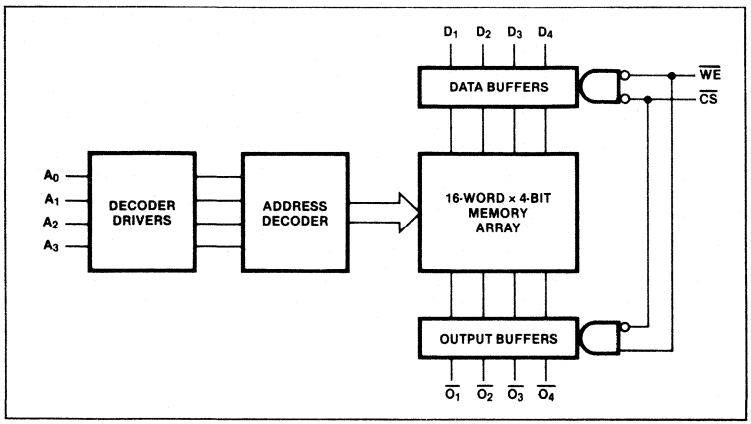
Preview

FUNCTIONAL TABLE

INPUTS		OPERATION	CONDITION OF OUTPUTS
$\overline{CS}$	$\overline{WE}$		
L	L	Write	High impedance
L	H	Read	Complement of stored data
H	X	Inhibit	High impedance

H = HIGH voltage level
L = LOW voltage level
X = Don't care

LOGIC DIAGRAM



5

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +55	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−3.0	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

64-BIT RANDOM ACCESS MEMORY (RAM) FAST 54/74F189

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F189 Min	54/74F189 Typ[2]	54/74F189 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.4	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V			2	50	μA
I_{OZL}	Off-state output current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, $\overline{WE}$, $\overline{CS}$ = GND			37	55	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Access time, HIGH or LOW	Waveform 2	11		26			11	27	ns
t_{PHL}	A_n to $\overline{O}_n$		8.0		19			8.0	20	
t_{PZH}	Access time, HIGH or LOW	Waveforms 3 & 4	3.5		8.5			3.5	9.5	ns
t_{PZL}	$\overline{CS}$ to $\overline{O}_n$		5.0		13			5.0	1.4	
t_{PHZ}	Disable time, HIGH or LOW	Waveforms 3 & 4	2.0		6.0			2.0	7.0	ns
t_{PLZ}	$\overline{CS}$ to $\overline{O}_n$		3.0		8.0			3.0	9.0	
t_{PZH}	Write recovery time, HIGH or LOW	Waveforms 3 & 4	12		28			12	29	ns
t_{PZL}	$\overline{WE}$ to $\overline{O}_n$		6.5		15.5			6.5	16.5	
t_{PHZ}	Disable time, HIGH or LOW	Waveforms 3 & 4	4.0		10			4.0	11	ns
t_{PLZ}	$\overline{WE}$ to $\overline{O}_n$		5.0		13			5.0	14	

NOTE
Subtract 0.2ns from minimum values for SO package.

64-BIT RANDOM ACCESS MEMORY (RAM) FAST 54/74F189

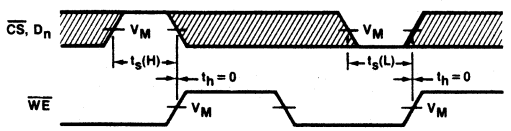
Preview

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW A_n to $\overline{WE}$	Waveform 2	0 0					0 0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW A_n to $\overline{WE}$	Waveform 2	0 0					0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW D_n to $\overline{WE}$	Waveform 1	10 10					10 10		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to $\overline{WE}$	Waveform 1	0 0					0 0		ns
$t_s(L)$	Setup time, LOW, $\overline{CS}$ to $\overline{WE}$	Waveform 1	6.0					6.0		ns
$t_h(L)$	Hold time, LOW, $\overline{CS}$ to $\overline{WE}$	Waveform 1	6.0					6.0		ns
$t_W(L)$	$\overline{WE}$ pulse width, LOW	Waveform 2	6.0					6.0		ns

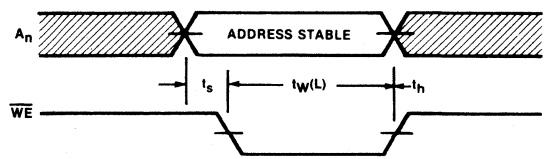
AC WAVEFORMS

DATA SETUP AND HOLD TIMES



Waveform 1

ADDRESS SETUP AND HOLD TIMES

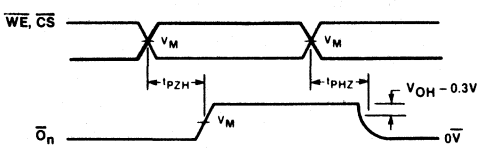


Waveform 2

$V_M = 1.5V$

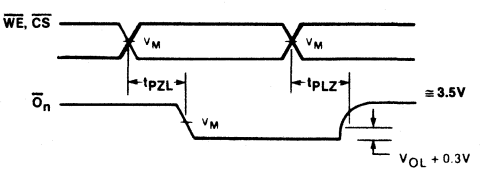
The shaded areas indicate when the input is permitted to change for predictable output performance.

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

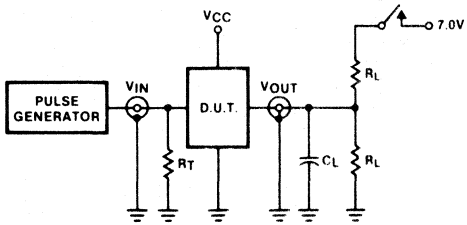
5

64-BIT RANDOM ACCESS MEMORY (RAM) FAST 54/74F189

Preview

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



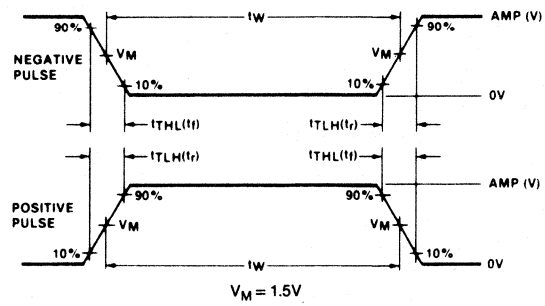
SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Preview

'F190 Asynchronous Presettable BCD/Decade Up/Down Counter
'F191 Asynchronous Presettable 4-Bit Binary Up/Down Counter

- **High speed — 110MHz typical f_{MAX}**
- **Synchronous, reversible counting**
- **BCD/decade — 'F190 4-bit binary — 'F191**
- **Asynchronous parallel load capability**
- **Count enable control for synchronous expansion**
- **Single up/down control input**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F190		38mA
74F191		38mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F190N • N74F191N	
Plastic SO	N74F190D • N74F191D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F190 is an asynchronously presettable up/down BCD decade counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation. The 'F191 is similar, but is a 4-bit binary counter.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs (D_0–D_3) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is LOW. As indicated in the Mode Select Table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the Count Enable ($\overline{CE}$) input. When $\overline{CE}$ is LOW, internal state changes are initiated.

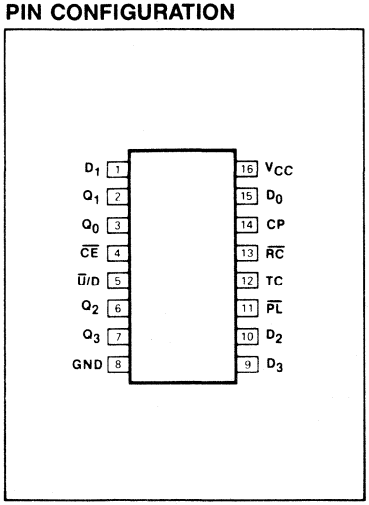
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{CE}$	Count enable input (active low)	1.0/3.0	20μA/1.8mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
D_0–D_3	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{PL}$	Asynchronous parallel load input (active low)	1.0/1.0	20μA/0.6mA
$\overline{U}$/D	Up/down count control input	1.0/1.0	20μA/0.6mA
Q_0–Q_3	Flip-flop outputs	50/33	1.0mA/20μA
$\overline{RC}$	Ripple clock output (active low)	50/33	1.0mA/20μA
TC	Terminal count output (active high)	50/33	1.0mA/20μA

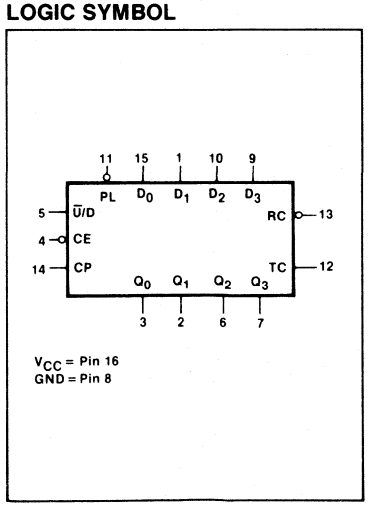
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

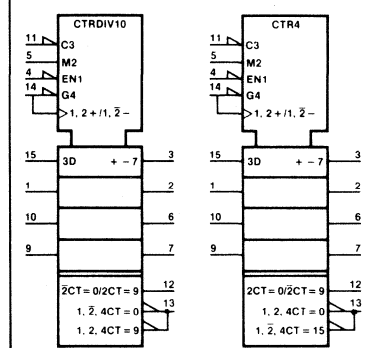
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Preview

Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "9" in the count-up mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes.

The TC signal is used internally to enable the $\overline{RC}$ output. When TC is HIGH and $\overline{CE}$ is LOW, the RC follows the Clock Pulse (CP) delayed by two gate delays. The $\overline{RC}$ output essentially duplicates the LOW clock pulse width, although delayed in time by two gate delays. This feature simplifies the design of multistage counters, as indicated in Figures A and B. In Figure A, each $\overline{RC}$ output is used as the Clock input for the next higher stage. When the clock source has a limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure B shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The LOW state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH, there is no such restriction on the HIGH state duration of the clock.

In Figure C, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own $\overline{CE}$, therefore, the simple inhibit scheme of Figure A and B does not apply.

N-STAGE COUNTER USING RIPPLE CLOCK

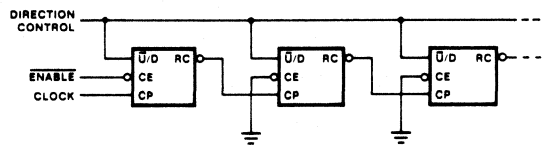


Figure A

SYNCHRONOUS N-STAGE COUNTER USING RIPPLE CARRY/BORROW

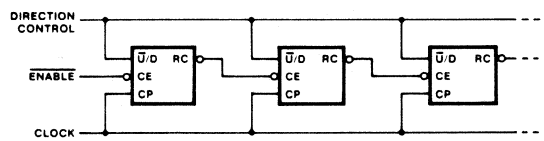


Figure B

SYNCHRONOUS N-STAGE COUNTER WITH PARALLEL GATED CARRY/BORROW

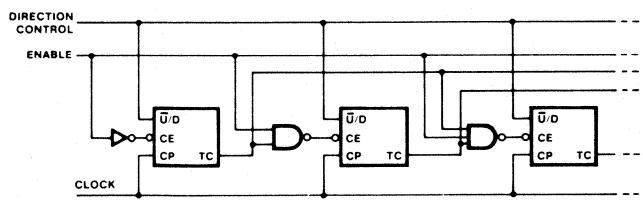
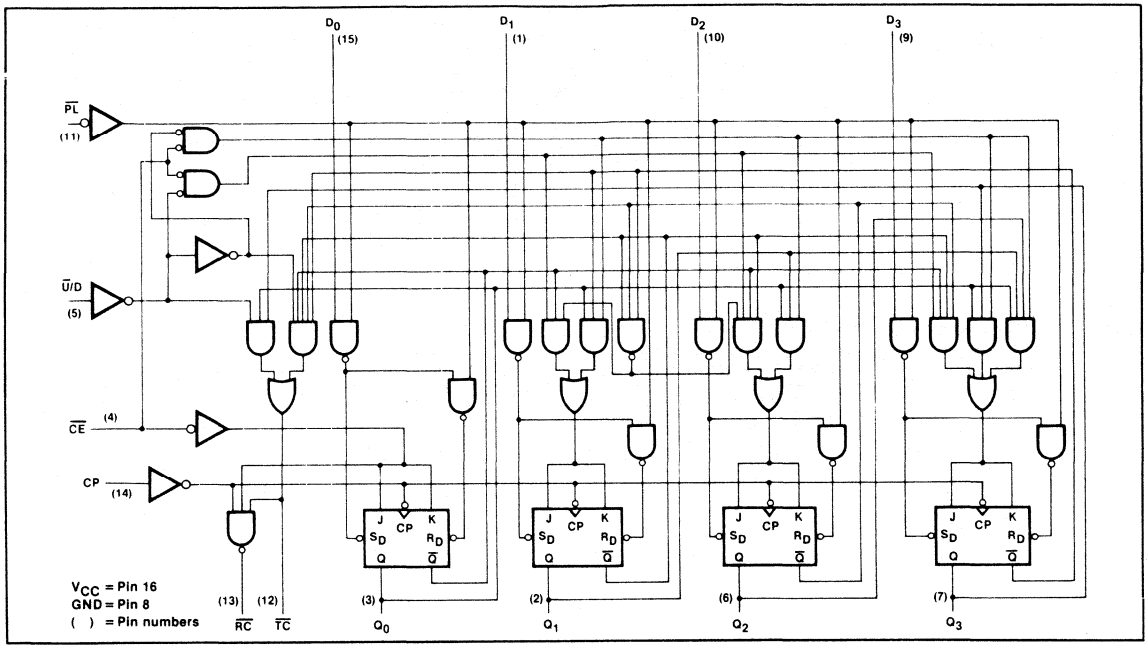


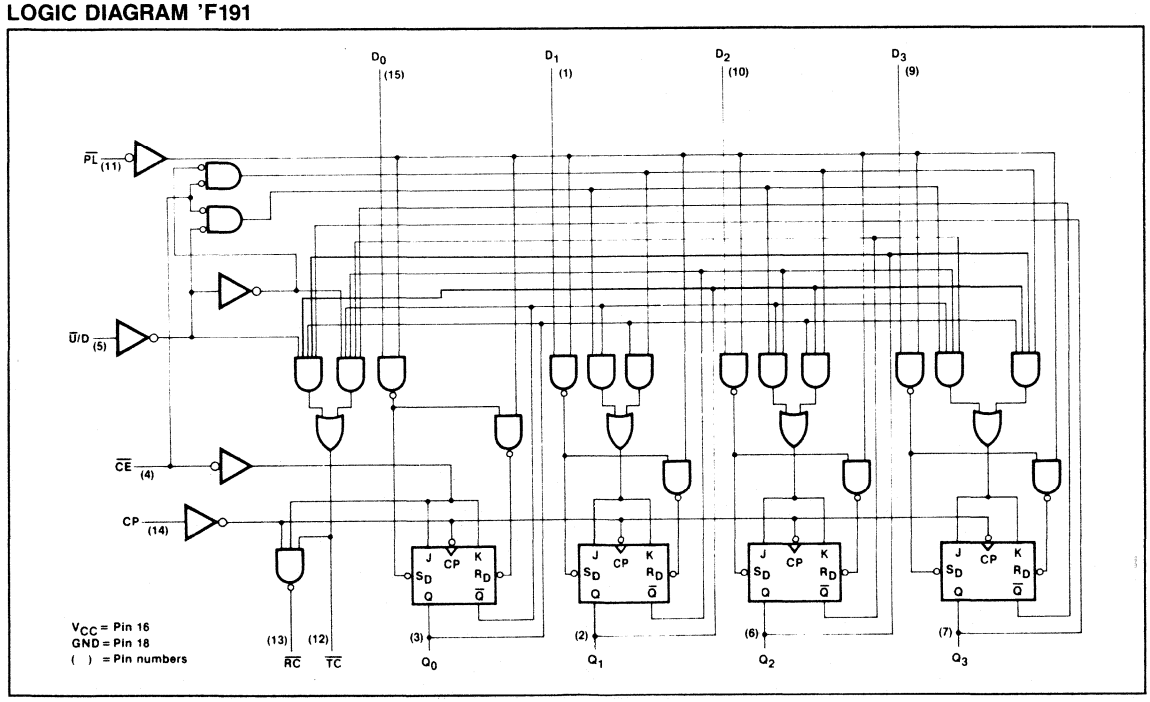
Figure C

Preview

LOGIC DIAGRAM 'F190



LOGIC DIAGRAM 'F191



5

COUNTERS

FAST 54/74F190, 54/74F191

Preview

MODE SELECT — FUNCTION TABLE, 'F190, 'F191

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}$/D	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
Count up	H	L	l	↑	X	count up
Count down	H	H	l	↑	X	count down
Hold "do nothing"	H	X	H	X	X	no change

TC AND $\overline{RC}$ FUNCTION TABLE, 'F190

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}$/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⊓	H	X	X	H	↓	⊓
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓	L	L	L	L	↓	⊓

TC AND $\overline{RC}$ FUNCTION TABLE, 'F191

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}$/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊓	H	H	H	H	↓	⊓
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓	L	L	L	L	↓	⊓

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.
⊓ = LOW pulse.
↓ = HIGH-to-LOW clock transition

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

Preview

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	– 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F190, 191			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MIN, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			– 0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V	CE input			0.3	mA
			Other inputs			0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V	CE input			60	μA
			Other inputs			20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	CE input			–1.8	mA
			Other inputs			–0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			38	55	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.

Preview

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum input count frequency	Waveform 1	100					90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.0 5.0		7.5 11.0			3.0 5.0	8.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$	Waveform 2	3.0 3.0		7.5 7.0			3.0 3.0	8.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	Waveform 1	6.0 5.0		13.0 11.0			6.0 5.0	14.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$	Waveform 7	7.0 5.5		18.0 12.0			7.0 5.5	20.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC	Waveform 7	4.0 4.0		10.0 10.0			4.0 4.0	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 3	3.0 6.0		7.0 13.0			3.0 6.0	8.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to any output	Waveform 4	5.0 5.5		11.0 12.0			5.0 5.5	12.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$	Waveform 2	3.0 3.0		7.0 7.0			3.0 3.0	8.0 8.0	ns

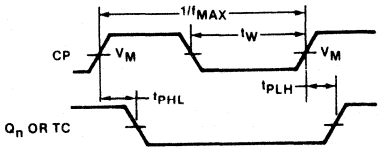
NOTE
Subtract 0.2ns from minimum values for SO package.

AC SETUP REQUIREMENTS

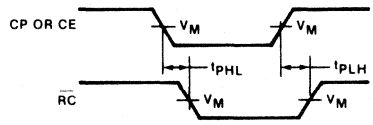
PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW D_n to $\overline{PL}$	Waveform 6	6.0 6.0					6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to $\overline{PL}$	Waveform 6	4.0 4.0					4.0 4.0		ns
$t_s(L)$	Setup time LOW $\overline{CE}$ to CP	Waveform 8	10.0					10.0		ns
$t_h(L)$	Hold time LOW $\overline{CE}$ to CP	Waveform 8	0					0		ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW $\overline{U}$/D to CP	Waveform 7	12 12					12 12		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{U}$/D to CP	Waveform 7	0 0					0 0		ns
$t_W(L)$	$\overline{PL}$ pulse width, LOW	Waveform 4	6.0					6.0		ns
$t_W(L)$	CP pulse width, LOW	Waveform 1	5.0					5.0		ns
t_{rec}	Recovery time, $\overline{PL}$ to CP	Waveform 5	6.0					6.0		ns

Preview

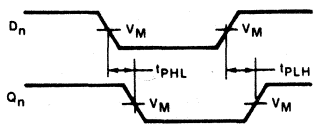
AC WAVEFORMS



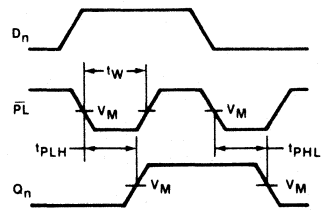
Waveform 1



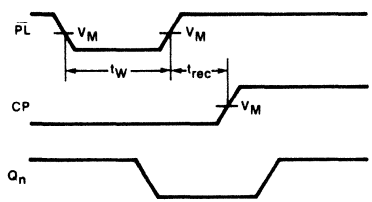
Waveform 2



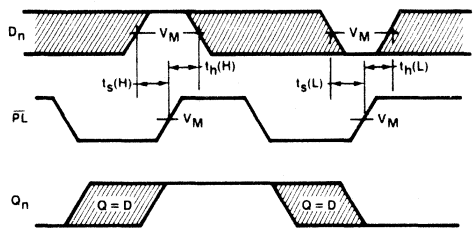
Waveform 3



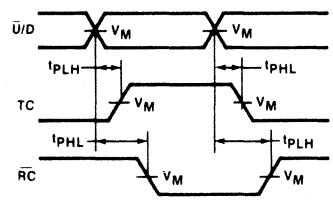
Waveform 4



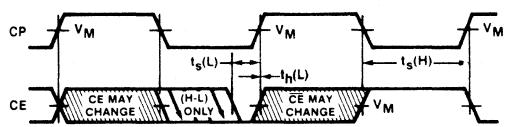
Waveform 5



Waveform 6



Waveform 7



Waveform 8

V_M = 1.5V

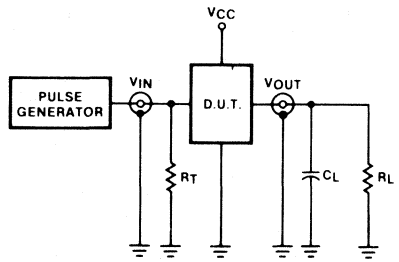
The shaded areas indicate when the input is permitted to change for predictable output performance.

5

Preview

TEST CIRCUITS AND WAVEFORMS

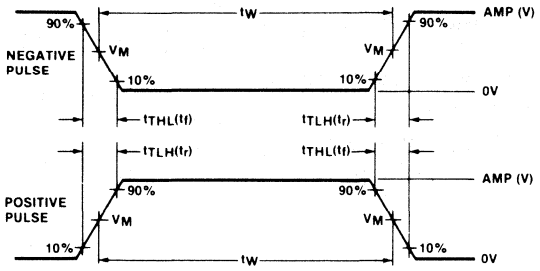
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Preview

'F192 — Synchronous Presettable BCD Decade Up/Down Counter
'F193 — Synchronous Presettable 4-Bit Binary Up/Down Counter

- **Synchronous reversible 4-bit binary counting**
- **Asynchronous parallel load**
- **Asynchronous reset (clear)**
- **Expandable without external logic**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F192	125MHz	30mA
74F193	125MHz	30mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F192N • N74F193N	
Plastic SO	N74F192D • N74F193D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F192 and 'F193 are 4-bit synchronous up/down counters — the 'F192 counts in BCD mode and the 'F193 counts in the binary mode. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either Clock input. If the CP_U clock is pulsed while CP_D is held HIGH, the device will count up . . . if CP_D is pulsed while CP_U is held HIGH, the device will count down. Only one Clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous reset pin — it may also be loaded in parallel by activating the asynchronous parallel load pin.

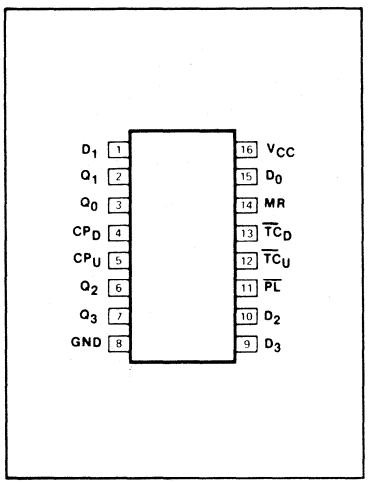
Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

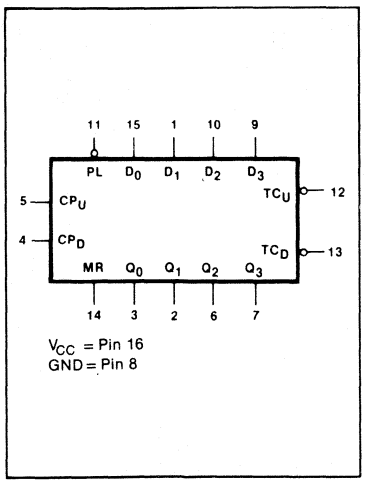
PINS	DESCRIPTION	54F/74F (U.L.) High/Low	LOAD VALUE High/Low
CP_U	Count up clock input (active rising edge)	1.0/2.0	20μA/1.2mA
CP_D	Count down clock input (active rising edge)	1.0/2.0	20μA/1.2mA
MR	Asynchronous master reset input (active high)	1.0/1.0	20μA/0.6mA
$\overline{PL}$	Asynchronous parallel load input (active low)	1.0/1.0	20μA/0.6mA
D_0–D_3	Parallel data inputs	1.0/1.0	20μA/0.6mA
Q_0–Q_3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}_D$	Terminal count down (borrow) output (active low)	50/33	1.0mA/20mA
$\overline{TC}_U$	Terminal count up (carry) output (active low)	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

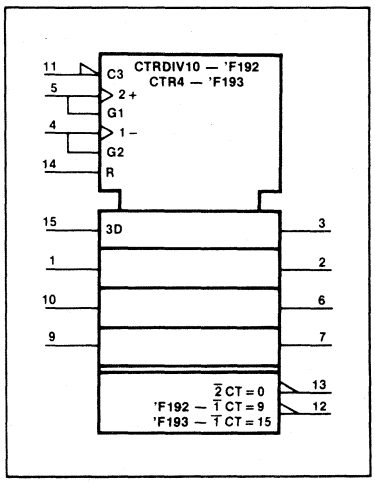
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



COUNTERS

FAST 54/74F192, 54/74F193

Preview

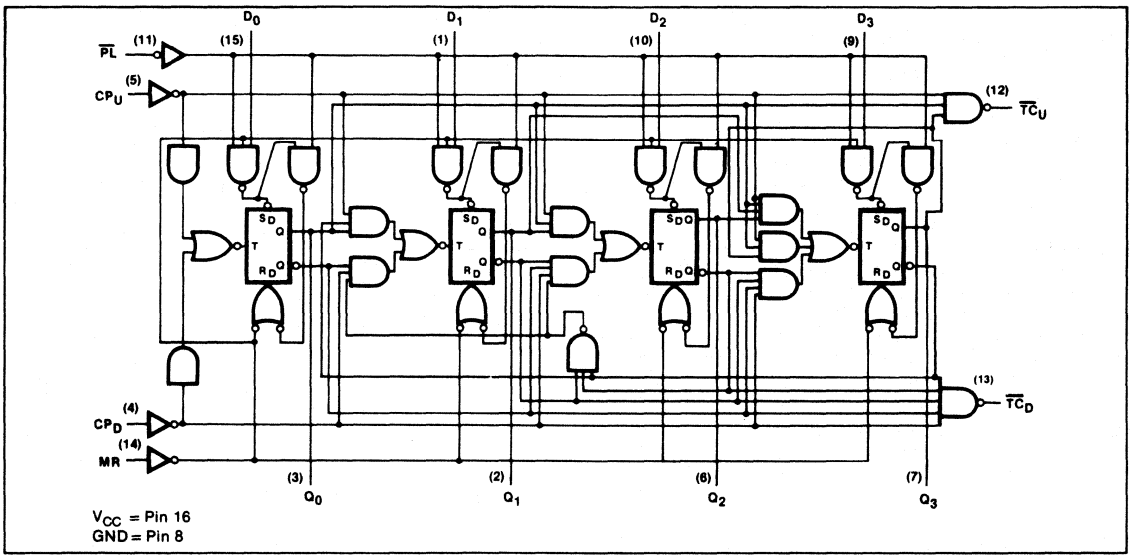
Each flop-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

One clock should be held HIGH while counting with the other, because the circuit will either count by twos or not at all, depending on the state of the first flip-flop which cannot toggle as long as either Clock input is LOW.

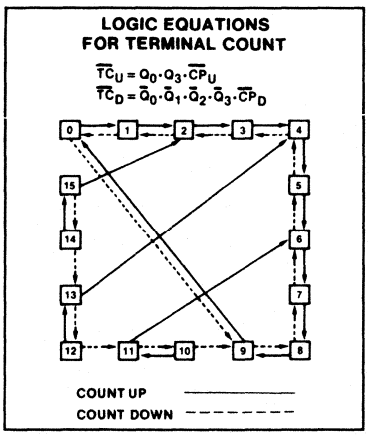
Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state of 9 (for the 'F192 and 15 for the 'F193), the next HIGH-to-LOW transition of CP_U will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, duplicating the count up clock, although delayed by two gate delays. Likewise, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The $\overline{TC}$ outputs can be used as the Clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not

LOGIC DIAGRAM, 'F192



STATE DIAGRAM, 'F192



MODE SELECT — FUNCTION TABLE, 'F192

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	X	X	H	$Q_n = D_n$				L	H
	L	L	H	X	H	X	X	H	$Q_n = D_n$				H	H
Count up	L	H	↑	H	X	X	X	X	Count up				H[a]	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	H[b]

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition

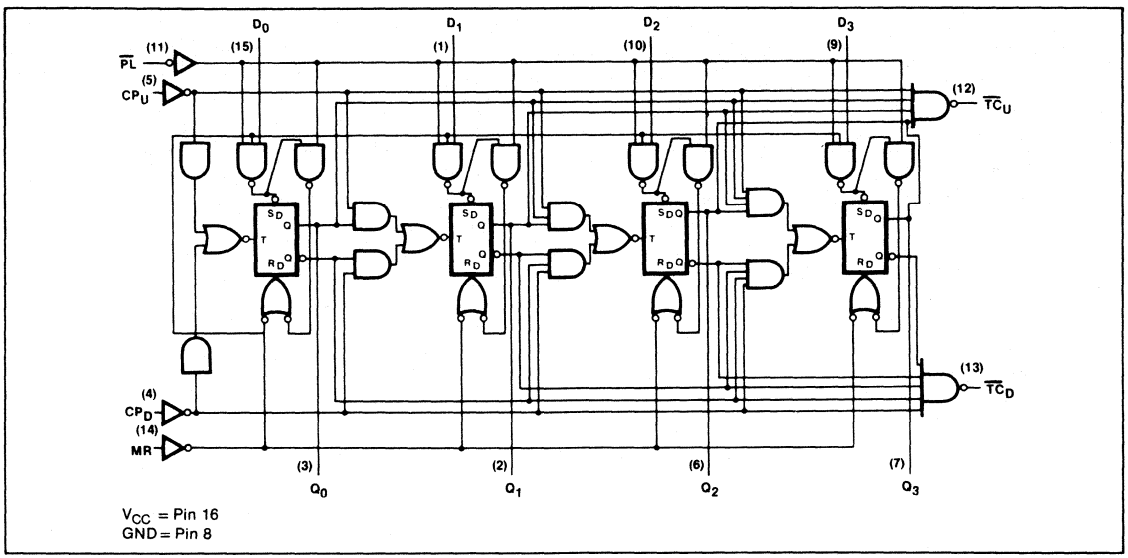
NOTES
a. $\overline{TC}_U = CP_U$ at terminal count up (HLLH).
b. $\overline{TC}_D = CP_D$ at terminal count down (LLLL).

Preview

be fully synchronous, since there is a two-gate delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs (D_0–D_3) is loaded into the counter and appears on the outputs regardless of the conditions of the Clock inputs when the Parallel Load ($\overline{PL}$) input is LOW. A HIGH level on the Master Reset (MR) input will disable the parallel load gates, override both Clock inputs, and set all Q outputs LOW. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

LOGIC DIAGRAM, 'F193

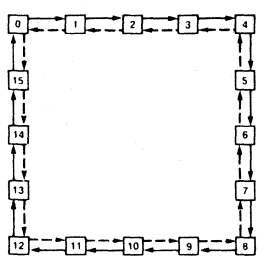


STATE DIAGRAM, 'F193

LOGIC EQUATIONS FOR TERMINAL COUNT

$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$

$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$



MODE SELECT — FUNCTION TABLE, 'F193

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
Reset clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
Count up	L	H	↑	H	X	X	X	X	Count up				$H^{(c)}$	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	$H^{(d)}$

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition.

NOTES
c. $TC_U = CP_U$ at terminal count up (HHHH).
d. $TC_D = CP_D$ at terminal count down (LLLL).

Preview

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F193 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F193 T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F193 T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum count frequency	Waveform 1	100	125				90		MHz
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to $\overline{TC}_U$	Waveform 1	4.0 3.5	7.0 6.0	9.0 8.0			4.0 3.5	10 9.0	ns
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to Q_n	Waveform 1	4.0 5.5	6.5 9.5	8.5 12.5			4.0 5.5	9.5 13.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 2	3.0 6.0	4.5 11	7.0 14.5			3.0 6.0	8.0 15.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n	Waveform 2	5.0 5.5	8.5 10	11 13			5.0 5.5	12 14	ns
t_{PHL}	Propagation delay MR to Q_n	Waveform 3	6.5	11	14.5			6.5	15.5	ns
t_{PLH}	Propagation delay MR to $\overline{TC}_U$	Waveform 3	6.0	10.5	13.5			6.0	14.5	ns
t_{PHL}	Propagation delay MR to $\overline{TC}_D$	Waveform 3	6.0	10.5	13.5			6.0	14.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 2	7.0 7.0	12 11.5	15.5 14.5			7.0 7.0	16.5 15.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 2	7.0 6.5	11.5 11	14.5 14			7.0 6.5	15.5 15	ns

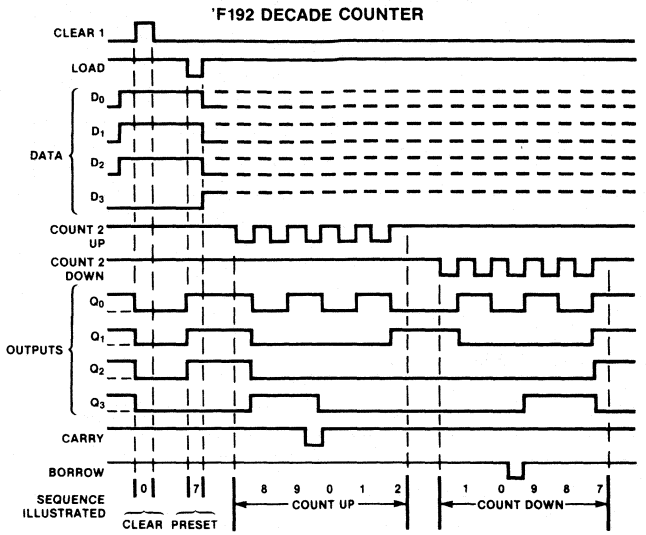
NOTE
Subtract 0.2ns from minimum values for SO package.

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW D_n to $\overline{PL}$	Waveform 4	6.0 6.0					6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to $\overline{PL}$	Waveform 4	4.0 4.0					4.0 4.0		ns
$t_W(L)$	$\overline{PL}$ pulse width LOW	Waveform 2	6.0					6.0		ns
$t_W(L)$	CP_U or CP_D pulse width LOW	Waveform 1	5.0					5.0		ns
$t_W(L)$	CP_U or CP_D pulse width LOW (change of direction)	Waveform 1	10					10		ns
$t_W(H)$	MR pulse width HIGH	Waveform 3	6.0					6.0		ns
t_{rec}	Recovery time $\overline{PL}$ to CP_U or CP_D	Waveform 2	6.0					6.0		ns
t_{rec}	Recovery time MR to CP_U or CP_D	Waveform 3	4.0					4.0		ns

Preview

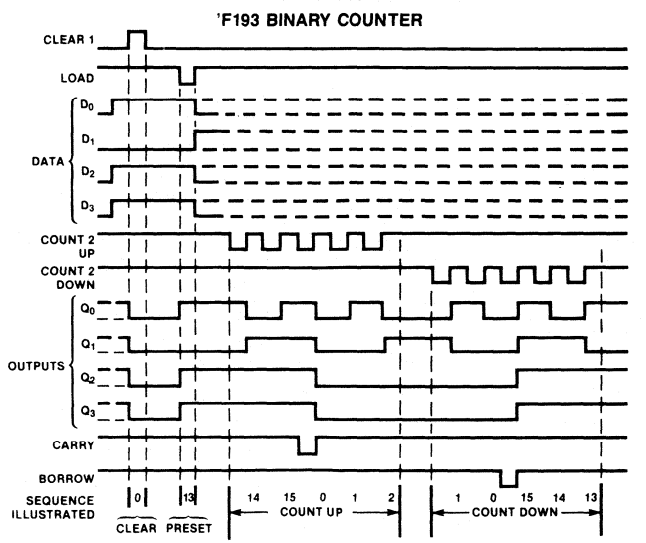
FUNCTIONAL WAVEFORMS (Typical clear, load, and count sequences)



NOTES
1. Clear overrides load data and count inputs.
2. When counting up, count-down input must be high; when counting down, count-up input must be high.

5

FUNCTIONAL WAVEFORMS (Typical clear, load, and count sequences)



NOTES
1. Clear overrides load data and count inputs.
2. When counting up, count-down input must be high; when counting down, count-up input must be high.

Preview

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

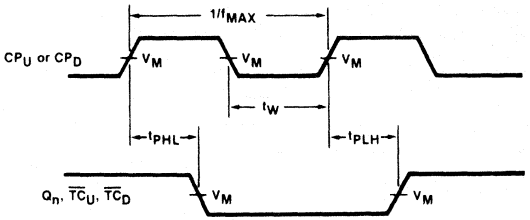
PARAMETER		TEST CONDITONS[1]		54/74F192, 'F193			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	CP_U, CP_D			−1.2	mA
			Other inputs		−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			30	45	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with parallel load and Master Reset inputs grounded, all other inputs at 4.5V and all outputs open.

Preview

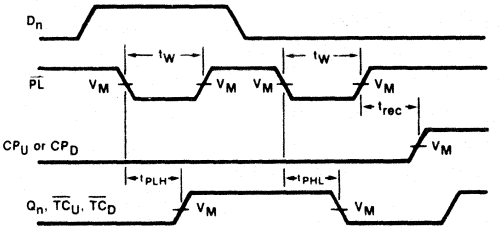
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



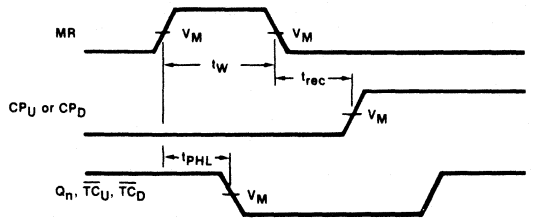
Waveform 1

PARALLEL LOAD PULSE WIDTH, PARALLEL LOAD TO OUTPUT DELAYS, AND PARALLEL LOAD TO CLOCK RECOVERY TIME



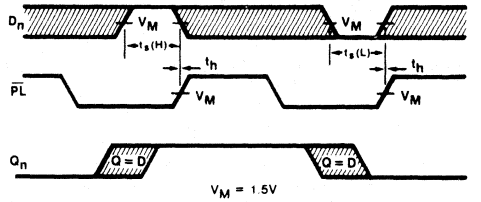
Waveform 2

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY & MASTER RESET TO CLOCK RECOVERY TIME



Waveform 3

SETUP AND HOLD TIMES DATA TO PARALLEL LOAD (PL)



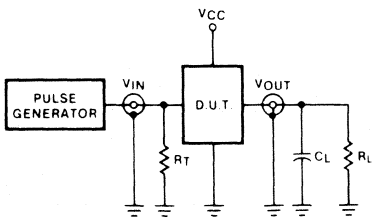
VM = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



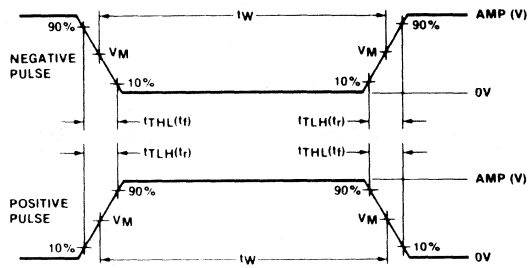
DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



VM = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

SHIFT REGISTER — FAST 54/74F194

4-Bit Bidirectional Universal Shift Register

- **Shift left and shift right capability**
- **Synchronous parallel and serial data transfers**
- **Easily expanded for both serial and parallel operation**
- **Asynchronous Master Reset**
- **Hold (do nothing) mode**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F194	150MHz	33mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F194N	
Plastic SO	N74F194D	
Ceramic DIP		S54F194F
Ceramic LLCC		S54F194G

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
D_0-D_3	Parallel Data Inputs	1.0/1.0	20μA/0.6mA
S_0, S_1	Mode Control Inputs	1.0/1.0	20μA/0.6mA
D_{SR}	Serial Data Input (Shift Right)	1.0/1.0	20μA/0.6mA
D_{SL}	Serial Data Input (Shift Left)	1.0/1.0	20μA0.6mA
C_P	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
MR	Asynchronous Master Reset (Active LOW)	1.0/1.0	20μA/0.6mA
Q_0-Q_3	Parallel Outputs	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

DESCRIPTION

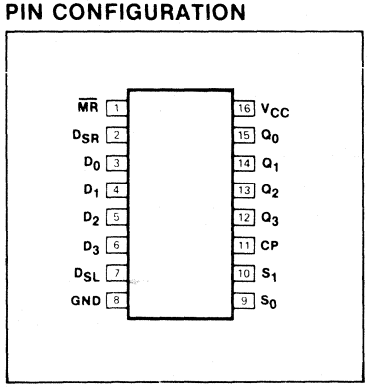
The functional characteristics of the 'F194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 9ns (typical) for 54/74F, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

The 'F194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S_0 and S_1. As shown in the Mode Select Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.), or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are LOW, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

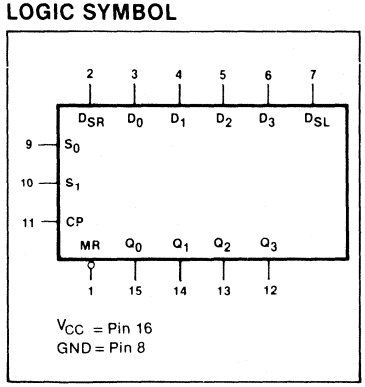
Mode Select and Data inputs on the 'F194 are edge-triggered, responding only to the LOW-to-HIGH transition of the Clock (CP). Therefore, the only timing restriction is that the Mode Control and selected Data inputs must be stable one setup time prior to the positive transition of the clock pulse. Signals on the Select, Parallel Data (D_0-D_3) and Serial Data (D_{SR}, D_{SL}) inputs can change when the clock is in either state, provided only the recommended setup and hold times, with respect to the clock rising edge, are observed.

The four Parallel Data inputs (D_0-D_3) are D-type inputs. Data appearing on D_0-D_3 inputs when S_0 and S_1 are HIGH is transferred to the Q_0-Q_3 outputs respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous Master Reset (MR) overrides all other input conditions and forces the Q outputs LOW.

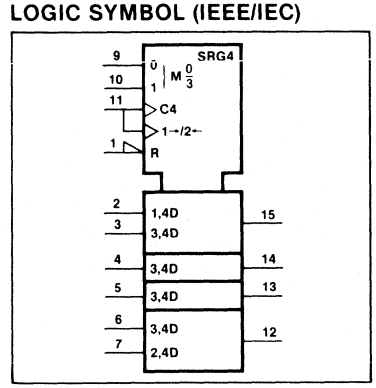
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

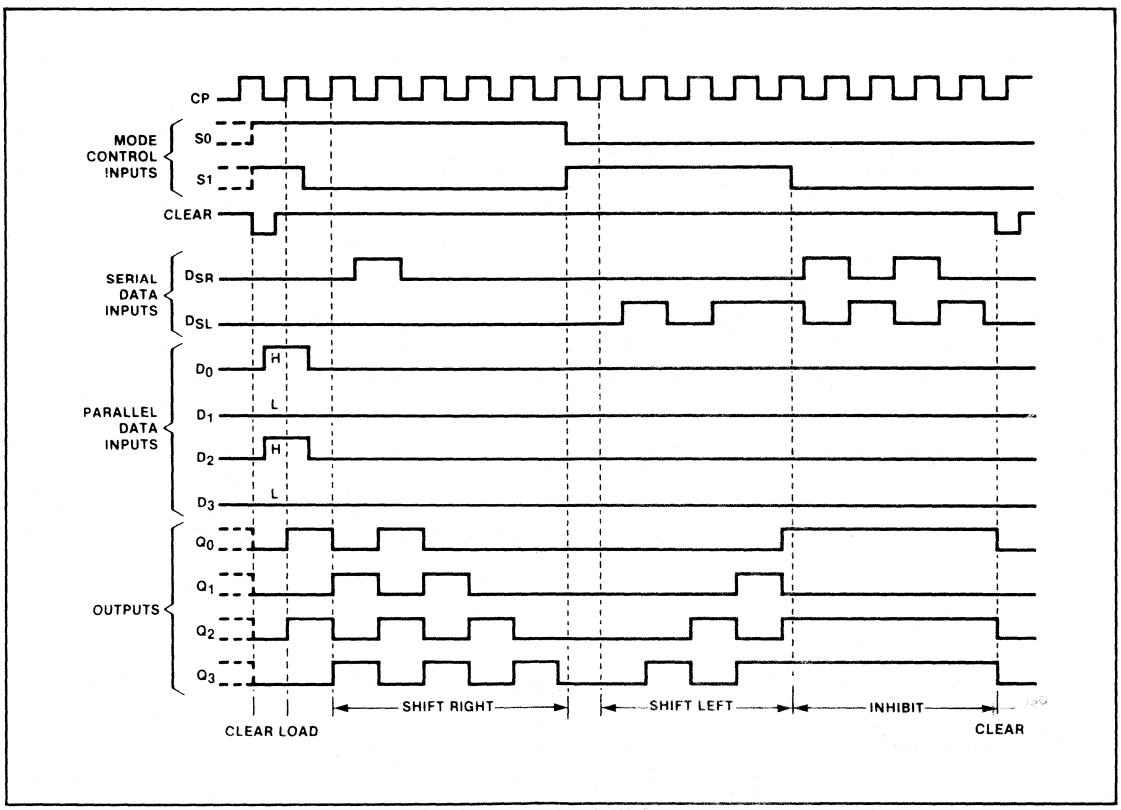


MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	↑	H	h	l	X	l	X	q_1	q_2	q_3	L
	↑	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	↑	H	l	h	l	X	X	L	q_0	q_1	q_2
	↑	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	↑	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3

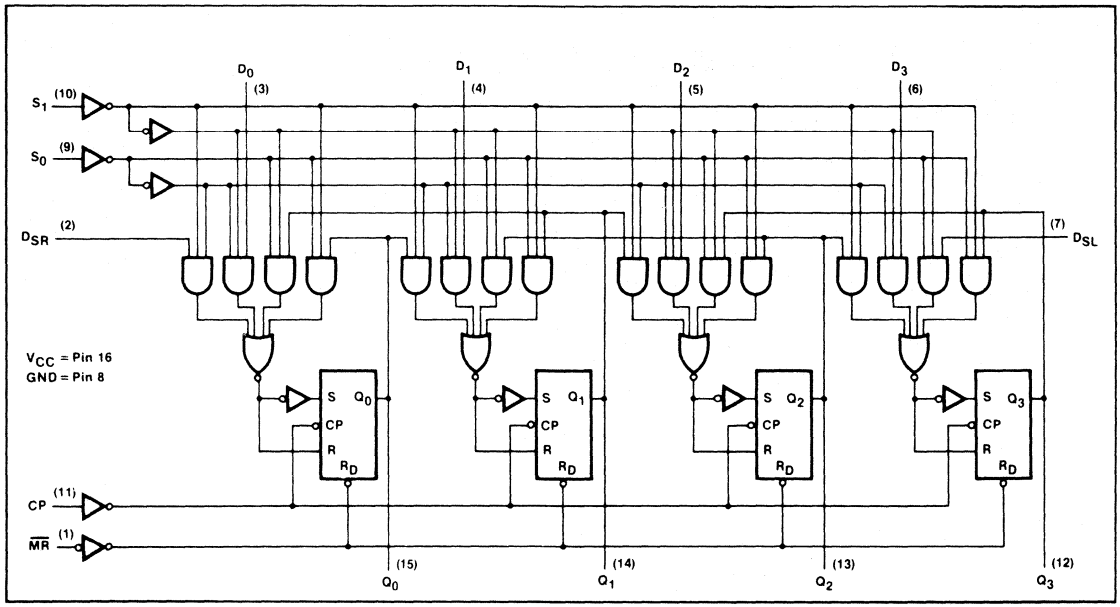
H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT AND CLEAR SEQUENCES



5

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F194			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage[3]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				− 0.73	− 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = + 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				− 0.4	− 0.6	mA
I_{OS}	Short-circuit output current[4]	V_{CC} = MAX, V_O = 0.0V			− 60	− 90	− 150	mA
I_{CC}	Supply current[5] (total)	V_{CC} = MAX				33	46	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Output HIGH state will change to LOW state if an external voltage of less than 0.0V is applied.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. With all outputs open, D_i inputs grounded and 4.5V applied to S_0, S_1, MR and the serial inputs. I_{CC} is tested with a momentary ground, then 4.5V applied to CP.

5

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F			54F		74F		UNIT
			T_A = + 25°C, V_{CC} = + 5.0V, C_L = 50pF, R_L = 500Ω			T_A, V_{CC} = Mil, C_L = 50pF, R_L = 500Ω		T_A, V_{CC} = Com'l, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	105	150		90		90		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1	3.5 3.5	5.2 5.5	7.0 7.0	3.0 3.0	9.8 8.5	3.5 3.5	8.0 8.0	ns
t_{PHL}	Propagation delay MR to output	Waveform 2	4.5	8.6	12	4.5	14.5	4.5	14	ns

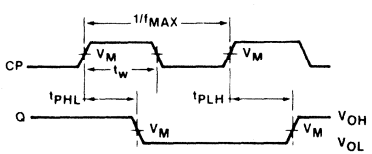
NOTE
Subtract 0.2ns from minimum values for SO package.

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			54F T_A, V_{CC} = Mil, $C_L = 50pF$, $R_L = 500\Omega$		74F T_A, V_{CC} = Com'l, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_w(H)$	Clock pulse width HIGH	Waveform 1	5.0			5.5		5.5		ns
$t_w(L)$	MR pulse width, LOW	Waveform 2	5.0			5.0		5.0		ns
$t_s(H)$ $t_s(L)$	Setup time, D_0-D_3 to clock, D_{SR}, D_{SL} to clock	Waveform 3	4.0 4.0			4.0 4.0		4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW, D_0-D_3 to clock, DSR, DSL to clock	Waveform 3	0 0			1.0 1.0		1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW, Sn to clock	Waveform 4	8.0 8.0			9.5 8.0		9.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW, Sn to clock	Waveform 4	0 0			0 0		0 0		ns
t_{rec}	Recovery time, MR to clock	Waveform 2	7.0			9.0		8.0		ns

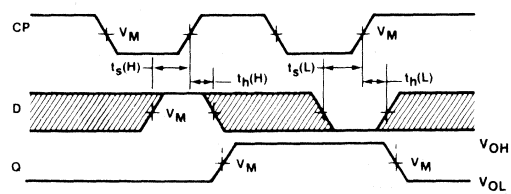
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

DATA SET-UP AND HOLD TIMES

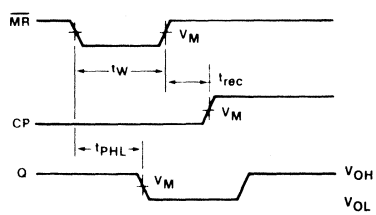


Waveform 3

$V_M = 1.5V$

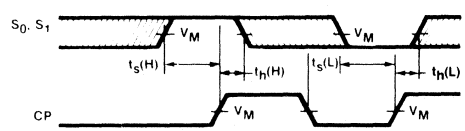
The shaded areas indicate when the input is permitted to change predictable output performance.

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY & MASTER RESET TO CLOCK RECOVERY TIME



Waveform 2

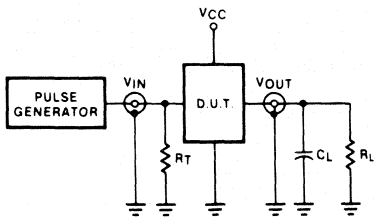
SETUP AND HOLD TIMES FOR S_0 AND S_1 INPUTS



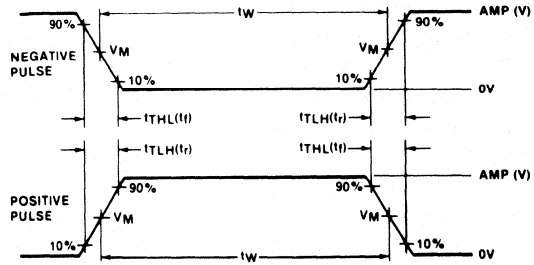
Waveform 4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

SHIFT REGISTER — FAST 54/74F195

Preliminary

4-Bit Parallel Access Shift Register

- High Impedance NPN base Inputs for reduced loading (20μA in LOW and HIGH states)
- Shift right and parallel load capability
- J-$\overline{K}$ (D) inputs to first stage
- Complement output from last stage
- Asynchronous Master Reset

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74F195	150 MHz	

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F195N	
Plastic SO	N74F195D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
CP	Clock Pulse Input (Active Rising Edge)	1.0/.033	20μA/20μA
D_0–D_3	Parallel Data Inputs	1.0/.033	20μA/20μA
$\overline{PE}$	Parallel Enable Input	1.0/.033	20μA/20μA
$\overline{MR}$	Asynchronous Master Reset	1.0/.033	20μA/20μA
J, $\overline{K}$	J-$\overline{K}$ or D Type Serial Inputs	1.0/.033	20μA/20μA
Q_0–Q_3, $\overline{Q}_3$	Outputs	50/33	1.0 mA/20 mA

NOTE
One (1.0) FAST Unit Load is defined as: 20 μA in the HIGH state and 0.6 mA in the LOW state.

DESCRIPTION

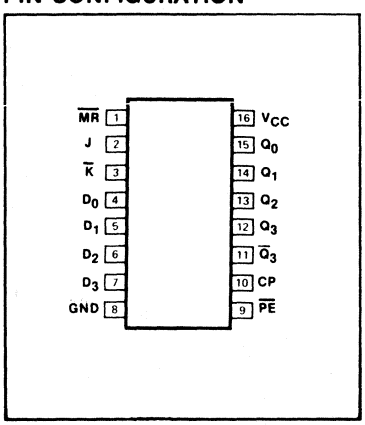
The functional characteristics of the 'F195 4-Bit Parallel Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

The 'F195 operates on two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is HIGH, and is shifted 1 bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The J and $\overline{K}$ inputs provide the flexibility of the JK type input for special applications and, by tying the two pins together, the simple D type input for general applications. The device appears as four common clocked D flip-flops when the $\overline{PE}$ input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs (D_0–D_3) is transferred to the respective Q_0–Q_3 outputs. Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the $\overline{PE}$ input low.

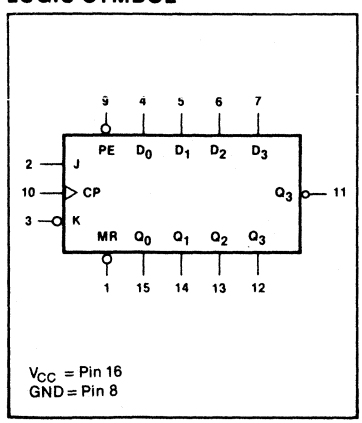
All parallel and serial data transfers are synchronous, occuring after each LOW-to-HIGH clock transition. The 'F195 utilizes edge-triggering, therefore, there is no restriction on the activity of the J, $\overline{K}$, D_n, and $\overline{PE}$ inputs for logic operation, other than the setup and release time requirements.

A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

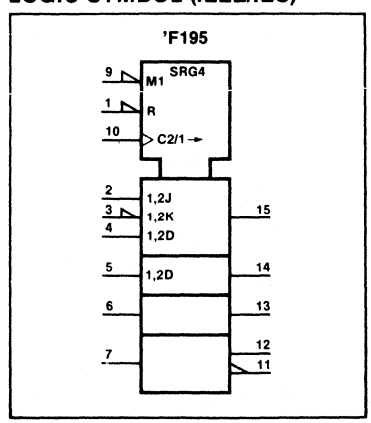
PIN CONFIGURATION



LOGIC SYMBOL



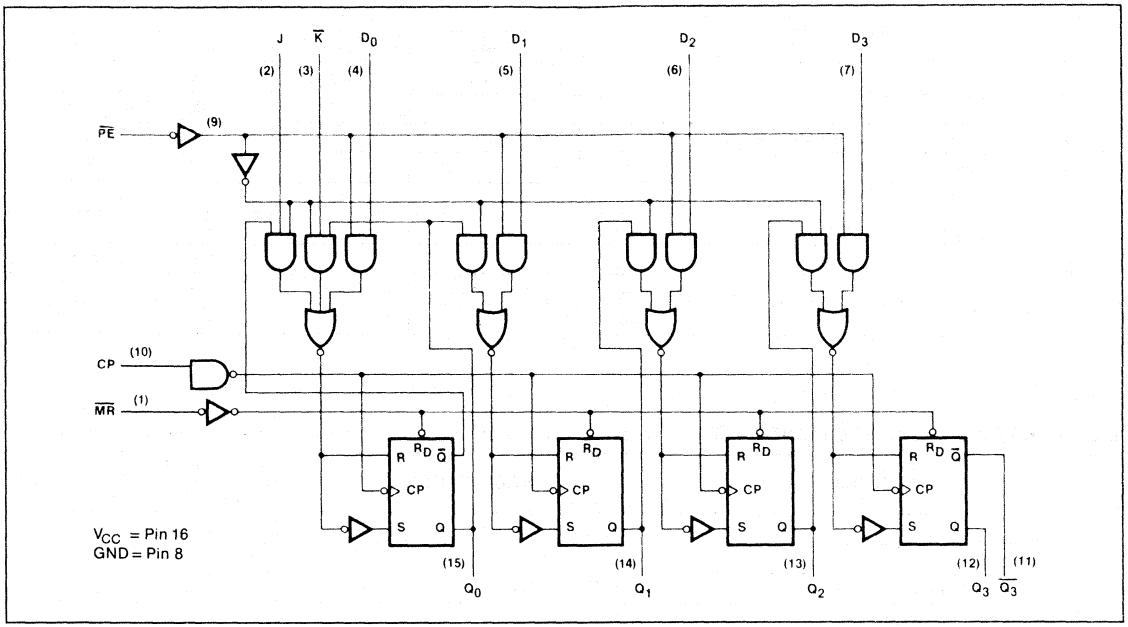
LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTER FAST 54/74F195

Preliminary

LOGIC DIAGRAM



5

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS				
	$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	↑	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	↑	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	↑	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	↑	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	↑	l	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d}_3$

H = HIGH voltage level.
L = LOW voltage level.
X = Don't care.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
d_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

SHIFT REGISTER — FAST 54/74F195

Preliminary

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	– 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F195			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 0.73	– 1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = + 7.0V					1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V					– 20	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 60	– 90	– 150	mA
I_{CC}	Power supply current[4]	V_{CC} = MAX						mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With all outputs open, $\overline{PE}$ grounded, and 4.5V applied to the J, $\overline{K}$, and Data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5V to $\overline{MR}$, and then a momentary ground, followed by 4.5V to clock.

Preliminary

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			54F T_A, V_{CC} = Mil, $C_L = 50pF$, $R_L = 500\Omega$		74F T_A, V_{CC} = Com'l, C_L = pF, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	105	150		90		90		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1	3.5 3.5	5.2 5.5	7.0 7.0	3.0 3.0	8.5 8.5	3.5 3.5	8.0 8.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 2	4.5	8.6	12	4.5	14.5	4.5	14	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			54F T_A, V_{CC} = Mil, $C_L = 50pF$, $R_L = 500\Omega$		74F T_A, V_{CC} = Com'l, C_L = pF, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_w	Clock pulse width HIGH	Waveform 1	5.0			5.5		5.5		ns
t_w	Master Reset pulse width LOW	Waveform 2	5.0			5.0		5.0		ns
t_s	Setup time, J, $\overline{K}$ and Data to Clock	Waveform 3	4.0			4.0		4.0		ns
t_h	Hold time, J, $\overline{K}$ and Data to Clock	Waveform 3	0			1.0		1.0		ns
t_s	Setup time, $\overline{PE}$ to CP	Waveform 4	8.0			8.0		8.0		ns
T_h	Hold time, $\overline{PE}$ to CP	Waveform 4	0			0		0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	7.0			9.0		8.0		ns

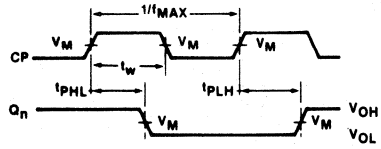
5

SHIFT REGISTER — FAST 54/74F195

Preliminary

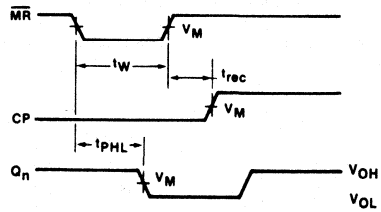
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



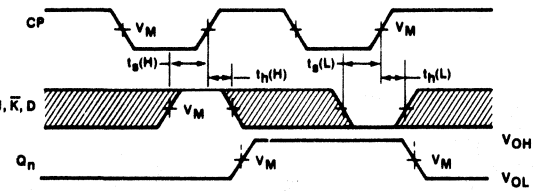
Waveform 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY & MASTER RESET TO CLOCK RECOVERY TIME



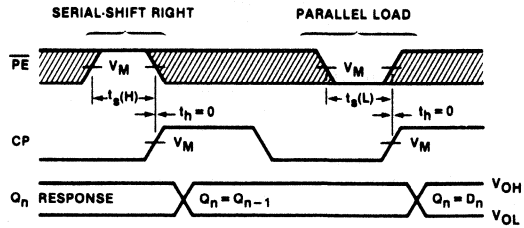
Waveform 2

DATA SET-UP AND HOLD TIMES



Waveform 3

SETUP AND HOLD TIMES PARALLEL ENABLE TO CLOCK



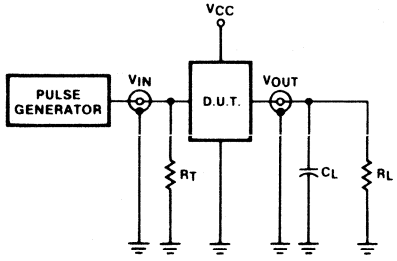
Waveform 4

V_M = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



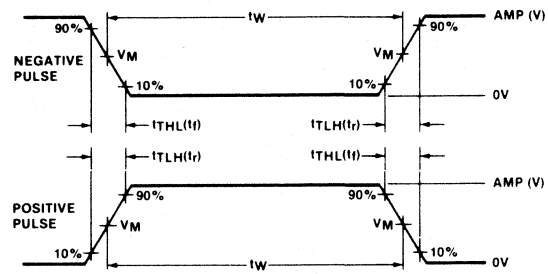
DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

SHIFT REGISTER FAST 54/74F198

8-Bit Bidirectional Universal Shift Register

DESCRIPTION

This bidirectional register is designed to incorporate virtually all of the features a system designer may want in a shift register. This circuit contains 87 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating mode control inputs, and a direct overriding clear line. The register has four distinct modes of operation:

- Parallel (broadside) Load
- Shift Right (in the direction Q_A toward Q_H)
- Shift Left (in the direction Q_H toward Q_A)
- Inhibit Clock (do nothing)

Synchronous parallel loading is accomplished by applying the 8 bits of data and taking both mode control inputs, S_0 and S_1, HIGH. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the Clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is HIGH and S_1 is LOW. Serial data for this mode is entered at the shift-right data input. When S_0 is LOW and S_1 is HIGH, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are LOW. The mode controls should be changed only while the Clock input is HIGH.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F198		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F198N	
Ceramic DIP		
Flatpack		S54F198W

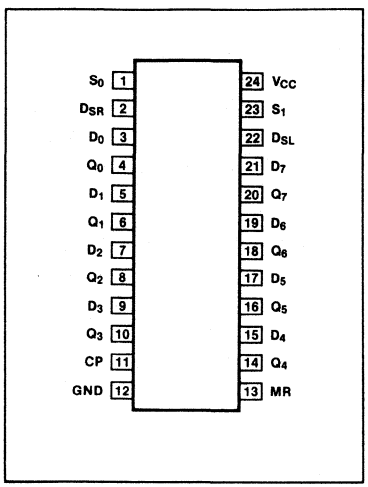
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
D_0-D_7	Parallel Data Inputs	1.0/1.0	20μA/0.6mA
S_0-S_1	Mode Control Inputs	1.0/1.0	20μA/0.6mA
D_{SR}	Serial Data Input (Shift Right)	1.0/1.0	20μA/0.6mA
D_{SL}	Serial Data Input (Shift Left)	1.0/1.0	20μA/0.6mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous Master Reset (Active LOW)	1.0/1.0	20μA/0.6mA
Q_0-Q_7	Parallel Outputs	50/33	1.0mA/20mA

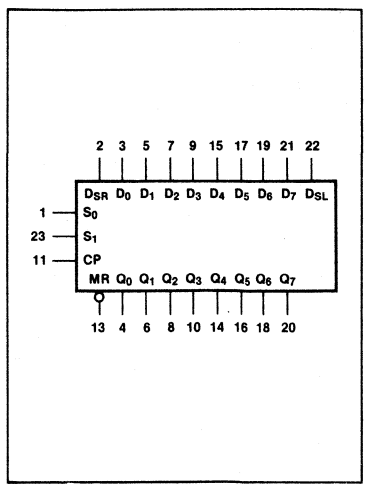
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

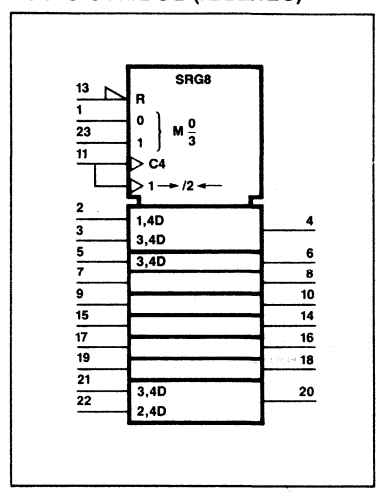
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



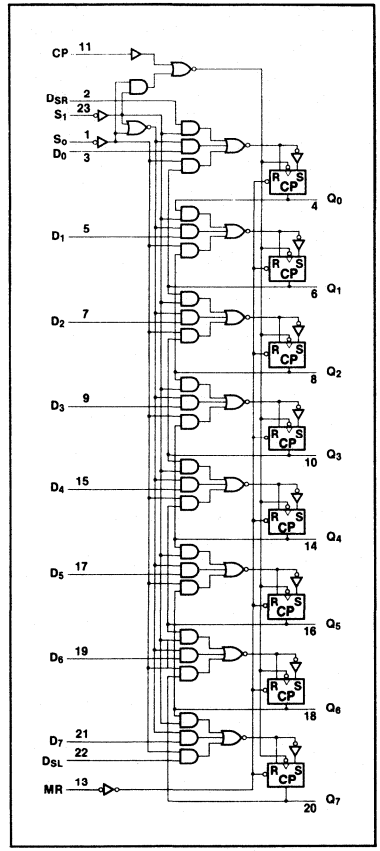
SHIFT REGISTER FAST 54/74F198

FUNCTION TABLE, 'F198

INPUTS							OUTPUTS			
$\overline{MR}$	MODE		CP	SERIAL		PARALLEL	Q_A	Q_B ...	Q_G	Q_H
	S_1	S_0		LEFT	RIGHT	A ... H				
L	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	Q_{A0}	Q_{B0}	Q_{G0}	Q_{H0}
H	H	H	↑	X	X	a ... h	a	b	g	h
H	L	H	↑	X	H	X	H	Q_{An}	Q_{Fn}	Q_{Gn}
H	L	H	↑	X	L	X	L	Q_{An}	Q_{Fn}	Q_{Gn}
H	H	L	↑	H	X	X	Q_{Bn}	Q_{Cn}	Q_{Hn}	H
H	H	L	↑	L	X	X	Q_{Bn}	Q_{Cn}	Q_{Hn}	L
H	L	L	X	X	X	X	Q_{A0}	Q_{B0}	Q_{G0}	Q_{H0}

H = HIGH level (steady state)
L = LOW level (steady state)
X = Irrelevant (any input, including transition)
↑ = Transition from LOW-to-HIGH level
a . . . h = The level of steady-state input at inputs A through H, respectively.
Q_{A0}, Q_{B0}, Q_{G0}, Q_{H0} = The level of Q_A, Q_B, Q_G or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc. = The level of Q_A, Q_B, etc., respectively, before the most recent ↑ transition of the clock.

FUNCTIONAL BLOCK DIAGRAM, 'F198



ABSOLUTE MAXIMUM RATINGS

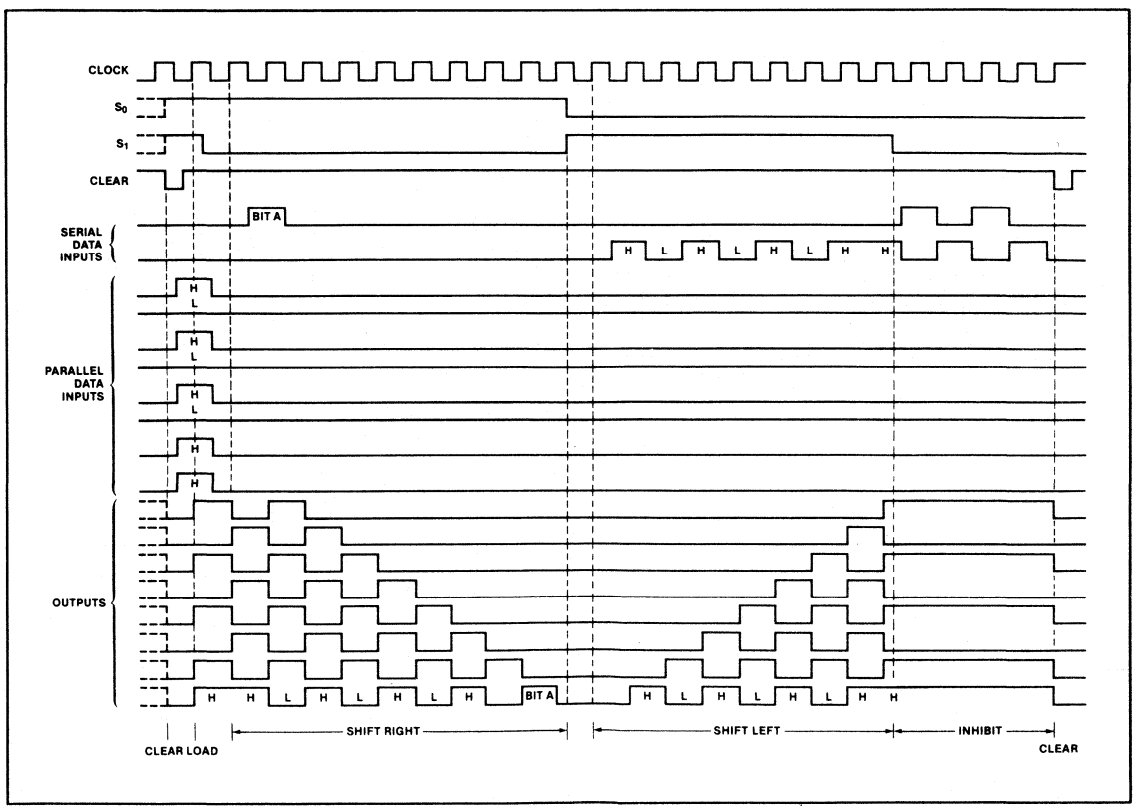
(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +55	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	– 55		125	°C
		Com'l	0		70	°C

TYPICAL TIMING DIAGRAM



DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F198 Min	54/74F198 Typ[2]	54/74F198 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		1.9	2.8	mA
			I_{CCL} Outputs LOW		6.8	10.2	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH}, V_{IN} = GND; I_{CCL}, V_{IN} = Open.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

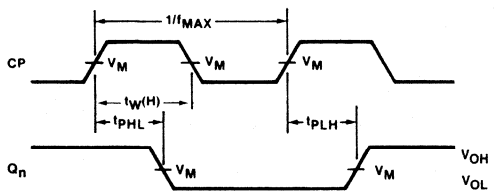
PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	105			90		90		MHz
t_{PLH}	Propagation delay	Waveform 1	3.5		7.0	3.0	8.5	3.5	8.0	ns
t_{PHL}	Clock to output		3.5		7.0	3.0	8.5	3.5	8.0	
t_{PHL}	Propagation delay, MR to output	Waveform 2	4.5		12	4.5	14.5	4.5	14	ns

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_W(H)$	Clock pulse width, HIGH	Waveform 1	5.0			5.5		5.5		ns
$t_W(L)$	MR pulse width, LOW	Waveform 2	5.0			5.0		5.0		ns
$t_s(H)$ $t_s(L)$	Setup time, D_n to clock D_{SR}, D_{SL} to clock	Waveform 3	4.0 4.0			4.0 4.0		4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW, D_n to clock D_{SR}, D_{SL} to clock	Waveform 3	0 0			1.0 1.0		1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW S_n to clock	Waveform 4	8.0 8.0			9.5 8.0		9.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW S_n to clock	Waveform 4	0 0			0 0		0 0		ns
t_{rec}	Recovery time, MR to clock	Waveform 2	7.0			9.0		8.0		ns

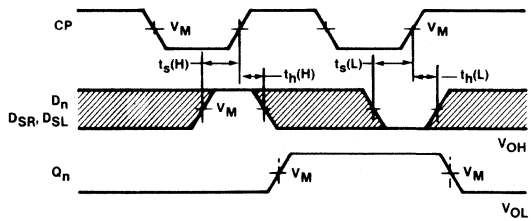
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

DATA SETUP AND HOLD TIMES

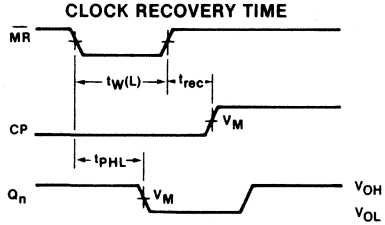


Waveform 3

$V_M = 1.5V$

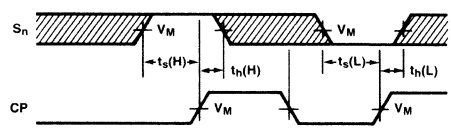
The shaded areas indicate when the input is permitted to change for predictable output performance.

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



Waveform 2

SETUP AND HOLD TIMES FOR S_0 AND S_1 INPUTS

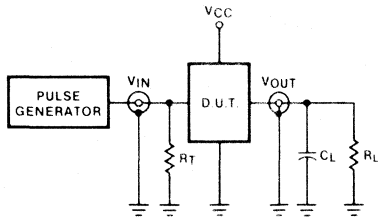


Waveform 4

5

TEST CIRCUITS AND WAVEFORMS

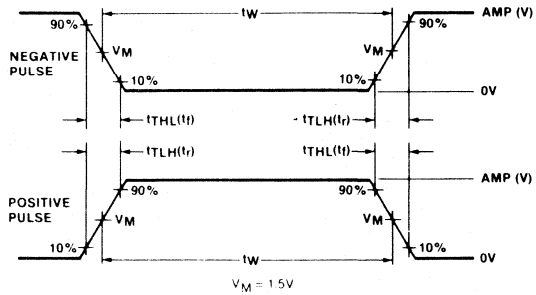
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

'F240 Octal Inverter Buffer (3-State)
'F241 Octal Buffer (3-State)

- **Octal bus interface**
- **3-State buffer outputs sink 64mA**
- **15mA source current**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F240	4.3ns	37mA
74F241	5.0ns	53mA

DESCRIPTION

The 'F240 and 'F241 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}$, each controlling four of the 3-state outputs.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F240N • N74F241N	
Plastic SO	N74F240D • N74F241D	
Ceramic DIP		S54F240F • S54F241F
Ceramic LLCC		S54F240G • S54F241G

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

FUNCTION TABLE, 'F240

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	(Z)	(Z)

FUNCTION TABLE, 'F241

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	(Z)	(Z)

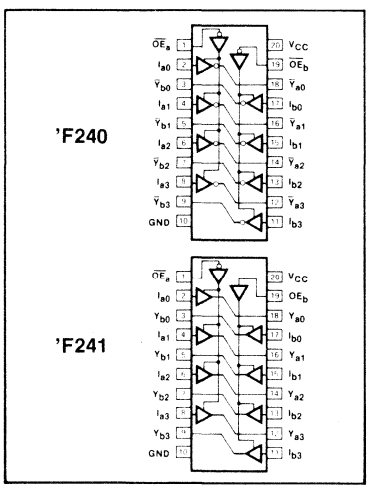
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

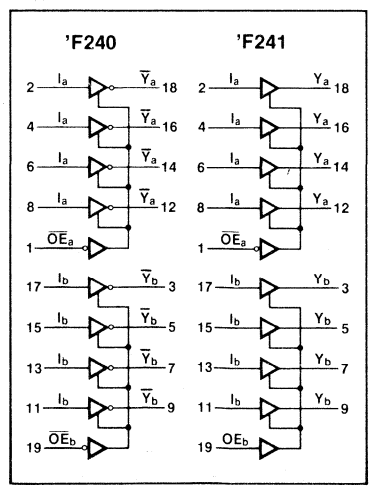
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{OE}_a$, $\overline{OE}_b$	3-State Output Enable Input (Active LOW)	1.0/1.67	20μA/1.0mA
OE_b	3-State Output Enable Input (Active HIGH)	1.0/1.67	20μA/1.0mA
I_{a0}–I_{a3}, I_{b0}–I_{b3}	Data Inputs ('F240)	1.0/1.67	20μA1.0mA
I_{a0}–I_{a3}, I_{b0}–I_{b3}	Data Inputs ('F241)	1.0/2.67	20μA/1.6mA
$\overline{Y}_a$, $\overline{Y}_b$ ('F240) Y_a, Y_b ('F241)	Data Outputs (Commercial)	150/106.7	3mA/64mA
$\overline{Y}_a$, $\overline{Y}_b$ ('F240) Y_a, Y_b ('F241)	Data Outputs (Military)	150/80	3mA/48mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

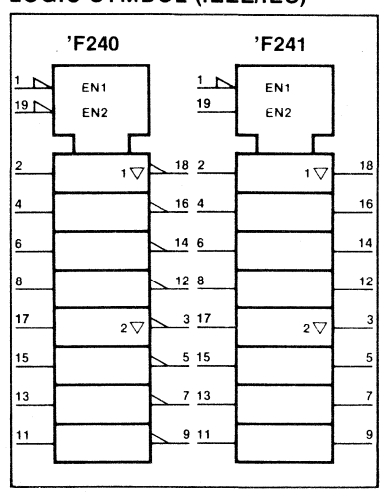
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



5

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	96	128	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current	Mil			48	mA
		Com'l			64	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F240, 241			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = 0.5V	I_{OH} = −12mA	Mil	2.0			V
			I_{OH} = −15mA	Com'l	2.0			V
		V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = −3mA	Mil	2.4	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 48mA	Mil		0.35	0.5	V
			I_{OL} = 64mA	Com'l		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = +7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	'F240 All Inputs			−0.6	−1.0	mA
			'F241 $\overline{OE}_a$, OE_b			−0.6	−1.0	mA
			'F241 I_{a0}–I_{a3}, I_{b0}–I_{b3}			−0.6	−1.6	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{OUT} = 2.4V				2	50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{OUT} = 0.5V				−2	−50	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V			−100	−150	−225	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	'F240	I_{CCH}		19	29	mA
				I_{CCL}		50	75	mA
				I_{CCZ}		42	63	mA
			'F241	I_{CCH}		40	60	mA
				I_{CCL}		60	90	mA
				I_{CCZ}		60	90	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open.

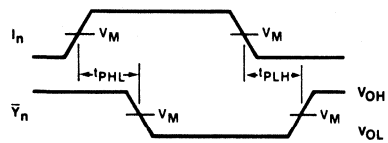
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			54F T_A, V_{CC} = Mil, $C_L = 50pF$, $R_L = 500\Omega$		74F T_A, V_{CC} = Com'l, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} Data to Output ('F240)	Waveform 1	3.0 2.0	4.5 3.0	6.5 4.5	3.0 1.5	9.0 5.5	3.0 2.0	7.5 5.0	ns
t_{PZH} Output Enable Time ('F240) t_{PZL}	Waveform 2 Waveform 3	3.0 4.5	5.0 6.5	7.5 8.5	2.0 4.0	9.5 10.5	3.0 4.0	4.0 10.0	ns
t_{PHZ} Output Disable Time ('F240) t_{PLZ}	Waveform 2 Waveform 3	3.0 3.0	5.5 5.0	7.0 7.0	2.5 2.5	8.0 8.5	3.0 3.0	7.5 7.5	ns
t_{PLH} Propagation Delay t_{PHL} Data to Output ('F241)	Waveform 2	2.5 2.5	4.0 4.0	5.2 5.2	2.5 2.5	6.5 7.0	2.5 2.5	6.2 6.5	ns
t_{PZH} Output Enable Time t_{PZL} ('F241)	Waveform 2 Waveform 3	2.0 2.0	4.0 5.0	5.7 7.0	2.0 2.0	7.0 8.5	2.0 2.0	6.7 8.0	ns
t_{PHZ} Output Disable Time t_{PLZ} ('F241)	Waveform 2 Waveform 3	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	7.0 7.5	2.0 2.0	7.0 7.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

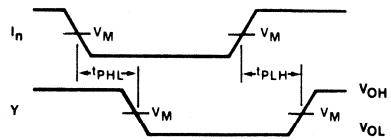
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



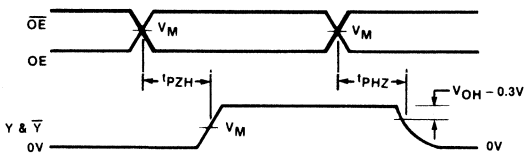
Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



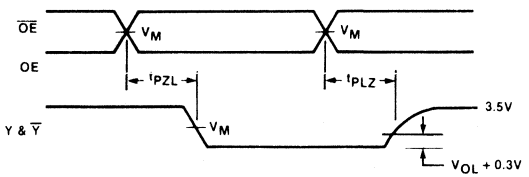
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL

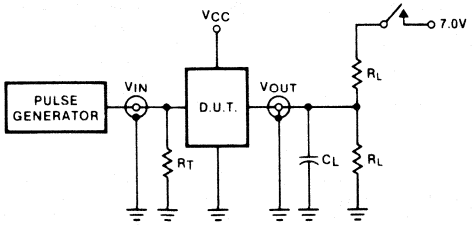


Waveform 4

$V_M = 1.5V$

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

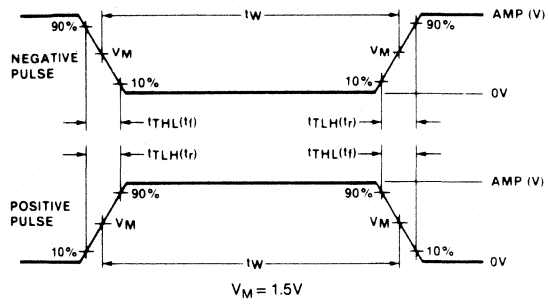
DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

'F242 Quad Transceiver, Inverting (3-State)
'F243 Quad Transceiver (3-State)

FUNCTION TABLE, 'F242

INPUTS		INPUT/OUTPUT	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	INPUT	$B = \overline{A}$
H	L	(Z)	(Z)
L	H	(a)	(a)
H	H	$A = \overline{B}$	INPUT

FUNCTION TABLE, 'F243

INPUTS		INPUT/OUTPUT	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	INPUT	B = A
H	L	(Z)	(Z)
L	H	(a)	(a)
H	H	A = B	INPUT

H = HIGH voltage level
L = LOW voltage level
(Z) = HIGH impedance (off) state
(a) = This condition is not allowed due to excessive currents.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F242	4.3ns	31.2mA
74F243	4.0ns	66mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F242N • N74F243N	
Plastic SO	N74F242D • N74F243D	
Ceramic DIP		
Ceramic LLCC		

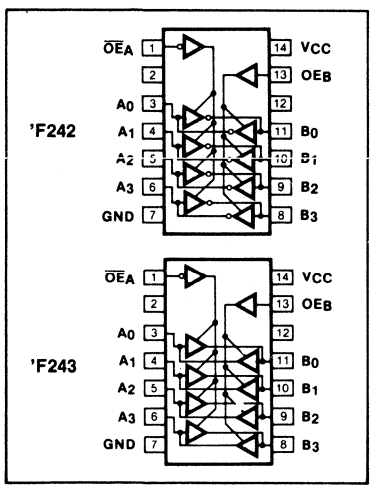
NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

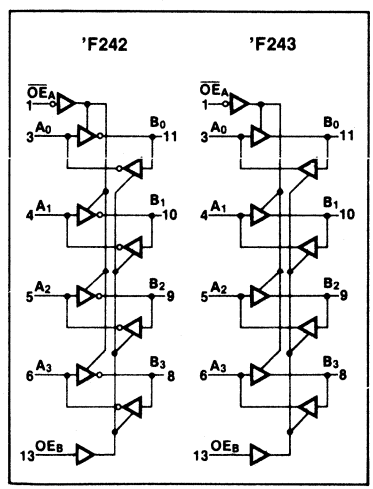
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{OE}_A$	Enable Input (Active LOW)	1.0/1.67	20μA/1mA
OE_B	Enable Input (Active HIGH)	1.0/1.67	20μA/1mA
A_n, B_n	Inputs ('F242)	3.5/1.67	70μA/1mA
A_n, B_n	Inputs ('F243)	3.5/2.67	70μA/1.6mA
A_n, B_n	Outputs (Commercial)	150/106.7	3mA/64mA
A_n, B_n	Outputs (Military)	150/80	3mA/48mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

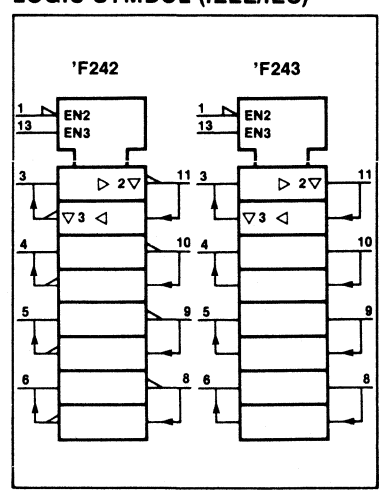
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	128	128	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current	Mil			48	mA
		Com'l			64	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]				74F242, 74F243			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = 0.5V, I_{OH} = MAX			Mil	2.0			V
					Com'l	2.0			V
		V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = − 3mA			Mil	2.4	3.4		V
					Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 48mA		Mil		0.35	0.5	V
			I_{OL} = 64mA		Com'l		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					− 0.73	− 1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 2.7V				1	70	μA
			V_O = 5.5V					100	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.4V					− 1.0	− 1.6	mA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	A, B inputs			0.1	1.0	mA
			V_I = 7.0V	$\overline{OE}_A$, OE_B inputs			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					1	70	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	A inputs $\overline{OE}_A$, OE_B = V_{IL} = MAX			− 1.2	− 1.6	mA
				B inputs $\overline{OE}_A$, OE_B = V_{IH} = MIN			− 1.2	− 1.6	mA
			V_I = 0.5V	$\overline{OE}_A$, OE_B inputs			− 0.6	− 1.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V				− 100	− 150	− 225	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH	'F242		22.1	35	mA
			I_{CCL}	Outputs LOW			39.4	55	mA
			I_{CCZ}	Outputs OFF			32.0	45	mA
			I_{CCH}	Output HIGH	'F243		64	80	mA
			I_{CCL}	Outputs LOW			64	90	mA
			I_{CCZ}	Outputs OFF			71	90	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open and transceivers enabled in one direction only, or with all transceivers disabled.

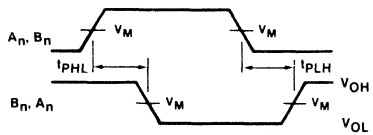
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F			54F		74F		UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output ('F242)	Waveform 1	3.0 2.0	4.5 3.0	6.5 4.5	3.0 1.5	9.0 5.0	3.0 2.0	7.5 4.5	
t_{PZH} t_{PZL}	Output enable time ('F242)	Waveform 3	3.5 3.5	6.0 6.5	7.5 9.0	3.0 3.0	10.0 12.0	3.5 3.5	9.0 10.5	ns
t_{PHZ} t_{PLZ}	Output disable time ('F242)	Waveform 3	4.0 3.5	7.0 6.0	9.0 9.5	4.0 3.0	11.0 13.5	4.0 3.5	9.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay Data to output ('F243)	Waveform 2	2.5 2.5	4.0 4.0	5.2 5.2	2.0 2.0	6.5 8.5	2.0 2.0	6.2 6.5	ns
t_{PZH} t_{PZL}	Output enable time ('F243)	Waveform 4	2.0 2.0	4.5 5.0	5.7 7.5	2.0 2.0	8.0 10.5	2.0 2.0	6.7 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time ('F243)	Waveform 4	2.0 2.0	4.0 4.5	6.0 6.0	2.0 2.0	7.5 8.5	2.0 2.0	7.0 7.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

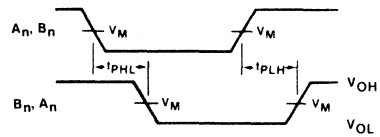
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



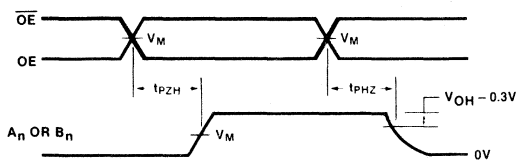
Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



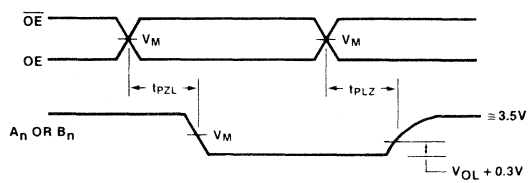
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL

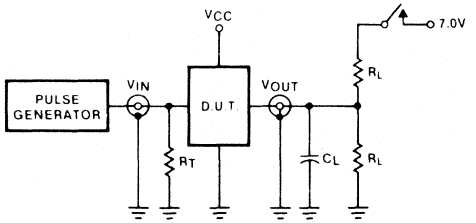


Waveform 4

VM = 1.5V

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

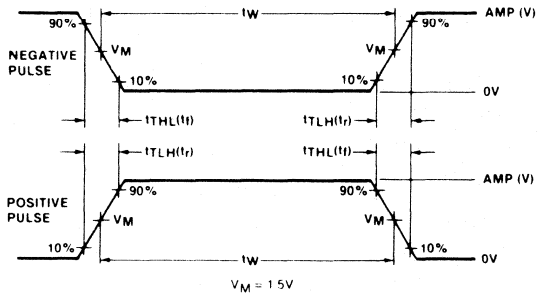
DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

BUFFER — FAST 54/74F244

Octal Buffer (3-State)

- **Octal bus interface**
- **3-state buffer outputs sink 64mA**
- **15mA source current**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F244	4.0ns	53mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F244N	
Plastic SO	N74F244D	
Ceramic DIP		S54F244F
Ceramic LLCC		S54F244G

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F244 is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}$, each controlling four of the 3-state outputs.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

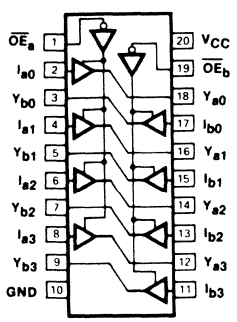
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{OE}_a$	3-State Output Enable Input (Active LOW)	1.0/1.67	20μA/1.0mA
$\overline{OE}_b$	3-State Output Enable Input (Active LOW)	1.0/1.67	20μA/1.0mA
I_{a0}–I_{a3}, I_{b0}–I_{b3}	Data Inputs	1.0/2.67	20μA/1.6mA
Y_{a0}–Y_{a3}, Y_{b0}–Y_{b3}	Data Outputs (Commercial)	150/106.7	3mA/64mA
Y_{a0}–Y_{a3}, Y_{b0}–Y_{b3}	Data Outputs (Military)	150/80	3mA/48mA

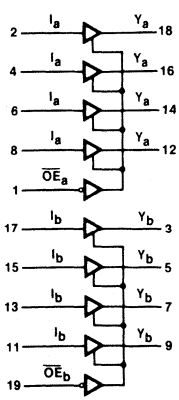
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

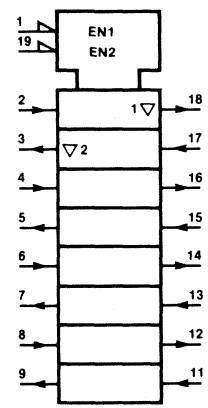
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	128	128	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current	Mil			48	mA
		Com'l			64	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F244 Min	54/74F244 Typ[2]	54/74F244 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = 0.5V	I_{OH} = −12mA	Mil	2.0			V
			I_{OH} = −15mA	Com'l	2.0			V
		V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = −3mA	Mil	2.4	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 48mA	Mil		0.35	0.5	V
			I_{OL} = 64mA	Com'l		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	$\overline{OE}_a$, $\overline{OE}_b$			−0.7	−1.0	mA
			Data Inputs I_{a0}-I_{a3}, I_{b0}-I_{b3}			−0.6	−1.6	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{OUT} = 2.4V				2	50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{OUT} = 0.5V				−2	−50	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V			−100	−150	−225	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		40	60	mA
			I_{CCL}	Outputs LOW		60	90	mA
			I_{CCZ}	Outputs OFF		60	90	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open.

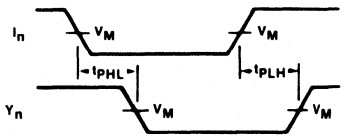
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	2.5	4.0	5.2	2.5	6.5	2.5	6.2	ns
t_{PHL}	Propagation delay	Waveform 1	2.5	4.0	5.2	2.5	7.0	2.5	6.5	ns
t_{PZH}	Enable to HIGH	Waveform 2	2.0	4.3	5.7	2.0	7.0	2.0	6.7	ns
t_{PZL}	Enable to LOW	Waveform 3	2.0	5.0	7.0	2.0	8.5	2.0	8.0	ns
t_{PHZ}	Disable from HIGH	Waveform 2	2.0	3.5	6.0	2.0	7.0	2.0	7.0	ns
t_{PLZ}	Disable from LOW	Waveform 3	2.0	4.0	6.0	2.0	7.5	2.0	7.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

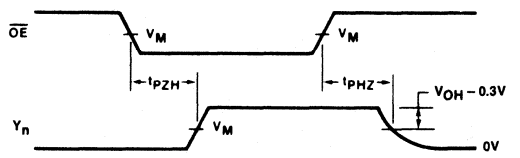
AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



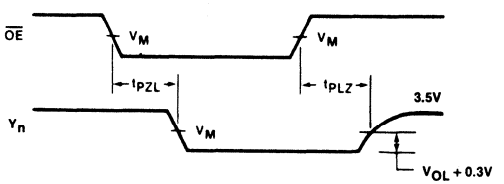
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL

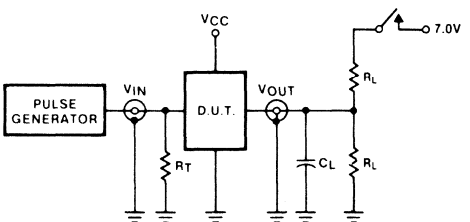


Waveform 3

$V_M = 1.5V$

TEST CIRCUITS AND WAVEFORMS

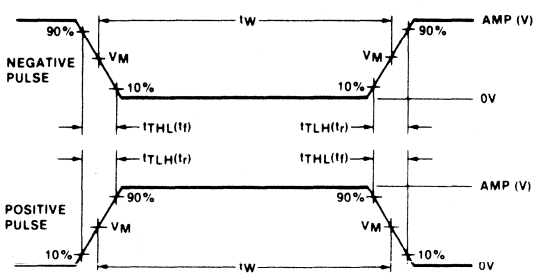
TEST CIRCUIT FOR 3-STATE OUTPUTS



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

TRANSCEIVER FAST 54/74F245

Preliminary

Octal Transceiver (3-State)

- **High impedance NPN base inputs for reduced loading (20μA in LOW and HIGH states)**
- **Octal bidirectional bus interface**
- **3-State buffer outputs sink 64mA**
- **15mA source current**
- **Outputs are placed in Hi-Z state during power-off conditions**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F245		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F245N	
Plastic SO	N74F245D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FANOUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/0.033	20μA/20μA
S/$\overline{R}$	Send Receive Input	1.0/0.033	20μA/20μA
A_0-A_7	3-State A Data Inputs	1.0/0.033	20μA/20μA
A_0-A_7	3-State A Data Outputs	150/33	3mA/20mA
B_0-B_7	3-State B Data Inputs	1.0/0.033	20μA/20μA
B_0-B_7	3-State B Data Outputs (Commercial) 3-State B Data Outputs (Military)	150/107 150/80	3mA/64mA 3mA/48mA

One (1.0) FAST Unit Load (Ful) is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

DESCRIPTION

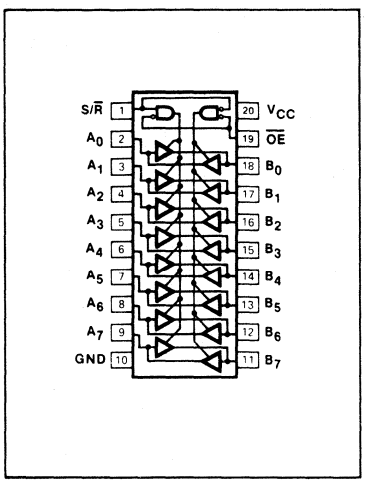
The 'F245 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Send/Receive (S/$\overline{R}$) input for direction control. All of the inputs utilize Signetics NPN input structures to reduce input loading and reduce input capacitance. The 3-State outputs, B_0-B_7, have been designed to prevent output bus loading if the power is removed from the device.

FUNCTION TABLE

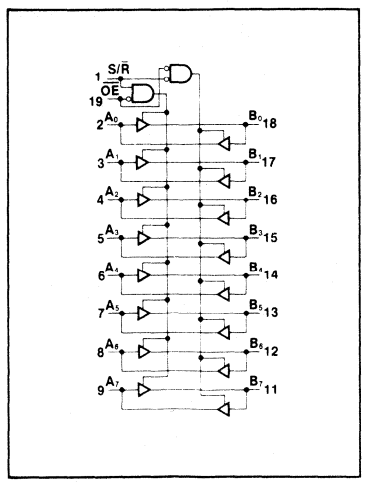
INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	S/$\overline{R}$	A_n	B_n
L	L	A = B	INPUTS
L	H	INPUT	B = A
H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

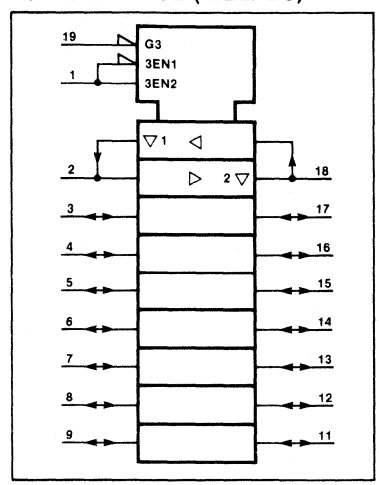
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



5

TRANSCEIVER FAST 54/74F245

Preliminary

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free air temperature range.

PARAMETER			54F	74F	UNIT
V_{CC}	Supply voltage		−0.5 to 7.0	−0.5 to 7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	A_0-A_7	40	48	mA
		B_0-B_7	128	128	mA
T_A	Operating free-air temperature range		−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current, A_0-A_7	Mil			−3	mA
		Com'l			−3	mA
I_{OH}	HIGH-level output current, B_0-B_7	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current, A_0-A_7	Mil			20	mA
		Com'l			24	mA
I_{OL}	LOW-level output current, B_0-B_7	Mil			48	mA
		Com'l			64	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

TRANSCEIVER FAST 54/74F245

Preliminary

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F245 Min	54/74F245 Typ[2]	54/74F245 Max	UNIT
V_{OH}	HIGH-level output voltage A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3.0mA	Mil	2.4	3.4		V
				Com'l	2.7	3.4		V
V_{OH}	HIGH-level output voltage B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −12mA	Mil	2.0			V
			I_{OH} = −15mA	Com'l	2.0			V
			I_{OH} = −3.0mA	Mil	2.4	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage A_0-A_7	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = 24mA				0.35	0.5	V
V_{OL}	LOW-level output voltage B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	Mil			0.5	V
			I_{OL} = 64mA	Com'l		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = +7.0V					100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V					−20	μA
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{OUT} = 2.4V					50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{OUT} = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current [4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH				mA
			I_{CCL}	Outputs LOW			143	mA
			I_{CCZ}	Outputs OFF				

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with outputs open.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} = Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} = Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	Waveform 1	2.5	4.2	5.5			2.5	6.5	ns
t_{PHL}	A_n to B_n or B_n to A_n	Waveform 1	2.5	4.6	6.0			2.5	7.0	
t_{PZH}	Output Enable Time	Waveform 2	3.0	5.3	7.0			3.0	8.0	ns
t_{PZL}		Waveform 3	4.5	7.9	10			4.5	11	
t_{PHZ}	Output Disable Time	Waveform 2	3.0	5.0	6.5			3.0	7.5	ns
t_{PLZ}		Waveform 3	2.0	3.7	5.0			2.0	6.0	

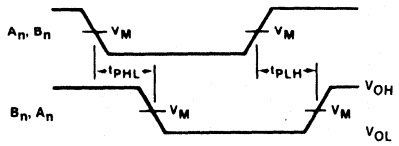
5

TRANSCEIVER FAST 54/74F245

Preliminary

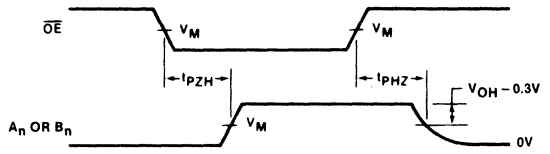
AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 1

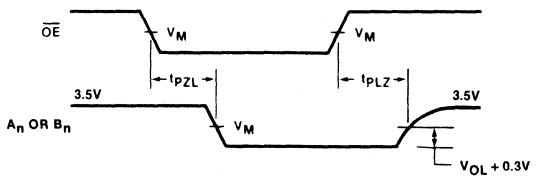
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

$V_M = 1.5V$

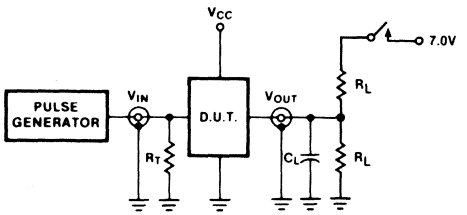
3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



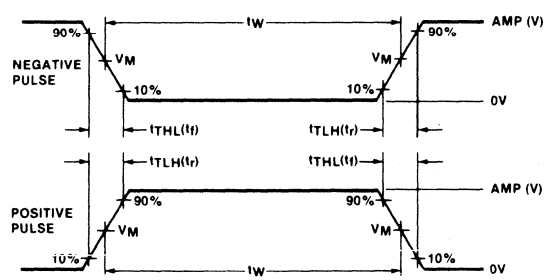
SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

MULTIPLEXER — FAST 54/74F251

Preview

8-Input Multiplexer (3-State)

- **High speed 8-to-1 multiplexing**
- **True and complement outputs**
- **Both outputs are 3-State for further multiplexer expansion**

TYPE	TYPICAL PROPAGATION DELAY (Data to Y)	TYPICAL SUPPLY CURRENT (Total)
74F251	18ns	9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F251N	
Plastic SO	N74F251P	
Ceramic DIP		S54F251F
Ceramic LLCC		S54F251G

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
I_0-I_7	Data Inputs	1.0/1.0	20μA/0.6mA
S_0-S_2	Select Inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}$	3-State Output Enable Input (Active LOW)	1.0/1.0	20μA/0.6mA
Y, $\overline{Y}$	3-State Output 3-State Output Inverted	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

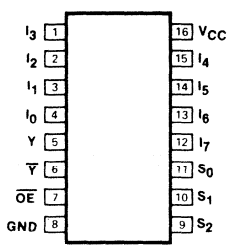
DESCRIPTION

The 'F251 is a logical implementation of a single-pole, 8-position switch with the state of three Select inputs (S_0, S_1, S_2) controlling the switch position. Assertion (Y) and Negation ($\overline{Y}$) outputs are both provided. The Output Enable input ($\overline{OE}$) is active LOW. The logic function provided at the output, when activated, is:

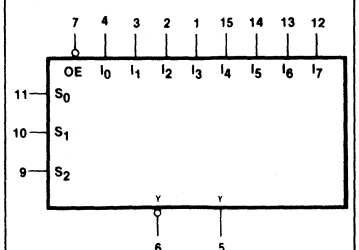
$$Y = \overline{OE} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

Both outputs are in the HIGH impedance (HIGH Z) state when the output enable is HIGH, allowing multiplexer expansion by tying the outputs of up to 128 devices together. All but one device must be in the HIGH impedance state to avoid high currents that would exceed the maximum ratings, when the outputs of the 3-State devices are tied together. Design of the output enable signals must ensure there is no overlap in the active LOW portion of the enable voltages.

PIN CONFIGURATION

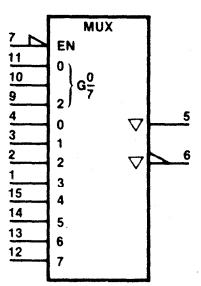


LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

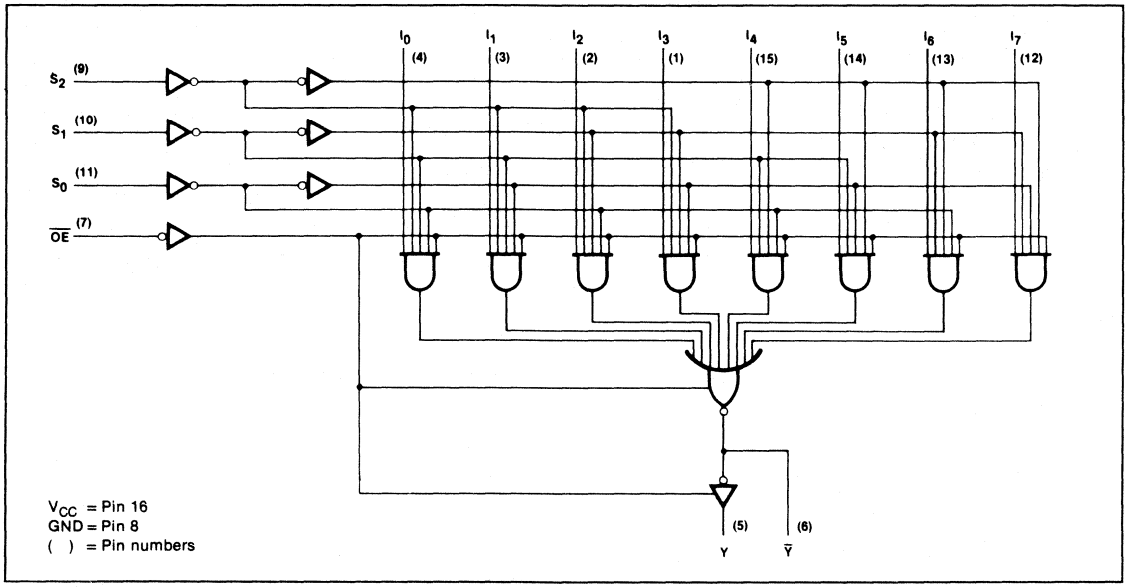
LOGIC SYMBOL (IEEE/IEC)



MULTIPLEXER FAST 54/74F251

Preview

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS												OUTPUTS	
$\overline{OE}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

Preview

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + 5.5	− 0.5 to + 5.5	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 3.0	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

MULTIPLEXER FAST 54/74F251

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F251 Min	54/74F251 Typ[2]	54/74F251 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IN} = MIN, I_{OH} = MAX	Mil	2.4	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V			2	50	μA
I_{OZL}	Off-state output current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		−60	−80	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH				mA
			I_{CCL} Outputs LOW				mA
			I_{CCZ} Outputs OFF				mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with V_{CC} = MAX, Select and Data inputs at 4.5V, and $\overline{OE}$ ground for output HIGH and LOW conditions; V_{CC} = MAX, Data inputs and the $\overline{OE}$ at 4.5V for outputs OFF condition.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	54F T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω Min	Max	74F T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH}	Propagation delay	Waveform 2	4.5	9.6	13	3.5	16.5	4.5	14	ns
t_{PHL}	Select to Y output		5.0	6.9	9.0	3.0	10.5	4.0	10	
t_{PLH}	Propagation delay	Waveform 1	4.0	5.9	8.0	3.5	9.5	4.0	9.0	ns
t_{PHL}	Select to $\overline{Y}$ output		3.2	5.7	7.5	3.2	9.5	3.2	8.5	
t_{PLH}	Propagation delay	Waveform 2	5.5	7.2	9.5	3.5	11.5	5.5	10.5	ns
t_{PHL}	Data to Y output		3.7	5.1	6.5	3.7	7.5	3.7	7.5	
t_{PLH}	Propagation delay	Waveform 1	3.0	4.1	5.7	2.5	8.0	3.0	7.0	ns
t_{PHL}	Data to $\overline{Y}$ output		2.0	3.0	4.0	2.0	6.0	2.0	5.0	
t_{PZH}	Output enable time	Waveform 3	4.0	6.9	9.0	4.0	10	4.0	10	ns
t_{PZL}	$\overline{OE}$ to Y		3.5	6.0	8.0	3.5	10	3.5	9.0	
t_{PZH}	Output enable time	Waveform 4	3.0	5.4	7.0	3.0	9.5	3.0	8.0	ns
t_{PZL}	$\overline{OE}$ to $\overline{Y}$		3.5	6.4	8.5	3.5	10.5	3.5	9.5	
t_{PHZ}	Output disable time	Waveform 3	3.0	5.0	6.5	3.0	8.5	3.0	7.5	ns
t_{PLZ}	$\overline{OE}$ to $\overline{Y}$		2.0	3.2	4.5	2.0	7.5	2.0	5.5	
t_{PHZ}	Output disable time	Waveform 4	3.0	4.7	6.0	3.0	7.0	3.0	7.0	ns
t_{PLZ}	$\overline{OE}$ to Y		2.0	3.5	4.5	2.0	5.5	2.0	5.5	

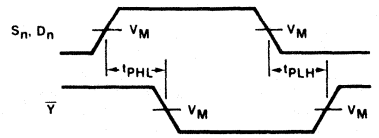
NOTE
Subtract 0.2ns from minimum values for SO package.

MULTIPLEXER — FAST 54/74F251

Preview

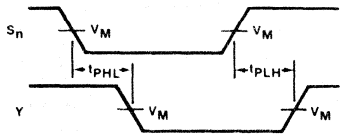
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



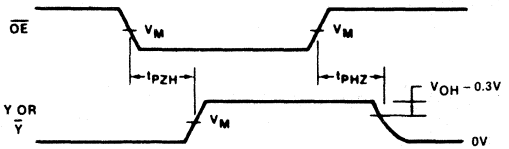
Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



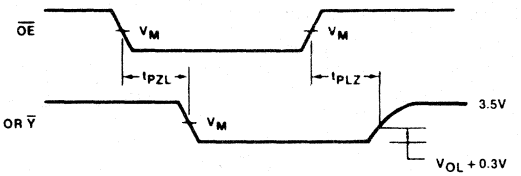
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



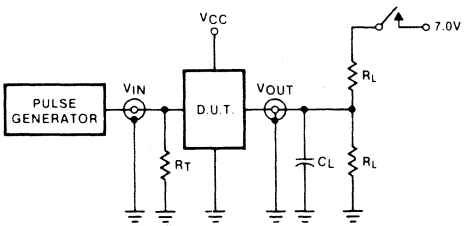
Waveform 4

$V_M = 1.5V$

5

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



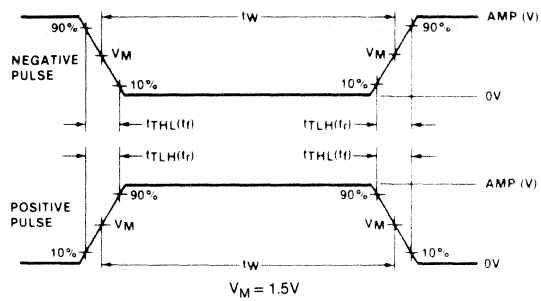
SWITCH POSITION

TEST	SWITCH
t_{PLZ} t_{PZL} All other	closed closed open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

MULTIPLEXER — FAST 54/74F253

Preview

Dual 4-Input Multiplexer (3-State)

- **3-State outputs for bus interface and multiplex expansion**
- **Common Select inputs**
- **Separate Output Enable inputs**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F253		14.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F253N	
Plastic SO	N74F253D	
Ceramic DIP		S54F253F
Ceramic LLCC		S54F253G

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F253 has two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common Select inputs (S_0, S_1). When the individual Output Enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs of the 4-input multiplexers are HIGH, the outputs are forced to a HIGH impedance (HIGH Z) state.

The 'F253 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two Select inputs. Logic equations for the outputs are shown below:

$$Y_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$Y_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0$$

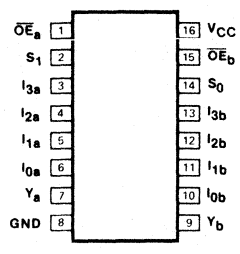
All but one device must be in the HIGH impedance state to avoid high currents exceeding the maximum ratings, if the outputs of the 3-State devices are tied together. Design of the Output Enable signals must ensure that there is no overlap.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

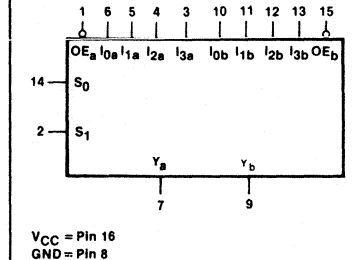
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
I_{0a}–I_{3a}	Side A data inputs	1.0/1.0	20μA/0.6mA
I_{0b}–I_{3b}	Side B data inputs	1.0/1.0	20μA/0.6mA
S_0, S_1	Common select inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}_a$	Side A output enable input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{OE}_b$	Side B output enable input (active LOW)	1.0/1.0	20μA/0.6mA
Y_a, Y_b	3-State outputs	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

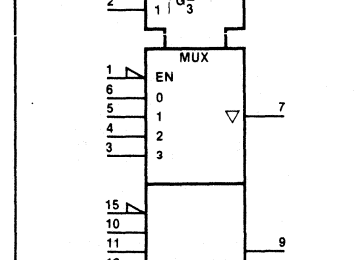
PIN CONFIGURATION



LOGIC SYMBOL



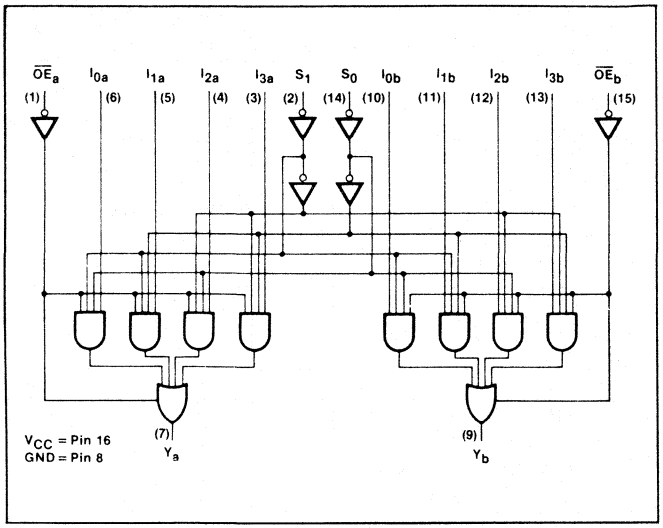
LOGIC SYMBOL (IEEE/IEC)



MULTIPLEXER — FAST 54/74F253

Preview

LOGIC DIAGRAM



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Y
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

5

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	– 0.5 to + 7.0	– 0.5 to + 7.0	V
V_{IN}	Input voltage	– 0.5 to + 7.0	– 0.5 to + 7.0	V
I_{IN}	Input current	– 30 to + 5	– 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	– 0.5 to + 5.5	– 0.5 to + 5.5	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	– 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 3	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	– 55		125	°C
		Com'l	0		70	°C

MULTIPLEXER FAST 54/74F253

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F524 Min	54/74F524 Typ[2]	54/74F524 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.4	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			– 0.73	– 1.2	V
I_{OZH}	Off-stage output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V			2	50	μA
I_{OZL}	Off-state output current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			– 2	– 50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			– 0.4	– 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		– 60	– 90	– 150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} $\overline{OE}_n$ = GND; I_o, S_n = 4.5V; I_1–I_3 = GND		11.5	16	mA
			I_{CCL} I_n, S_n, $\overline{OE}_n$ = GND		16	23	mA
			I_{CCZ} $\overline{OE}_n$ = 4.5V; I_n, S_n = GND		16	23	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

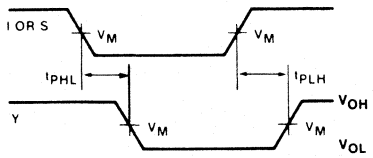
PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	54/74F Typ	54/74F Max	54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω Min	54F Max	74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω Min	74F Max	UNIT
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1	3.0 3.0	5.5 5.5	7.0 7.0	2.5 2.5	9.0 8.0	3.0 3.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1	5.5 4.5	10.1 9.2	12.5 11	3.5 2.5	15 12	4.5 3.5	13.5 12	ns
t_{PZH}	Output enable to HIGH level	Waveform 2	3.0	6.8	9.0	2.5	10.5	3.0	10	ns
t_{PZL}	Output enable to LOW level	Waveform 3	3.0	7.2	9.5	2.5	11	3.0	10.5	ns
t_{PHZ}	Output disable from HIGH level	Waveform 2, C_L = 5pF	2.0	3.7	5.0	2.0	6.5	2.0	6.0	ns
t_{PLZ}	Output disable from LOW level	Waveform 3, C_L = 5pF	2.0	4.4	6.0	2.0	9.0	2.0	7.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

Preview

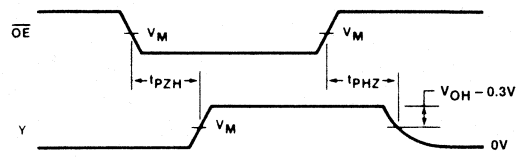
AC WAVEFORMS

PROPAGATION DELAY DATA AND SELECT TO OUTPUT



Waveform 1

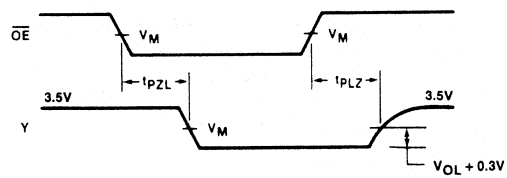
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

$V_M = 1.5V$

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL

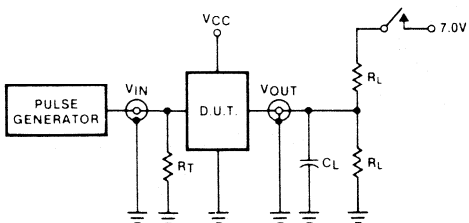


Waveform 3

5

TEST CIRCUITS AND WAVEFORMS

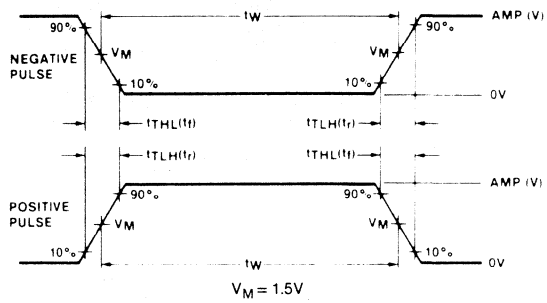
TEST CIRCUIT FOR 3-STATE OUTPUTS



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

LATCH

FAST 54/74F256

Dual 4-Bit Addressable Latch

- Combines dual demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common Clear input
- Useful as dual 1-of-4 active HIGH decoder

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F256	7ns	35mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F256N	
Plastic SO	N74F256D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

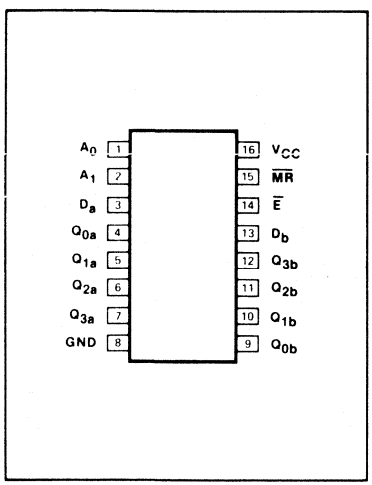
The 'F256 dual addressable latch has four distinct modes of operation which are selectable by controlling the Master Reset and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode ($\overline{MR}$ = $\overline{E}$ = LOW), addressed outputs will follow the level of the D inputs, with all other outputs LOW. In the Master Reset mode, all outputs are LOW and unaffected by the Address and Data inputs.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

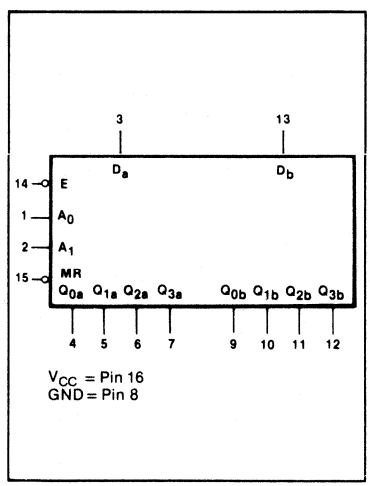
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
D_a, D_b	Side A, Side B Data Inputs	1.0/1.0	20μA/0.6mA
A_0, A_1	Address Inputs	1.0/1.0	20μA/0.6mA
$\overline{E}$, $\overline{MR}$	Enable, Master Reset Inputs	1.0/1.0	20μA/0.6mA
Q_{0a}-Q_{3a}	Side A Outputs	50/33	1mA/20mA
Q_{0b}-Q_{3b}	Side B Outputs	50/33	1mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

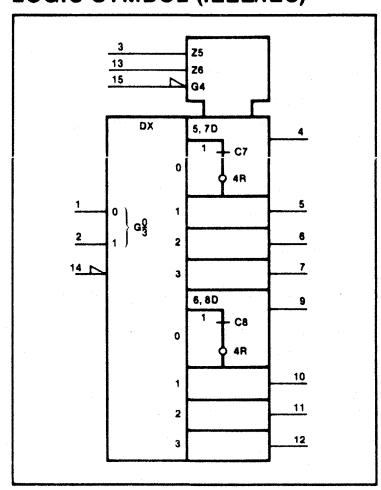
PIN CONFIGURATION



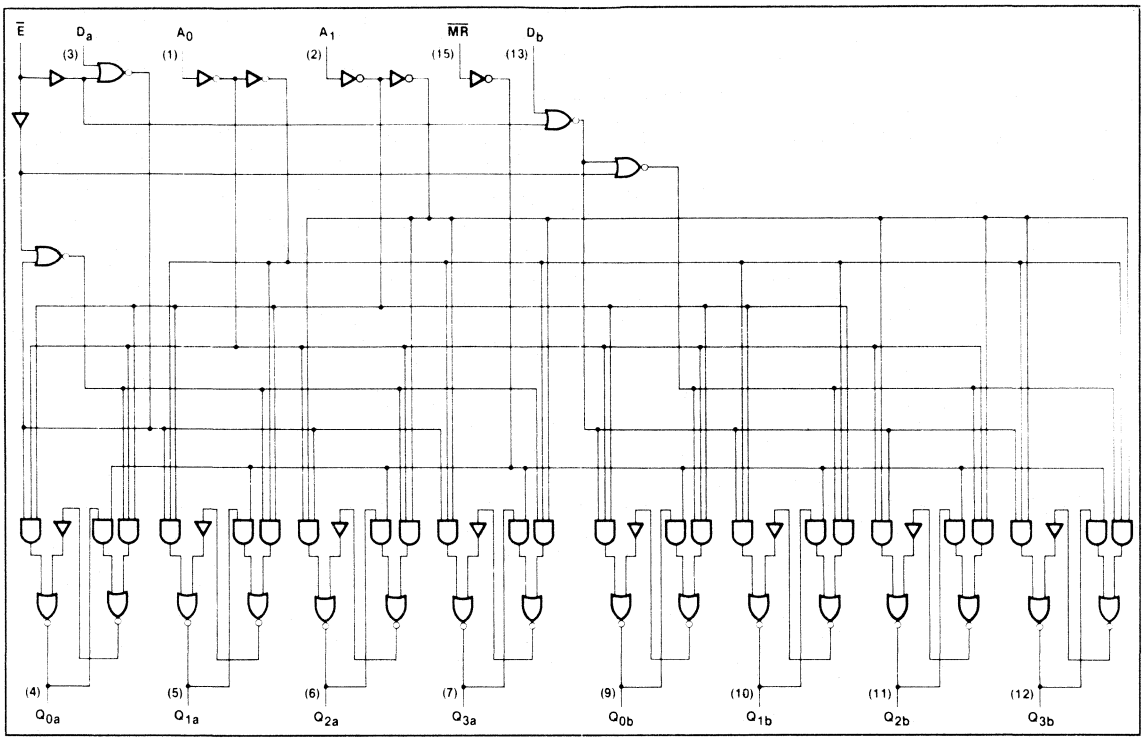
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



5

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	$\overline{MR}$	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3
Master Reset	L	H	X	X	X	L	L	L	L
Demultiplex (active HIGH decoder when D = H)	L	L	d	L	L	Q = d	L	L	L
	L	L	d	H	L	L	Q = d	L	L
	L	L	d	L	H	L	L	Q = d	L
	L	L	d	H	H	L	L	L	Q = d
Store (do nothing)	H	H	X	X	X	q_0	q_1	q_2	q_3
Addressable latch	H	L	d	L	L	Q = d	q_1	q_2	q_3
	H	L	d	H	L	q_0	Q = d	q_2	q_3
	H	L	d	L	H	q_0	q_1	Q = d	q_3
	H	L	d	H	H	q_0	q_1	q_2	Q = d

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
X = Don't care.
d = HIGH or LOW data one setup time prior to the LOW-to-HIGH Enable transition.
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	– 0.5 to 7.0	– 0.5 to 7.0	V
V_{IN}	Input voltage	– 0.5 to + 7.0	– 0.5 to + 7.0	V
I_{IN}	Input current	– 30 to + 5	– 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	– 0.5 to + V_{CC}	– 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	– 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				+ 0.8	V
I_{IK}	Input clamp current				18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F256			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			− 0.73	− 1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			− 0.4	− 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		− 60		− 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Output HIGH			40	mA
			I_{CCL} Output LOW			60	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with inputs grounded and outputs open.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F			54F		74F		UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			T_A, V_{CC} = Mil $C_L = 50pF$ $R_L = 500\Omega$		T_A, V_{CC} = Com'l $C_L = 50pF$ $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay Enable to output	Waveform 1	6.0 3.0	8.0 5.0	10.5 7.0			6.0 3.0	12.0 7.5	ns
t_{PLH} t_{PHL} Propagation delay Data to output	Waveform 2	5.0 3.0	7.0 5.0	9.0 7.0			5.0 2.5	10.0 7.5	ns
t_{PLH} t_{PHL} Propagation delay Address to output	Waveform 3	5.0 4.5	10.0 8.5	14.0 9.5			5.0 4.0	14.5 10.0	ns
t_{PHL} Propagation delay Master Reset to output	Waveform 4	5.0	7.0	9.0			4.5	10.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

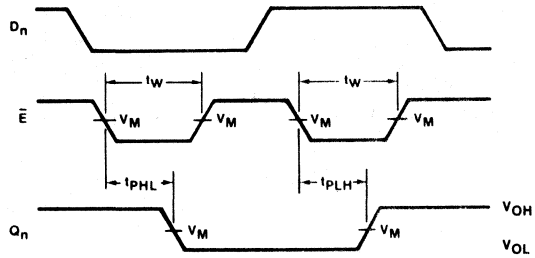
AC SETUP REQUIREMENTS

PARAMETER	TEST CONDITIONS	54/74F			54F		74F		UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			T_A, V_{CC} = Mil $C_L = 50pF$ $R_L = 500\Omega$		T_A, V_{CC} = Com'l $C_L = 50pF$ $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	Min	Max	
t_W Enable pulse width	Waveform 1	4.0			4.0		4.0		ns
t_W Master Reset pulse width	Waveform 4	4.0			4.0		4.0		ns
$t_s(H)$ Setup time HIGH, Data to Enable	Waveform 5	4.0			4.0		4.0		ns
$t_s(L)$ Setup time LOW, Data to Enable	Waveform 5	4.0			4.0		4.0		ns
$t_h(H)$ Hold time HIGH, Data to Enable	Waveform 5	1.0			1.0		1.0		ns
$t_h(L)$ Hold time LOW, Data to Enable	Waveform 5	1.0			1.0		1.0		ns
t_s Setup time, Address to Enable[a]	Waveform 6	4.0			4.0		4.0		ns
t_h Hold time, Address to Enable[b]	Waveform 6	0			0		0		ns

NOTES
a. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
b. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

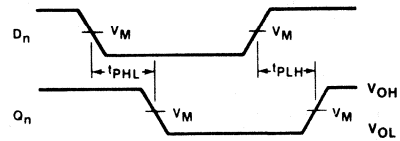
AC WAVEFORMS

PROPAGATION DELAY ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



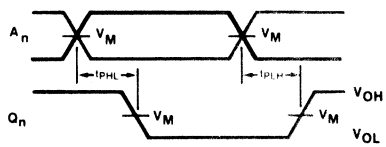
Waveform 1

PROPAGATION DELAY DATA TO OUTPUT



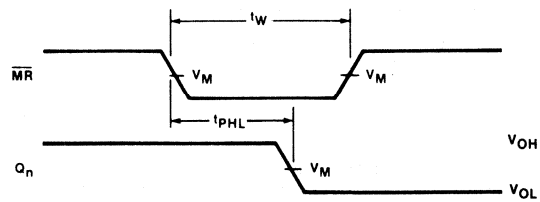
Waveform 2

PROPAGATION DELAY ADDRESS TO OUTPUT



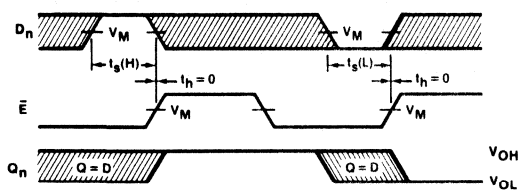
Waveform 3

MASTER RESET TO OUTPUT DELAY AND MASTER RESET PULSE WIDTH



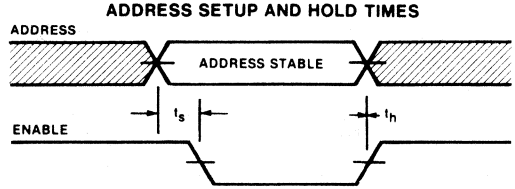
Waveform 4

DATA SETUP AND HOLD TIMES



Waveform 5

ADDRESS SETUP AND HOLD TIMES



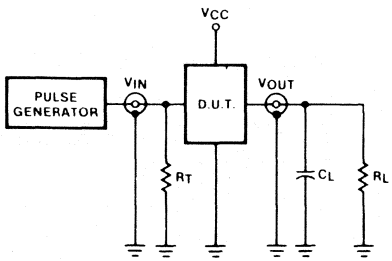
Waveform 6

V_M = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

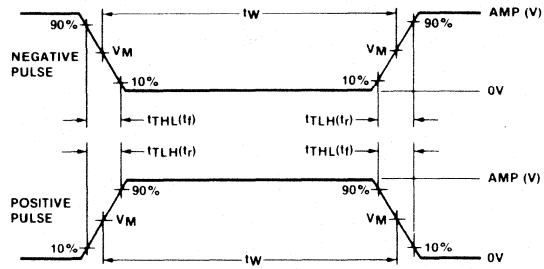
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

DATA SELECTOR/MULTIPLEXER — FAST 54/74F257

Quad 2-Line To 1-Line Data Selector/Multiplexer (3-State)

- **Multifunction capability**
- **Non-inverting data path**
- **3-State outputs**
- **See 'F258 for inverting version**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F257	4.3ns	12mA

DESCRIPTION

The 'F257 has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the Select input is HIGH. Data appears at the outputs in true (non-inverted) form from the selected outputs.

The 'F257 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

Outputs are forced to a HIGH impedance "off" state when the Output Enable input ($\overline{OE}$) is HIGH. All but one device must be in the HIGH impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F257N	
Plastic SO	N74F257D	
Ceramic DIP		S54F257F
Ceramic LLCC		S54F257G

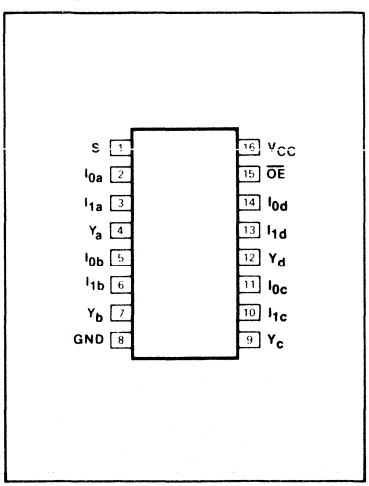
NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

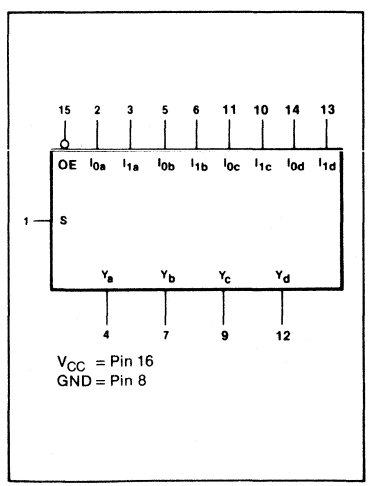
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
All	Inputs	1.0/1.0	20μA/0.6mA
Y_a-Y_d	Outputs	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

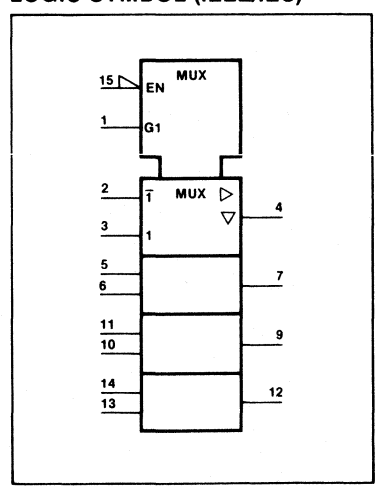
PIN CONFIGURATION



LOGIC SYMBOL

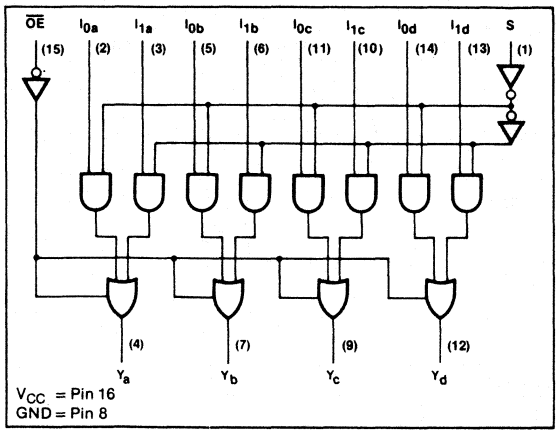


LOGIC SYMBOL (IEEE/IEC)



DATA SELECTOR/MULTIPLEXER FAST 54/74F257

LOGIC DIAGRAM



FUNCTION TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	48	48	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

5

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−3.0	mA
I_{OL}	LOW-level output current				24	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F257			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = MAX	Mil	2.4			V
				Com'l	2.7			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 20mA	Mil		0.3	0.5	V
			I_{OL} = 24mA	Com'l		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				− 0.73	− 1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V				2	50	μA
I_{OZL}	Off-state output current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				− 2	− 50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				− 0.4	− 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V			− 60	− 80	− 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		9.0	15.0	mA
			I_{CCL}	Outputs LOW		14.5	22.0	mA
			I_{CCZ}	Outputs OFF		15.0	23.0	mA

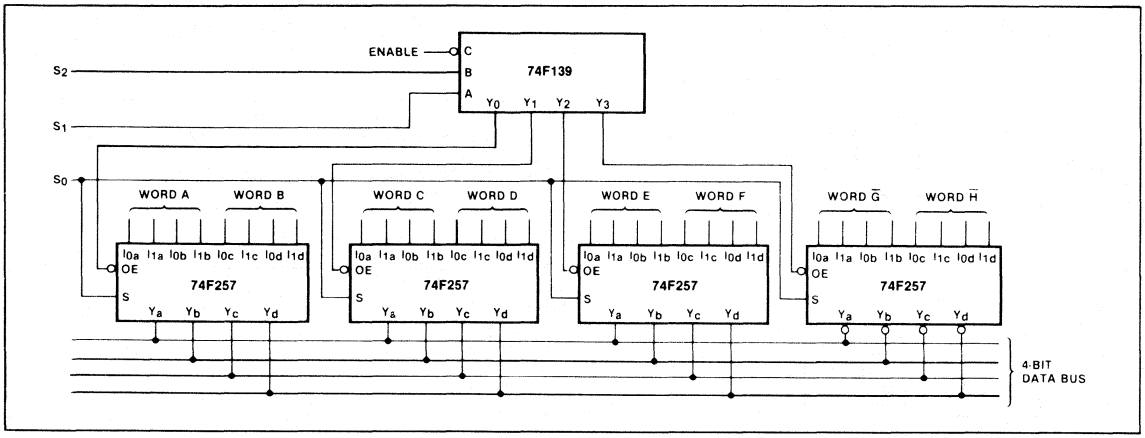
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with all outputs open and inputs grounded.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

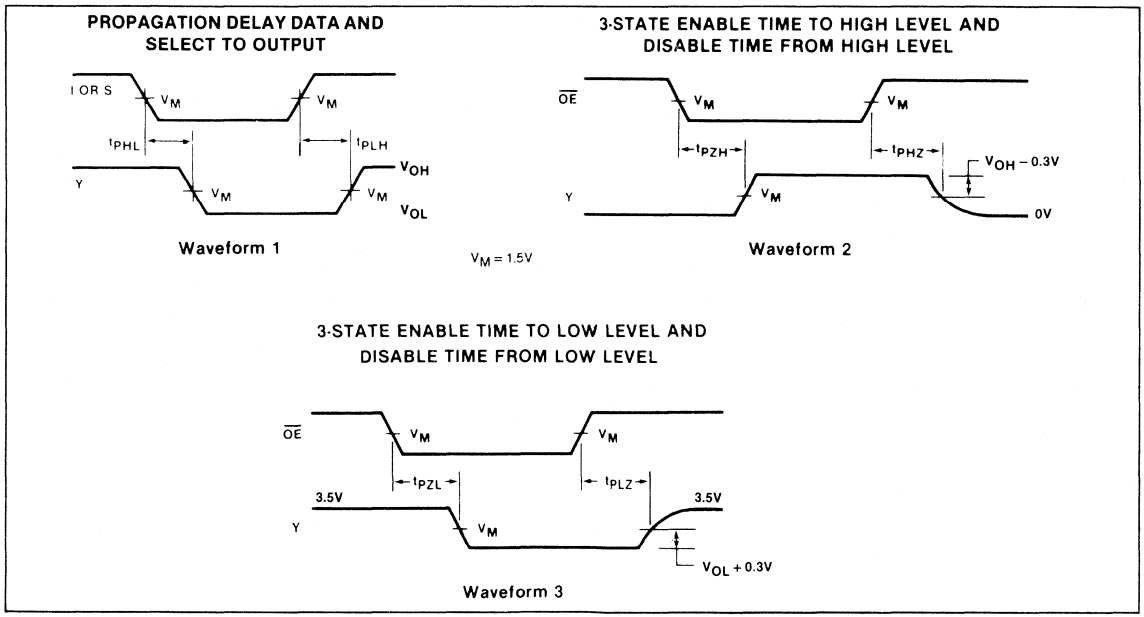
PARAMETER		TEST CONDITIONS	54/74F			54F		74F		UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	3.0	4.5	6.0	3.0	8.0	3.0	7.0	ns
t_{PHL}	Data to output		2.5	4.2	5.5	2.5	8.0	2.5	6.5	
t_{PLH}	Propagation delay	Waveform 1	4.5	10.1	13.0	4.5	15.5	4.5	15.0	ns
t_{PHL}	Select to output		3.5	6.5	8.5	3.5	10.5	3.5	9.5	
t_{PZH}	Output enable to HIGH level	Waveform 2	3.0	5.9	7.5	3.0	9.5	3.0	8.5	ns
t_{PZL}	Output enable to LOW level	Waveform 3	2.5	5.5	7.5	3.0	10.0	3.0	8.5	ns
t_{PHZ}	Output disable from HIGH level	Waveform 2	2.0	4.3	6.0	2.0	7.0	2.0	7.0	ns
t_{PLZ}	Output disable from LOW level	Waveform 3	2.0	4.5	6.0	2.0	9.5	2.0	7.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

APPLICATION



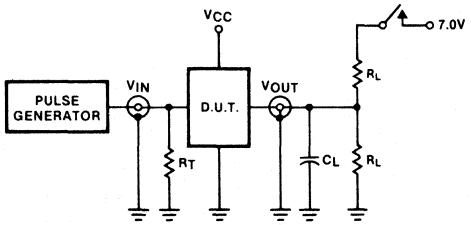
AC WAVEFORMS



5

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



SWITCH POSITION

Test	Switch 1
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

DEFINITIONS

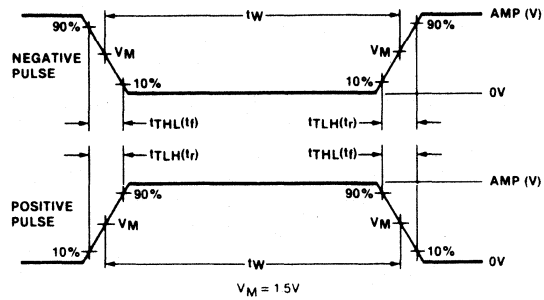
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

t_{TLH}, t_{THL} values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DATA SELECTOR/MULTIPLEXER FAST 54/74F258

Quad 2-Line To 1-Line Data Selector/Multiplexer (3-State)

- **Multifunction capability**
- **Inverting data path**
- **3-State outputs**
- **See 'F257 for non-inverting version**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F258	3.8ns	10.7mA

DESCRIPTION

The 'F258 has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the Select input is HIGH. Data appears at the outputs in inverted (complementary) form.

The 'F258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

Outputs are forced to a HIGH impedance "off" state when the Output Enable input ($\overline{OE}$) is HIGH. All but one device must be in the HIGH impedance state to avoid currents exceeding the maximum ratings if outputs of the 3-state devices are tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F258N	
Plastic SO	N74F258D	
Ceramic DIP		
Ceramic LLCC		

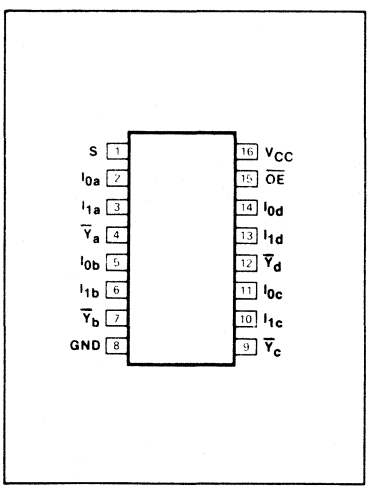
NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

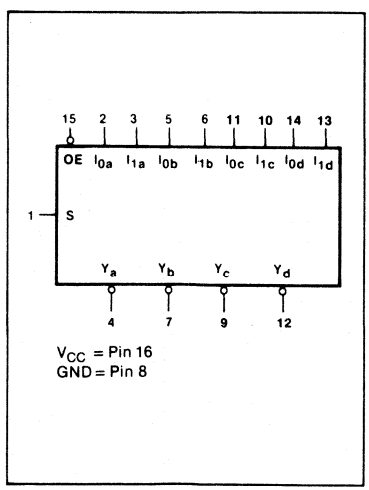
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
All	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}_a$-$\overline{Y}_d$	Outputs	150/40	1.0mA/24mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

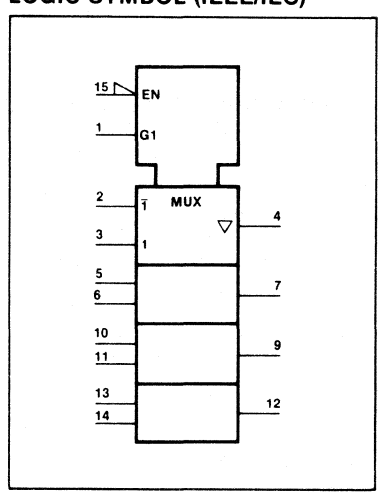
PIN CONFIGURATION



LOGIC SYMBOL

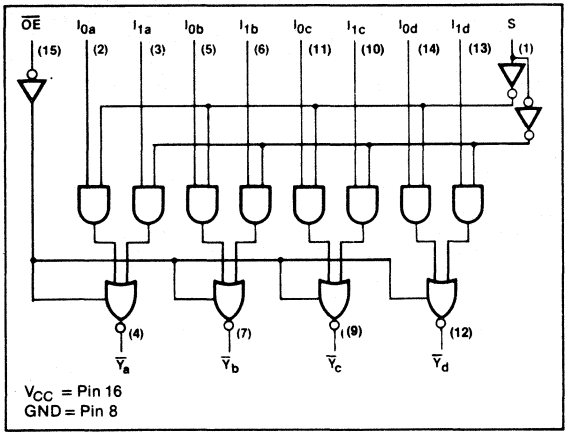


LOGIC SYMBOL (IEEE/IEC)



DATA SELECTOR/MULTIPLEXER FAST 54/74F258

LOGIC DIAGRAM



FUNCTION TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	(Z)
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + 5.5	− 0.5 to + 5.5	V
I_{OUT}	Current applied to output in LOW output state	40	48	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				-3	mA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F258			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = MAX	Mil	2.4			V
				Com'l	2.7			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 20mA	Mil		0.35	0.5	V
			I_{OL} = 24mA	Com'l		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 0.73	– 1.2	V
I_{OZH}	Off-stage output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V				2	50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				– 2	– 50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				– 0.4	– 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V			– 60	– 80	– 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		6.2	9.5	mA
			I_{CCL}	Outputs LOW		15.1	23.0	mA
			I_{CCZ}	Outputs OFF		11.3	17.0	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with all outputs open and all inputs grounded.

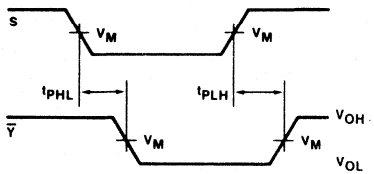
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F T_A, V_{CC} = Mil, C_L = 50pF, R_L = 500Ω		74F T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4	2.5 2.0	4.0 3.5	5.3 4.7	2.0 1.5	7.5 6.0	2.5 2.0	6.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveforms 1 & 4	4.0 4.0	6.5 7.3	8.5 9.5	4.0 4.0	12.0 11.5	4.0 4.0	9.5 11.0	ns
t_{PZH}	Output enable to HIGH level	Waveform 2	3.0	5.9	7.5	3.0	11.0	3.0	8.5	ns
t_{PZL}	Output enable to LOW level	Waveform 3	3.0	5.5	7.5	3.0	9.5	3.0	8.5	ns
t_{PHZ}	Output disable from HIGH level	Waveform 2	2.0	3.0	6.0	1.5	7.0	2.0	7.0	ns
t_{PLZ}	Output disable from LOW level	Waveform 3	2.0	4.5	6.0	2.0	9.0	2.0	7.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

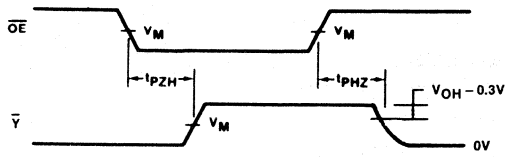
AC WAVEFORMS

PROPAGATION DELAY SELECT OUTPUT



Waveform 1

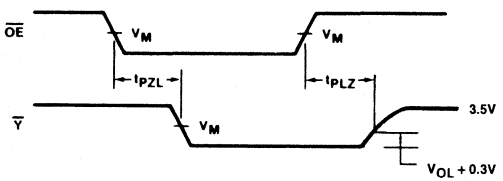
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

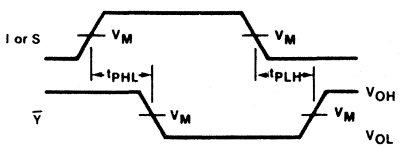
$V_M = 1.5V$

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

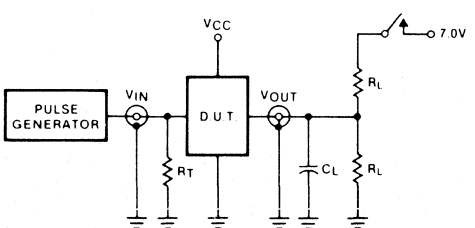
PROPAGATION DELAY DATA AND SELECT OUTPUT



Waveform 4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



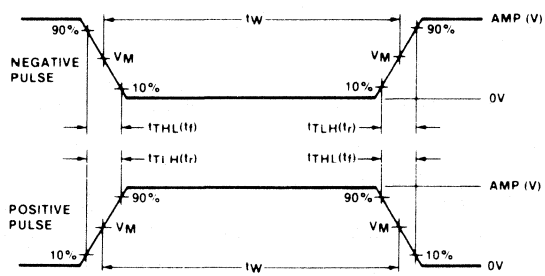
SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

8-Bit Addressable Latch

- **Combines demultiplexer and 8-bit latch**
- **Serial-to-parallel capability**
- **Output from each storage bit available**
- **Random (addressable) data entry**
- **Easily expandable**
- **Common Clear input**
- **Useful as a 1-of-8 active HIGH decoder**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F259	7.5ns	35mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74F259N	
Plastic SO	N74F259D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{MR}$, $\overline{E}$	Master Reset, Enable Inputs	1.0/1.0	20μA/0.6mA
A_0, A_2	Address Inputs	1.0/1.0	20μA/0.6mA
D	Data Input	1.0/1.0	20μA/0.6mA
Q_0-Q_7	Outputs	50/33	1mA/20mA

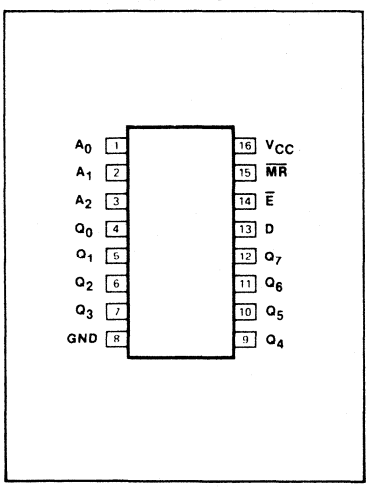
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

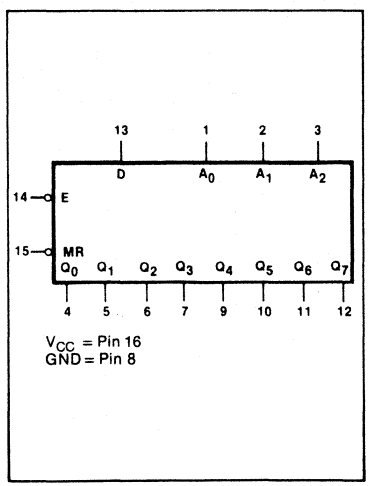
DESCRIPTION

The 'F259 dual addressable latch has four distinct modes of operation that are selectable by controlling the Master Reset and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode ($\overline{MR}$ = $\overline{E}$ = LOW), addressed outputs will follow the level of the D inputs, with all other outputs LOW. In the Master Reset mode, all outputs are LOW and unaffected by the Address and Data inputs.

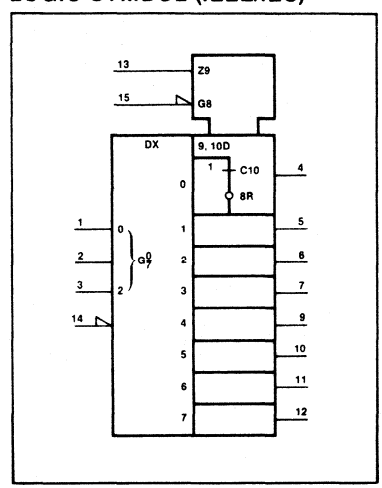
PIN CONFIGURATION



LOGIC SYMBOL



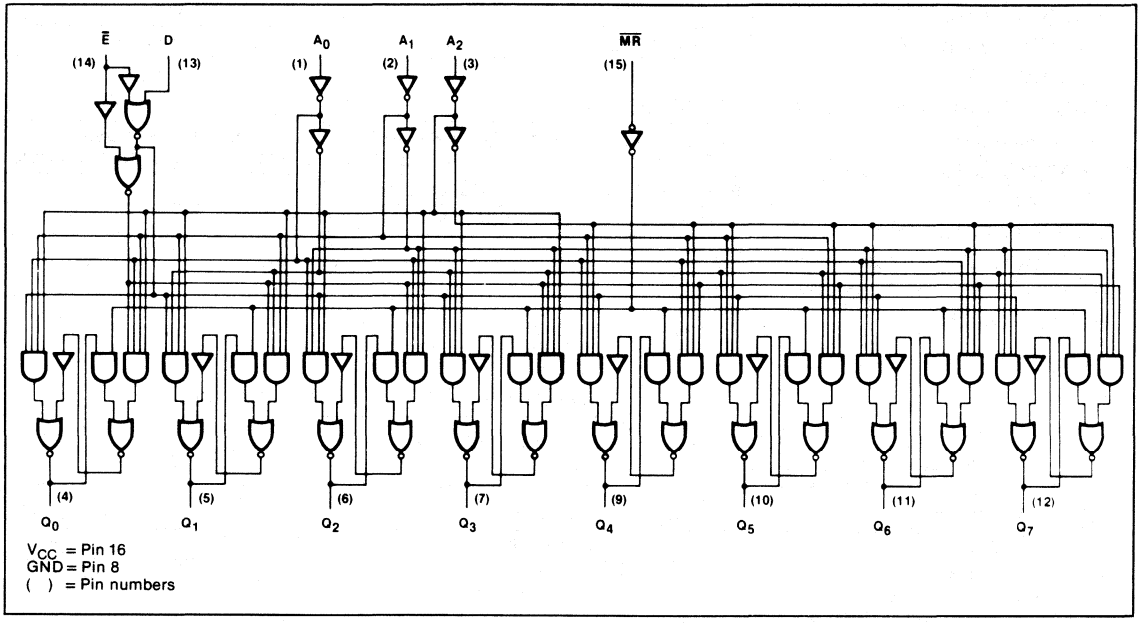
LOGIC SYMBOL (IEEE/IEC)



LATCH

FAST 54/74F259

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS							
	$\overline{CLR}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Master Reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (active HIGH decoder when D = H)	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q = d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q = d	L	L	L	L	L
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q = d
Store (do nothing)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
Addressable latch	H	L	d	L	L	L	Q = d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	L	L	q_0	Q = d	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	L	H	L	q_0	q_1	Q = d	q_3	q_4	q_5	q_6	q_7
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q = d

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
X = Don't care.
d = HIGH or LOW data one setup time prior to the LOW-to-HIGH Enable transition.
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

	PARAMETER	TEST CONDITIONS[1]			54/74F259			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−60	−90	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Output HIGH			40	mA
			I_{CCL}	Output LOW			75	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the inputs grounded and the outputs open.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			54F T_A, $V_{CC} = Mil$, $C_L = 50pF$, $R_L = 500\Omega$		74F T_A, $V_{CC} = Com'l$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} Enable to output	Waveform 1	6.0 3.0	8.0 5.0	10.5 7.0			6.0 3.0	12.0 7.0	ns
t_{PLH} Propagation delay t_{PHL} Data to output	Waveform 2	5.0 3.0	6.5 4.5	9.0 6.5			5.0 2.5	10.0 7.0	ns
t_{PLH} Propagation delay t_{PHL} Address to output	Waveform 3	5.0 4.0	9.5 6.5	13.0 9.0			5.0 4.0	14.5 9.5	ns
t_{PHL} Propagation delay Master Reset to output	Waveform 4	5.0	7.0	9.0			5.0	10.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

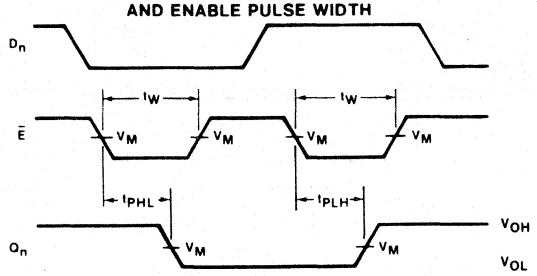
AC SETUP REQUIREMENTS

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			54F T_A, $V_{CC} = Mil$, $C_L = 50pF$, $R_L = 500\Omega$		74F T_A, $V_{CC} = Com'l$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_W Enable pulse width	Waveform 1	4.0			4.0		4.0		ns
t_W Master Reset pulse width	Waveform 4	4.0			4.0		4.0		ns
$t_s(H)$ Setup time HIGH, Data to Enable	Waveform 5	4.0			4.0		4.0		ns
$t_s(L)$ Setup time LOW, Data to Enable	Waveform 5	4.0			4.0		4.0		ns
$t_h(H)$ Hold time HIGH, Data to Enable	Waveform 5	1.0			1.0		1.0		ns
$t_h(L)$ Hold time LOW, Data to Enable	Waveform 5	1.0			1.0		1.0		ns
t_s Setup time, Address to Enable[a]	Waveform 6	4.0			4.0		4.0		ns
t_h Hold time, Address to Enable[b]	Waveform 6	0			0		0		ns

NOTES
a. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
b. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

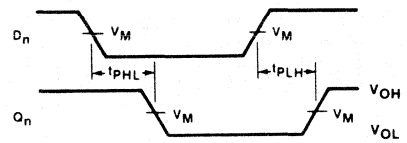
AC WAVEFORMS

PROPAGATION DELAY ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



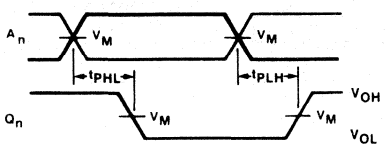
Waveform 1

PROPAGATION DELAY DATA TO OUTPUT



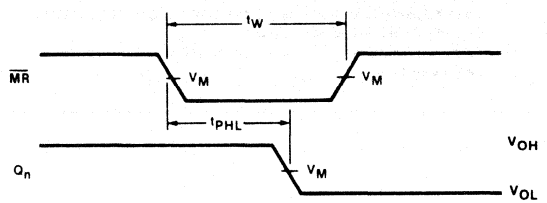
Waveform 2

PROPAGATION DELAY ADDRESS TO OUTPUT



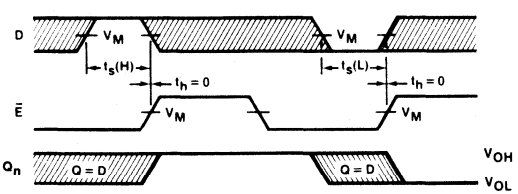
Waveform 3

MASTER RESET TO OUTPUT DELAY AND MASTER RESET PULSE WIDTH



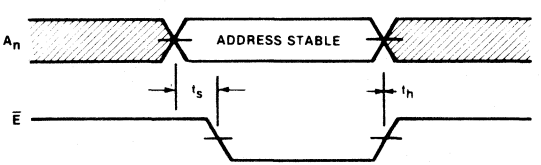
Waveform 4

DATA SETUP AND HOLD TIMES



Waveform 5

ADDRESS SETUP AND HOLD TIMES



Waveform 6

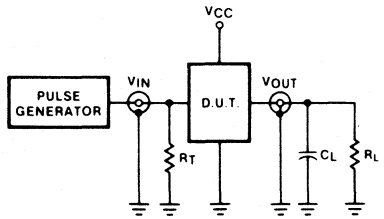
$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

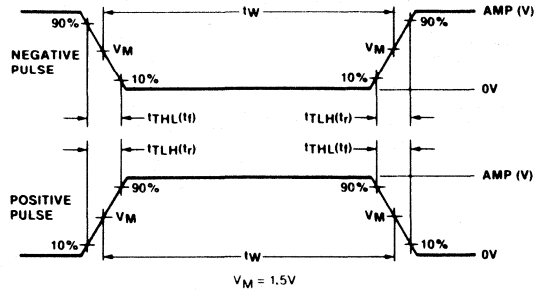
5

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

8-BIT COUNTER — FAST 54/74F269

Preliminary

8-Bit Bidirectional Binary Counter

- **Synchronous counting and loading**
- **Built-in lookahead carry capability**
- **Count frequency 100MHz typ**
- **Supply current 65mA typ**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F269	100MHz	65mA

DESCRIPTION

The 'F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to + 70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to + 125°C
Plastic DIP	N74F269N	
Plastic SO	N74F269D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

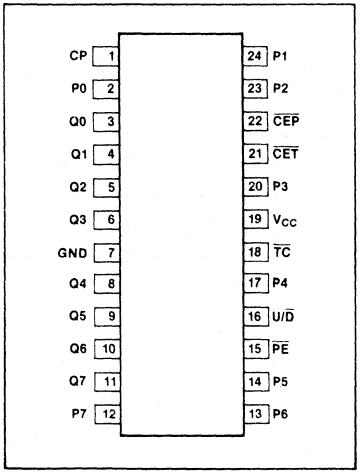
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
P_0-P_7	Parallel Data Inputs	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0	20μA/0.6mA
U/$\overline{D}$	Up-Down Count Control Input	1.0/1.0	20μA/0.6mA
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	1.0/1.0	20μA/0.6mA
CP	Clock Input	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal Count Output (Active LOW)	1.0/1.0	20μA/0.6mA
Q_0-Q_7	Flip-Flop Outputs	50/33	1mA/20mA

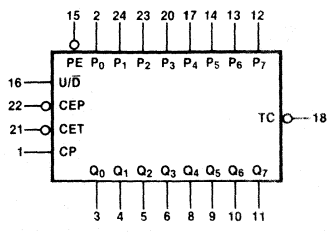
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

PIN CONFIGURATION



LOGIC SYMBOL



V_{CC} = Pin 19
GND = Pin 7

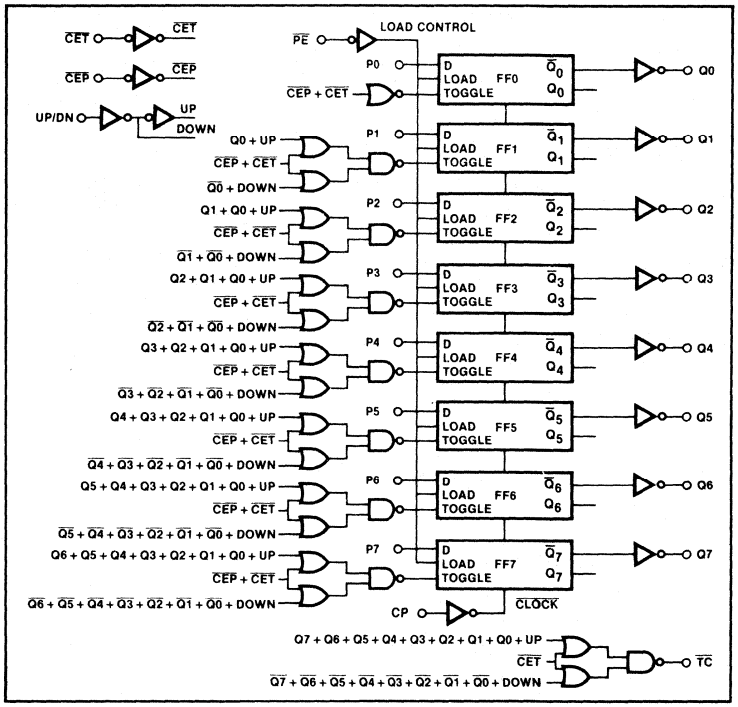
LOGIC SYMBOL (IEEE/IEC)

8-BIT COUNTER

FAST 54/74F269

Preliminary

LOGIC DIAGRAM



FUNCTION TABLE

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	CP	
L	X	X	X	∧	Parallel load all flip flops
H	H	X	X	∧	Hold
H	X	H	X	∧	Hold ($\overline{TC}$ held high)
H	L	L	H	∧	Count up
H	L	L	L	∧	Count down

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

8-BIT COUNTER FAST 54/74F269

Preliminary

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F269 Min	Typ[2]	Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			– 0.73	– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			– 0.4	– 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		– 60	– 115	– 150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		50	70	mA
			I_{CCL} Outputs LOW		80	100	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

5

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		60		70		MHz
t_{PLH}	CP to Qn	Waveform 1	3.0	6.0	10.0	2.5	12.0	2.5	11.0	ns
t_{PHL}	CP to Qn		4.5	7.5	10.0	4.0	12.0	4.0	11.0	
t_{PLH}	U/$\overline{D}$ to TC, CET to TC	Waveform 1	6.0	10.0	15.0	5.0	17.0	5.0	16.0	ns
t_{PHL}	CP to TC		5.0	8.0	15.0	4.0	17.0	4.0	16.0	

NOTE
Subtract 0.2ns from minimum values for SO package.

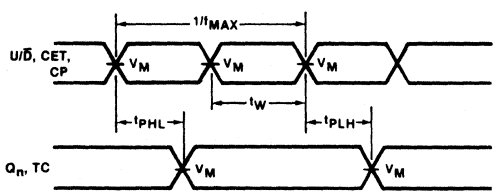
Preliminary

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Data to CP Data to CP	Waveform 2	5.0 5.0			6.0 6.0		5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Data to CP Data to CP	Waveform 2	0 0			0 0		0 0		ns
$t_s(H)$ $t_s(L)$	PE to CP PE to CP	Waveform 2	12 12			14 14		12 12		ns
$t_h(H)$ $t_h(L)$	PE to CP PE to CP	Waveform 2	0 0			0 0		0 0		ns
$t_s(H)$ $t_s(L)$	CET or CEP to CP CET or CEP to CP	Waveform 2	10 10			11 11		10 10		ns
$t_h(H)$ $t_h(L)$	CET or CEP to CP CEP or CET to CP	Waveform 2	0 0			0 0		0 0		ns
$t_w(H)$	Clock pulse width	Waveform 1	5			7		6		ns

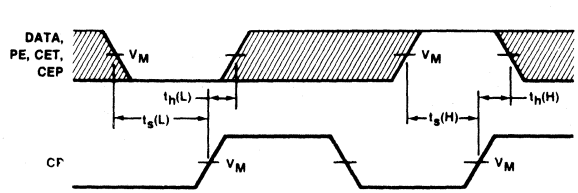
AC WAVEFORMS

U/$\overline{D}$, CET, CP TO OUTPUT Q_n, TC DELAYS AND CLOCK PULSE WIDTH



Waveform 1

DATA SETUP AND HOLD TIMES



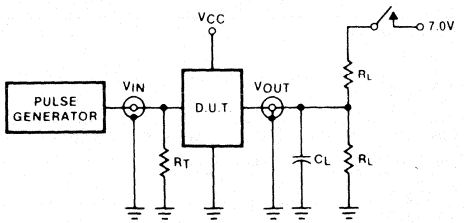
Waveform 2

$V_M = 1.5V$

Preliminary

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



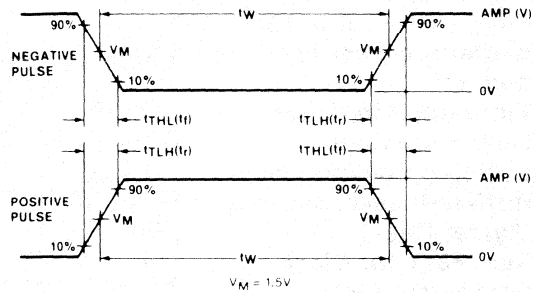
SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

FLIP-FLOP

FAST 54/74F273

Preliminary

Octal D Flip-Flop

- **High impedance NPN base inputs for reduced loading (20μA in LOW and HIGH states)**
- **Ideal buffer for MOS microprocessor or memory**
- **Eight edge-triggered D-type flip-flops**
- **Buffered common clock**
- **Buffered, asynchronous Master Reset**
- **See 'F377 for Clock Enable version**
- **See 'F373 for transparent latch version**
- **See 'F374 for 3-State version**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F273		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F273N	
Plastic SO	N74F273D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
D_0–D_7	Data Inputs	1.0/0.033	20μA/20μA
$\overline{MR}$	Master Reset (Active LOW)	1.0/0.033	20μA/20μA
CP	Clock Pulse Input (Active Rising Edge)	1.0/0.033	20μA/20μA
Q_0–Q_7	Data Outputs	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

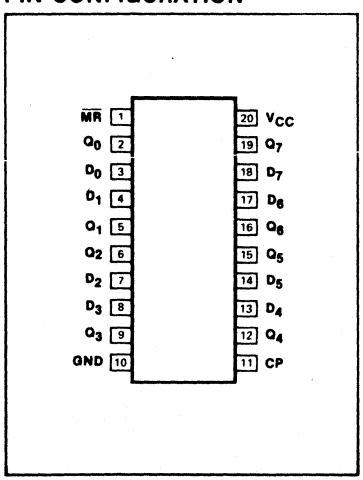
DESCRIPTION

The 'F273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

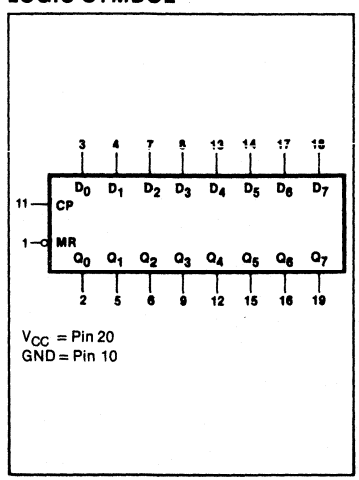
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

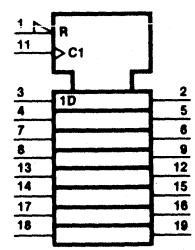
PIN CONFIGURATION



LOGIC SYMBOL



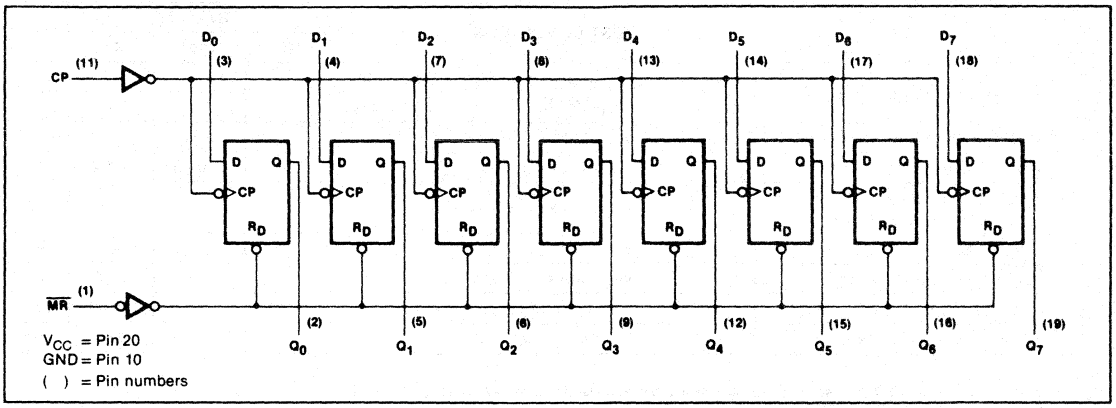
LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOP FAST 54/74F273

Preliminary

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

5

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

FLIP-FLOP

FAST 54/74F273

Preliminary

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F273			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = MAX	Mil	2.5			V
			Com'l	2.7			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			− 0.73	− 1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				− 20	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		− 40		− 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			50	60	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
4. Measure I_{CC} after a momentary ground, then 4.5V is applied to clock with all outputs open and 4.5V applied to all Data inputs and the Master Reset input.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			54F T_A, V_{CC} Mil C_L = 50pF R_L = 500Ω		74F T_A, V_{CC} Com'l C_L = 50pF R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	Waveform 1	100			70		80		MHz
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	Waveform 1		7 8				4.0 4.0	11 12	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Output	Waveform 2		8 8				4.0 4.0	12 12	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

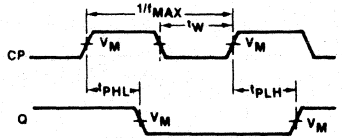
AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			54F T_A, V_{CC} Mil C_L = 50pF R_L = 500Ω		74F T_A, V_{CC} Com'l C_L = 50pF R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_w(L)	Clock pulse width (LOW)	Waveform 1						4		
t_w	Master Reset pulse width	Waveform 2						4		
t_s(H)	Setup time, HIGH data to CP	Waveform 3						3		
t_h(H)	Hold time, HIGH data to CP	Waveform 3						1		
t_s(L)	Setup time, LOW data to CP	Waveform 3						3		
t_h(L)	Hold time, LOW data to CP	Waveform 3						1		
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2						3		

Preliminary

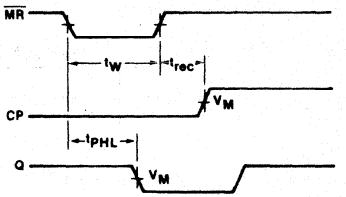
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



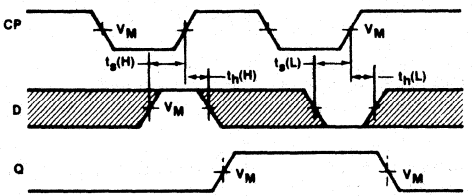
Waveform 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



Waveform 2

DATA SET-UP AND HOLD TIMES



Waveform 3

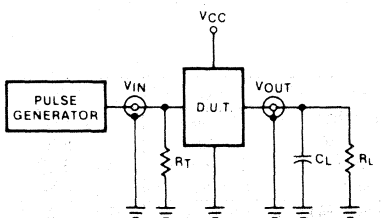
$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

5

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



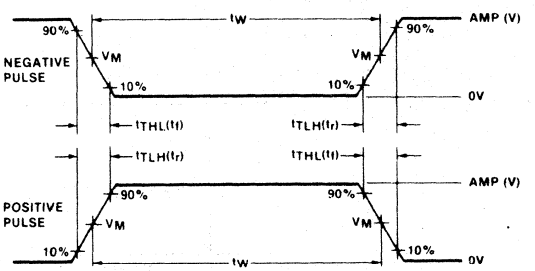
DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

PARITY GENERATOR/CHECKER — FAST 54/74F280A

9-Bit Odd/Even Parity Generator/Checker

- **High impedance NPN base inputs for reduced loading (20μA in LOW and HIGH states)**
- **Buffered inputs — one normalized load**
- **Word length easily expanded by cascading**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT
74F280A	9.0 ns	26 mA

DESCRIPTION

The 'F280A is a 9-bit parity generator or checker commonly used to detect errors in high-speed data transmission or data retrieval systems. Both Even and Odd parity outputs are available for generating or checking even or odd parity on up to 9 bits.

The Even parity output (Σ_E) is HIGH when an even number of Data inputs (I_0-I_8) are HIGH. The Odd parity output (Σ_O) is HIGH when an odd number of Data inputs are HIGH.

Expansion to larger word sizes is accomplished by tying the Even outputs (Σ_E) of up to nine parallel devices to the Data inputs of the final stage. This expansion scheme allows an 81-bit data word to be checked in less than 25ns with the 'F280A.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F280AN	
Plastic SO	N74F280AD	
Ceramic DIP		S54F280AF
Ceramic LLCC		S54F280AG

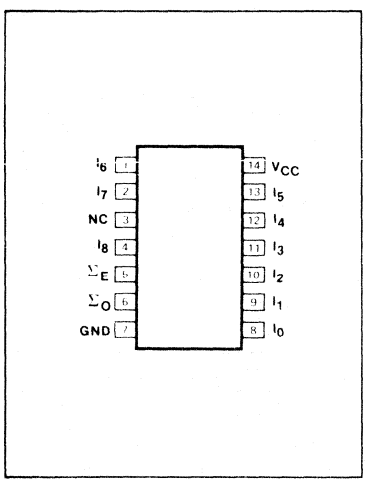
NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

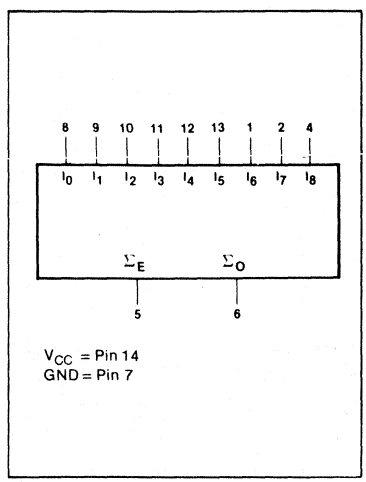
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
I_0-I_8	Data Inputs	1.0/0.033	20μA/20μA
Σ_E, Σ_O	Parity Outputs	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

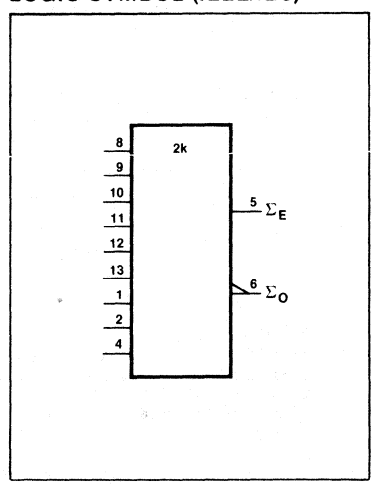
PIN CONFIGURATION



LOGIC SYMBOL

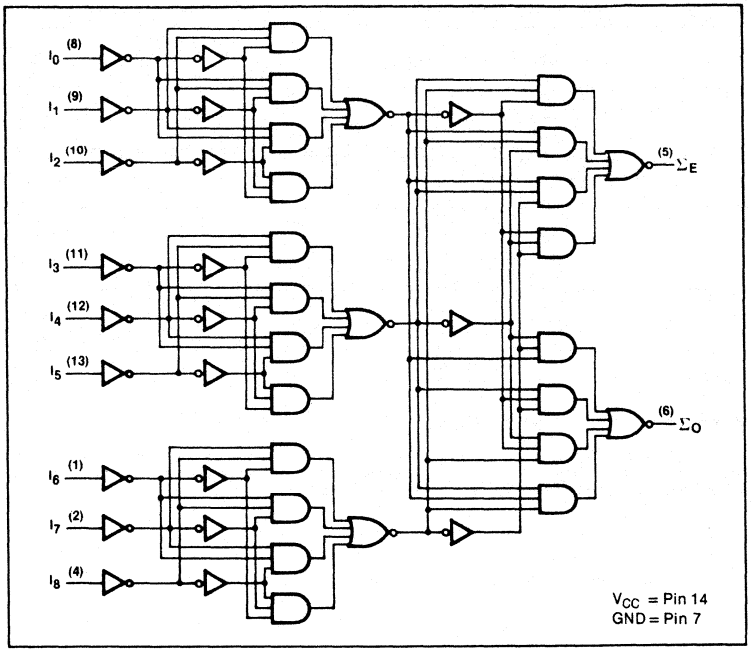


LOGIC SYMBOL (IEEE/IEC)



PARITY GENERATOR/CHECKER FAST 54/74F280A

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS	OUTPUTS	
Number of HIGH Data inputs (I_0–I_8)	Σ_E	Σ_O
Even — 0, 2, 4, 6, 8	H	L
Odd — 1, 3, 5, 7, 9	L	H

H = HIGH voltage level
L = LOW voltage level

5

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

PARITY GENERATOR/CHECKER — FAST 54/74F280A

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F280A			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				− 0.73	− 1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				0.5	1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				4.0	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−0.1	−20	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V			− 60	−114	− 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				26	35	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with all inputs grounded and all outputs open.

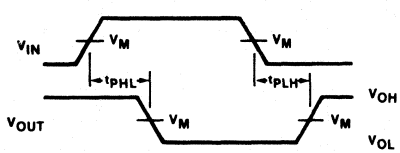
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F			54F		74F		UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A, V_{CC} = Mil, C_L = 50pF, R_L = 500Ω		T_A, V_{CC} = Com'l, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to Even output	Waveforms 1 & 2	5.0 9.0	7.0 11.1	9.0 13.0	5.0 7.0	11.0 17.0	5.0 7.5	10.0 14.5	ns
t_{PLH} t_{PHL}	Propagation delay Data to Odd output	Waveforms 1 & 2	6.5 7.0	8.6 9.1	10.5 11.0	6.5 5.0	12.0 16.0	6.5 6.0	11.0 13.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS

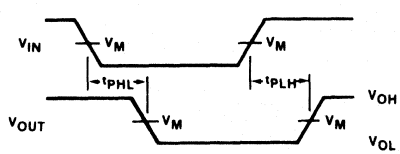
WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.5V

Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS

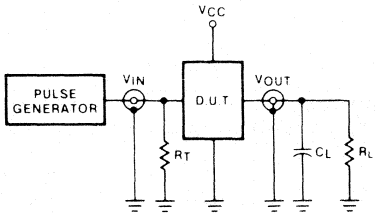


V_M = 1.5V

Waveform 2

TEST CIRCUITS AND WAVEFORMS

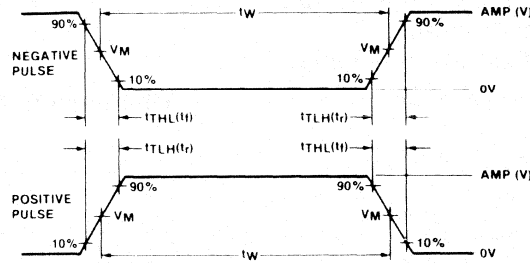
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

4-BIT ADDER — FAST 54/74F283

Preview

4-Bit Binary Full Adder With Fast Carry

- **High-speed 4-bit binary addition**
- **Cascadable in 4-bit increments**
- **Fast internal carry lookahead**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F283		

DESCRIPTION

The 'F283 adds two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the Sum outputs ($\Sigma_1 - \Sigma_4$) and the outgoing carry (C_{OUT}) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

where (+) = plus.

Due to the symmetry of the binary add function, the 'F283 can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic)—see Function Table. In case of all active LOW operands the results Σ_1-Σ_4 and C_{OUT} should be interpreted also as active LOW. With active HIGH inputs, C_{IN} cannot be left open; it must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus C_{IN}, A_1, B_1 can arbitrarily be assigned to pins 5, 6, 7, etc.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F283N	
Plastic SO	N74F283D	
Ceramic DIP		S54F283F
Ceramic LLCC		S54F283G

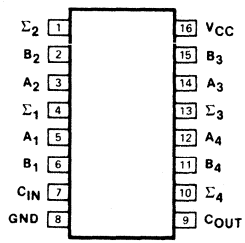
NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

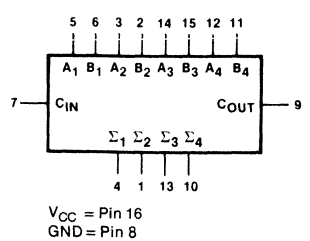
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A_1–A_4	A Operand Inputs	1.0/2.0	20μA/1.2mA
B_1–B_4	B Operand Inputs	1.0/2.0	20μA/1.2mA
C_{IN}	Carry Input	1.0/1.0	20μA/0.6mA
Σ_1–Σ_4	Sum Outputs	50/33	1.0mA/20mA
C_{OUT}	Carry Output	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and the 0.6mA in the LOW state.

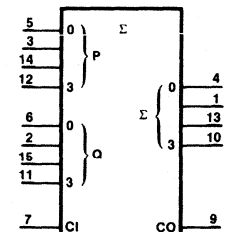
PIN CONFIGURATION



LOGIC SYMBOL



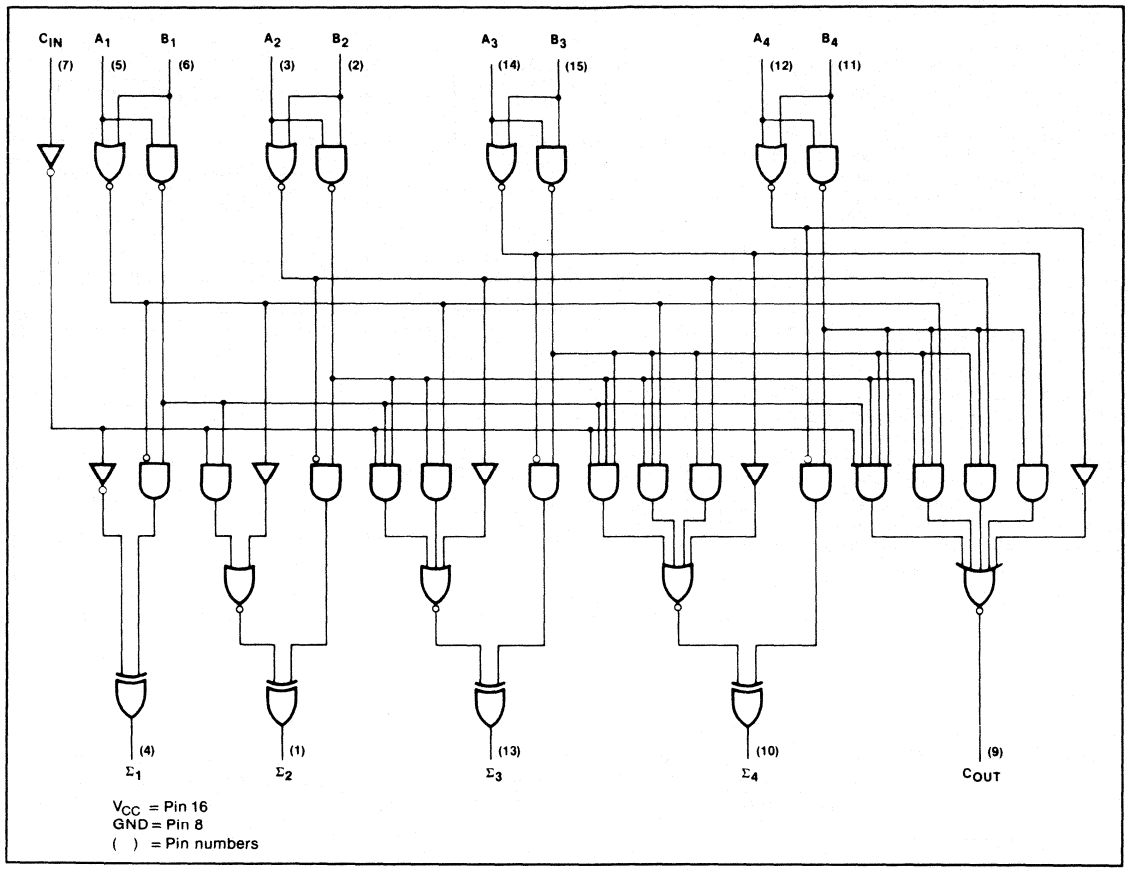
LOGIC SYMBOL (IEEE/IEC)



4-BIT ADDER FAST 54/74F283

Preview

LOGIC DIAGRAM



FUNCTION TABLE

PINS	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

H = LOW voltage level
L = LOW voltage level

Example:
1001
1010
10011
(10 + 9 = 19)
(carry + 5 + 6 = 12)

5

4-BIT ADDER

FAST 54/74F283

Preview

Due to pin limitations, the intermediate carries of the 'F283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure a shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3, B_3) LOW makes S_3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure b shows a way of dividing the 'F283 into a 2-bit and a 1-bit adder. The third stage adder (A_2, B_2, S_2) is used merely as a means of getting a carry (C_{10}) signal into the fourth stage (via A_2 and B_2) and bringing out the carry from the second stage on S_2. Note that as long as A_2 and B_2 are the same, whether HIGH or LOW, they do not influence S_2. Similarly, when A_2 and B_2 are the same the carry into the third stage does not influence the carry out of the third stage. Figure c shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S_0, S_1 and S_2 present a binary number equal to the number of inputs I_1–I_5 that are true. Figure d shows one method of implementing a 5-input majority gate. When three or more of the inputs I_1–I_5 are true, the output M_5 is true.

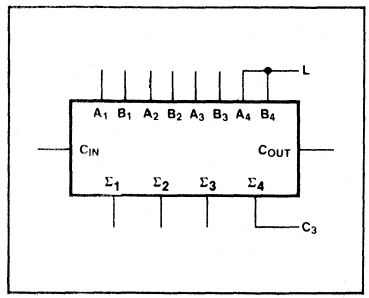


Figure a. 3-Bit Adder

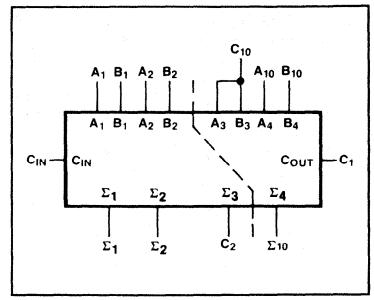


Figure b. 2-Bit and 1-Bit Adders

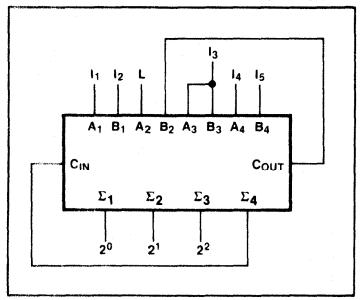


Figure c. 5-Input Encoder

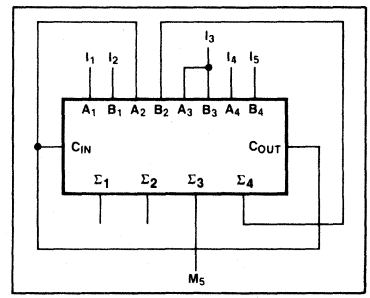


Figure d. 5-Input Majority Gate

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

4-BIT ADDER FAST 54/74F283

Preview

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	– 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F283			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			– 0.73	– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	A_1-A_4, B_1-B_4			– 1.2	mA
			C_{IN}		– 0.4	– 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		– 60	– 80	– 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				55	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} should be measured with all outputs open and the following conditions:
   Condition 1: all inputs grounded
   Condition 2: all B inputs LOW, other inputs at 4.5V
   Condition 3: all inputs at 4.5V.

5

4-BIT ADDER

FAST 54/74F283

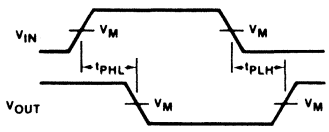
Preview

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_i	Waveforms 1 and 2	3.5 4.0	7.0 7.0	9.9 9.5	3.5 4.0	14.0 14.0	3.5 4.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to Σ_i	Waveforms 1 and 2	4.0 3.5	7.0 7.0	9.5 9.5	4.0 3.5	14 14	4.0 3.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to C_{OUT}	Waveform 2	3.5 3.0	5.7 5.4	7.5 7.0	3.5 3.0	10.5 10	3.5 3.0	8.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to C_{OUT}	Waveforms 1 and 2	3.5 3.0	5.7 5.3	7.5 7.0	3.5 3.0	10.5 10	3.5 3.0	8.5 8.0	ns

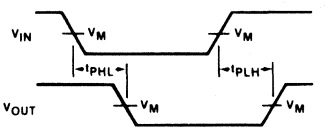
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS

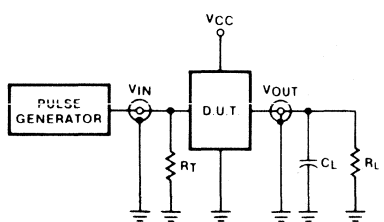


Waveform 2

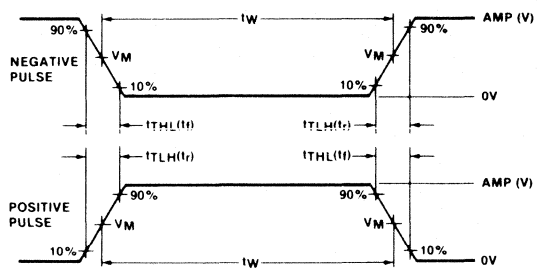
V_M = 1.5V

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



V_M = 1.5V

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

MULTIPLEXER

FAST 54/74F298

Preliminary

Quad 2-Input Multiplexer With Storage

- **Fully synchronous operation**
- **Select from two data sources**
- **Buffered, negative edge triggered clock**

TYPE	TYPICAL, f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F298	105MHz	36mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F298N	
Plastic SO	N74F298D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

This device is a high-speed Multiplexer with storage. It selects 4 bits of data from two sources (Ports) under the control of a common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). The 4-bit register is fully edge triggered. The Data inputs (I_0 and I_1) and Select input (S) must be stable only one setup time prior to the HIGH-to-LOW transition of the clock for predictable operation.

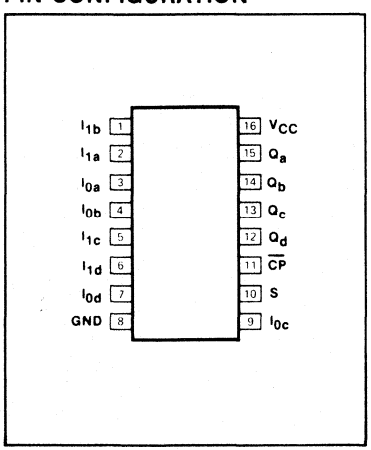
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
I_{1a}, I_{1b}, I_{1c}, I_{1d}	Data Inputs	1.0/1.0	20μA/0.6mA
I_{0a}, I_{0b}, I_{0c}, I_{0d}	Data Inputs	1.0/1.0	20μA/0.6mA
S	Select Input	1.0/1.0	20μA/0.6mA
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	1.0/1.0	20μA/0.6mA
Q_a, Q_b, Q_c, Q_d	Outputs	50/33	1.0mA/20mA

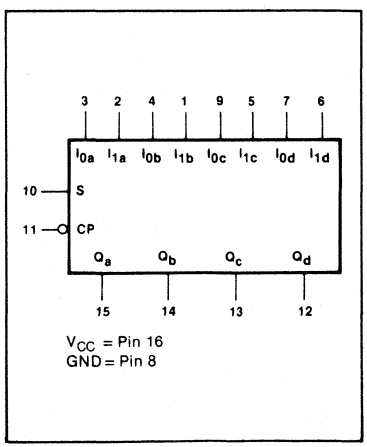
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

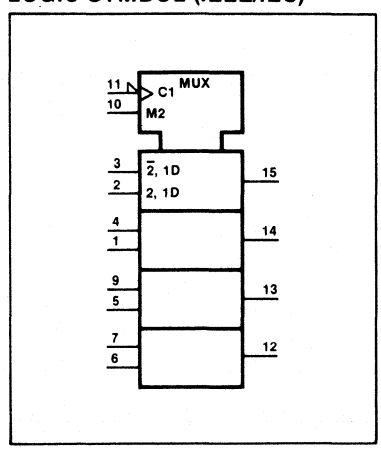
PIN CONFIGURATION



LOGIC SYMBOL



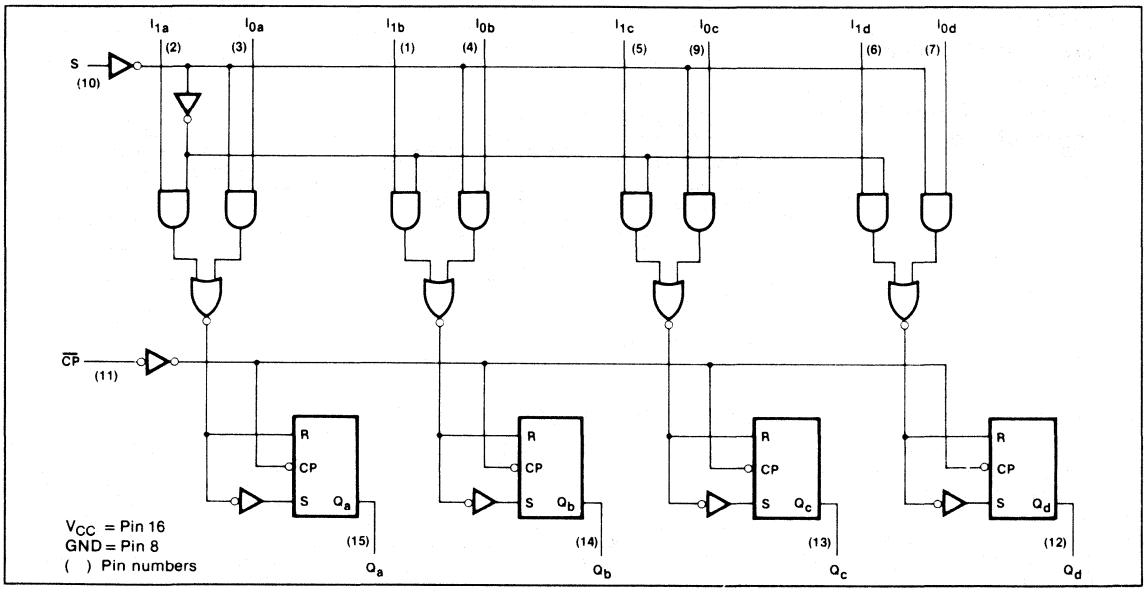
LOGIC SYMBOL (IEEE/IEC)



MULTIPLEXER FAST 54/74F298

Preliminary

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

MULTIPLEXER FAST 54/74F298

Preliminary

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]		54/74F298 Min	54/74F298 Typ[2]	54/74F298 Max	UNIT
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
		Com'l	2.7	3.4		V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			– 0.73	– 1.2	V
I_I Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH} HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL} LOW-level input current	V_{CC} = MAX, V_I = 0.5V			– 0.4	– 0.6	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX		– 60	– 80	– 150	mA
I_{CC} Supply current[4] (total)	V_{CC} = MAX			36	46	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured after applying a momentary 4.5V followed by ground to the Clock input, with all other inputs LOW and all outputs open.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} = Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} = Com'l, C_L = 50pF, R_L = 500Ω		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Waveform 1	105			90		90		MHz
t_{PLH} Propagation delay, Clock to Output	Waveform 1	3.5		7.0	3.0	10.0	3.5	9.0	ns
t_{PHL} Propagation delay, Clock to Output	Waveform 1	3.5		7.0	3.0	10.0	3.5	9.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC SETUP REQUIREMENTS

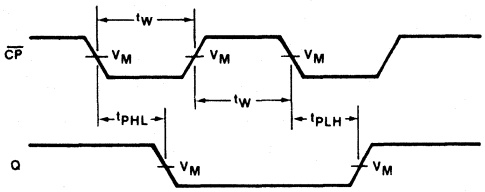
PARAMETER	TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} = Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} = Com'l, C_L = 50pF, R_L = 500Ω		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_W Clock pulse width	Waveform 1	5.0			5.0		5.0		ns
t_s Setup time, Data to Clock	Waveform 2	4.0			4.0		4.0		ns
t_h Hold time, Data to Clock	Waveform 2	0			1.0		1.0		ns
t_s Setup time, Select to Clock	Waveform 2	8.0			9.0		9.0		ns
t_h Hold time, Select to Clock	Waveform 2	0			0		0		ns

MULTIPLEXER FAST 54/74F298

Preliminary

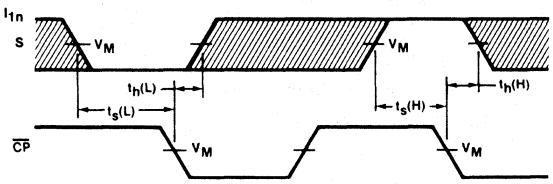
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

DATA SETUP AND HOLD TIMES



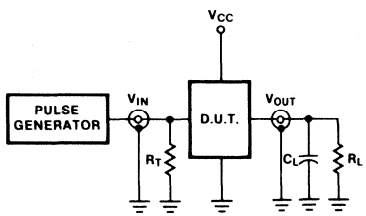
Waveform 2

$V_M = 1.5V$

The shaded ares indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

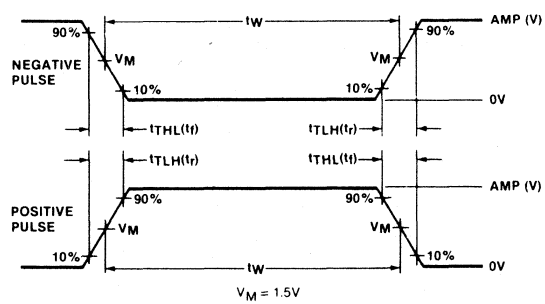
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND, see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Preview

8-Input Universal Shift/Storage Register (3-State)

- **Common parallel I/O for reduced pin count**
- **Additional Serial inputs and outputs for expansion**
- **Four operating modes: Shift Left, Shift Right, Load and Store**
- **3-State outputs for bus-oriented applications**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F299		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F299N	
Plastic SO	N74F299D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F299 is an 8-bit universal shift/storage register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. A separate active-LOW Master Reset is used to reset the register.

The 'F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

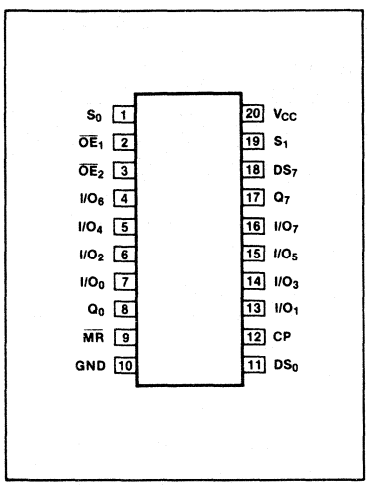
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA0.6mA
DS_0	Serial Data Input for Right Shift	1.0/1.0	20μA/0.6mA
DS_7	Serial Data Input for Left Shift	1.0/1.0	20μA/0.6mA
S_0, S_1	Mode Select Inputs	1.0/2.0	20μA/1.2mA
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)	1.0/1.0	20μA/0.6mA
I/O_0, I/O_7	Parallel Data Inputs or 3-State Parallel Outputs	1.0/1.0 150/33	20μA/0.6mA 3.0mA/20mA
Q_0, Q_7	Serial Outputs	50/33	1.0mA/20mA

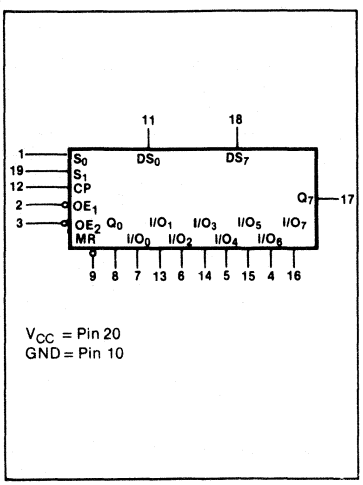
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

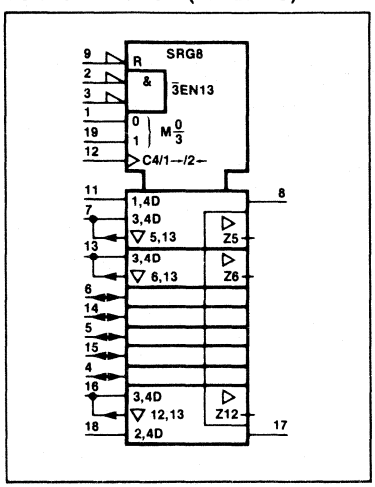
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



REGISTER

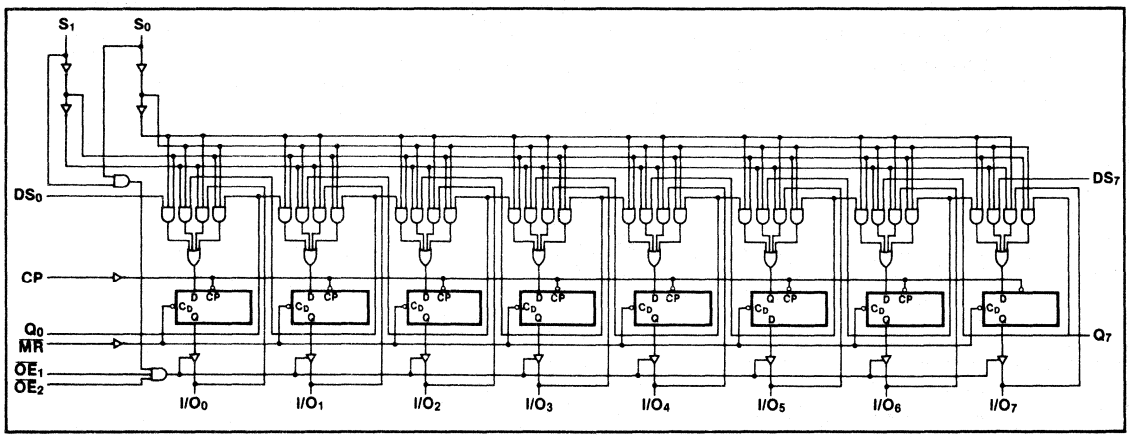
FAST 54/74F299

Preview

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				RESPONSE
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; $Q_0 - Q_7$ = LOW
H	H	H	↑	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	↑	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	↑	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

Preview

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 3	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	– 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F299			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX	I_{OH} = MAX	Mil	2.4			V
				Com'l	2.7			V
			I_{OH} = – 1mA	Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 0.73	– 1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V				2	0	μA
I_{OZL}	Off-state output current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				– 2	– 650	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	S_0, S_1				– 1.2	mA
			Other inputs			– 0.4	– 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 60	– 80	– 150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH				mA
			I_{CCL}	Outputs LOW			92	mA
			I_{CCZ}	Outputs OFF				mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Preview

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Input Frequency	Waveform 2	70	100				70		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	Waveform 2	4.0 3.5	7.0 6.5	9.0 8.5			4.0 3.5	10 9.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n	Waveform 2	4.0 5.0	7.0 8.5	9.0 11			4.0 5.0	10 12	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	Waveform 3	4.5	7.5	9.5			4.5	10.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	Waveform 3	6.5	11	14			6.5	15	ns
t_{PZH} t_{PZL}	Output Enable Time	Waveform 4 Waveform 5	3.5 4.0	6.0 7.0	8.0 10.0			3.5 4.0	9.0 11	ns
t_{PHZ} t_{PLZ}	Output Disable Time	Waveform 4 Waveform 5	2.5 2.0	4.5 4.0	6.0 5.5			2.5 2.0	7.0 6.5	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

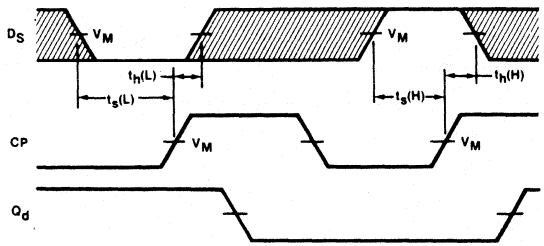
AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_s (H) t_s (L)	Setup Time, HIGH or LOW S_0 or S_1 to CP	Waveform 1	8.5 8.5					8.5 8.5		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW S_0 or S_1 to CP	Waveform 1	0 0					0 0		ns
t_s (H) t_s (L)	Setup Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	Waveform 1	5.0 5.0					5.0 5.0		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	Waveform 1	2.0 2.0					2.0 2.0		ns
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	Waveform 2	7.0 7.0					7.0 7.0		ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	Waveform 3	7.0					7.0		ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	Waveform 3	7.0					7.0		ns

Preview

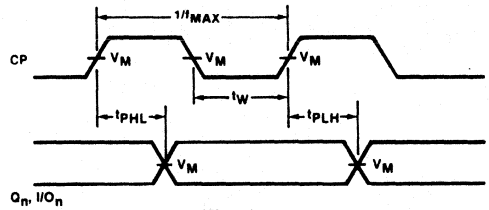
AC WAVEFORMS

DATA SETUP AND HOLD TIMES



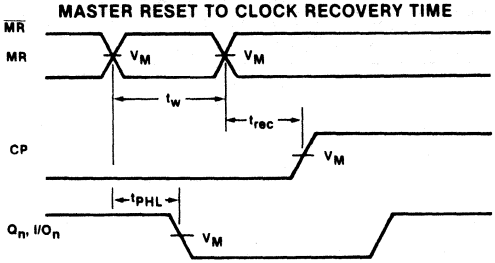
Waveform 1

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



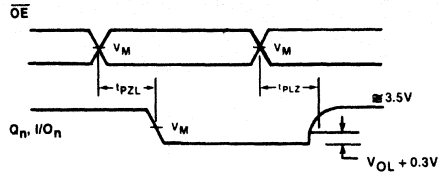
Waveform 2

MASTER RESET PULSE WIDTH
MASTER RESET TO OUTPUT DELAY &
MASTER RESET TO CLOCK RECOVERY TIME



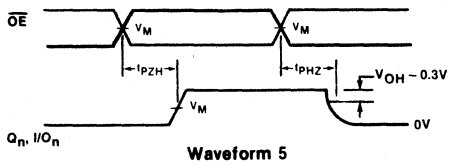
Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 5

V_M = 1.5V

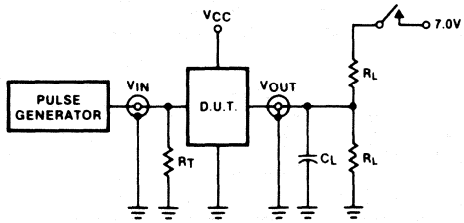
The shaded areas indicate when the input is permitted to change for predictable output performance.

5

Preview

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

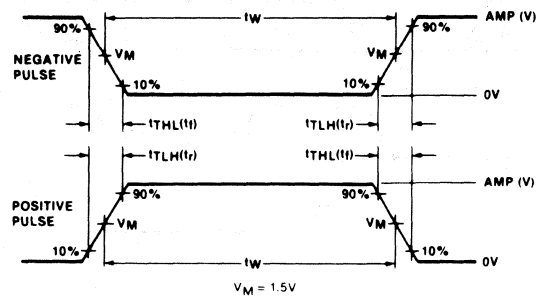
DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Preview

8-Bit Serial/Parallel Register With Sign Extend (3-State)

- **Multiplexed parallel I/O ports**
- **Separate Serial input and output**
- **Sign extend function**
- **3-State outputs for bus applications**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F322		60mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F322N	
Plastic SO	N74F322D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F322 is an 8-bit shift register with provision for either serial or parallel loading and with 3-State parallel outputs plus a bi-state Serial output. Parallel Data inputs and outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with sign extend, and parallel load. An asynchronous Master Reset ($\overline{M}/\overline{R}$) input overrides clocked operation and clears the register.

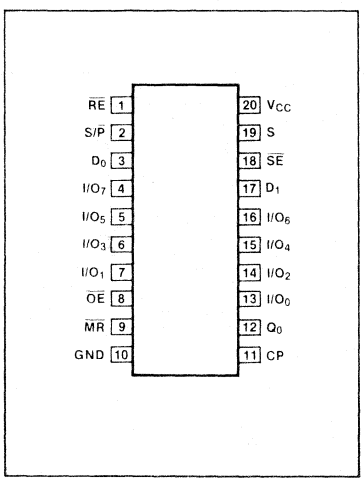
The 'F322 contains eight D-type edge-triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A LOW signal on $\overline{RE}$ enables shifting or parallel loading, while a HIGH signal enables the hold mode. A HIGH signal on S/$\overline{P}$ enables shift right, while a LOW signal disables the 3-State output buffers and enables parallel

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

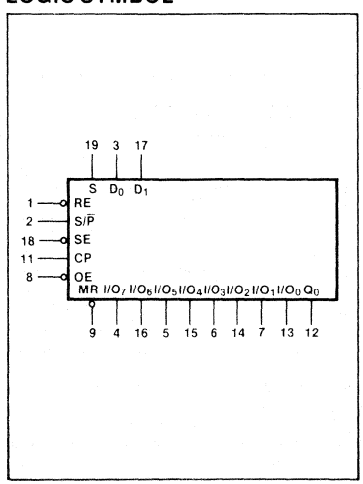
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{RE}$	Register Enable Input (Active LOW)	1.0/1.0	20μA/0.6mA
S/$\overline{P}$	Serial (HIGH) or Parallel (LOW) Mode Control Input	1.0/1.0	20μA/0.6mA
$\overline{SE}$	Sign Extend Input (Active LOW)	1.0/3.0	20μA/1.8mA
S	Serial Data Select Input	1.0/2.0	20μA/1.2mA
D_0, D_1	Serial Data Inputs	1.0/1.0	20μA/0.6mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	3-State Output Enable Input (Active LOW)	1.0/1.0	20μA/0.6mA
Q_0	Bi-state Serial Output	50/33	1.0mA/20mA
I/O_0-I/O_7	Multiplexed Parallel Data Inputs or	1.0/1.0	20μA/0.6mA
	3-State Parallel Data Outputs	150/33	3.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as 20μA in the HIGH state and 0.6mA in the LOW state.

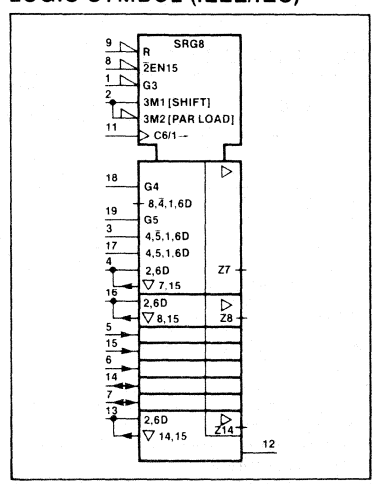
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



5

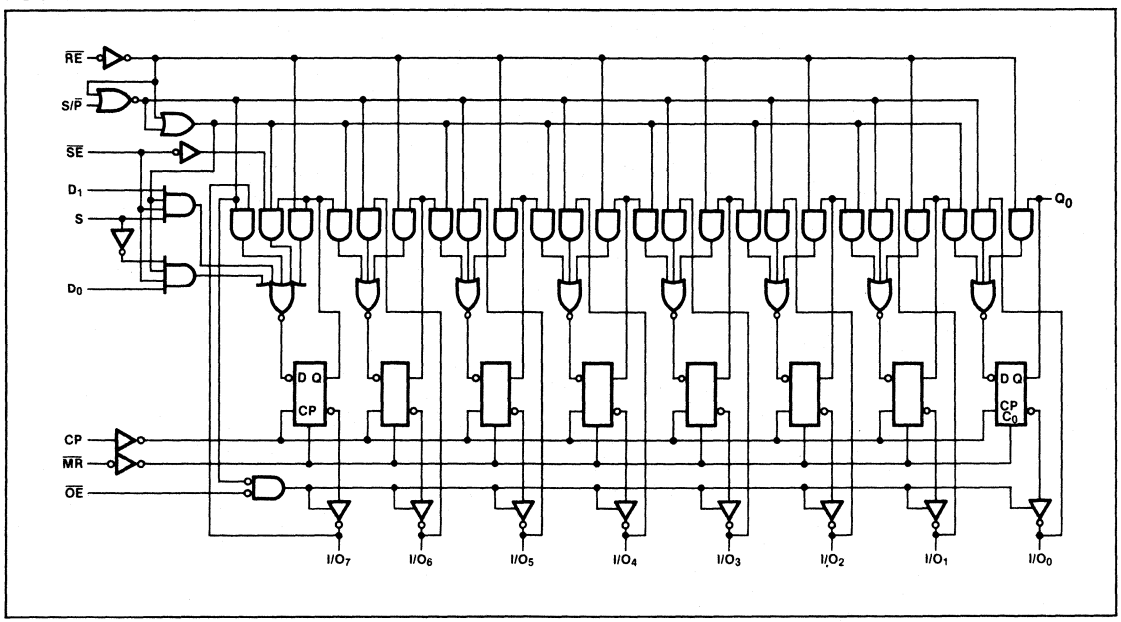
REGISTER

FAST 54/74F322

Preview

loading. In the shift right mode a HIGH signal on $\overline{SE}$ enables serial entry from either D_0 or D_1, as determined by the S input. A LOW signal on $\overline{SE}$ enables shift right but Q_7 reloads its contents, thus performing the sign extend function required for the 'LS384 Two's Complement Multiplier. A HIGH signal on $\overline{OE}$ disables the 3-State output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

LOGIC DIAGRAM



FUNCTION TABLE

MODE	INPUTS							OUTPUTS								
	$\overline{MR}$	$\overline{RE}$	S/$\overline{P}$	$\overline{SE}$	S	$\overline{OE}$*	CP	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Q_0
Clear	L	X	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	X	X	X	X	H	X	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel Load	H	L	L	X	X	X	↑	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	I_0
Shift Right	H	L	H	H	L	L	↑	D_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
	H	L	H	H	H	L	↑	D_1	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
Sign Extend	H	L	H	L	X	L	↑	O_7	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
Hold	H	H	X	X	X	L	↑	NC	NC	NC	NC	NC	NC	NC	NC	NC

*When the $\overline{OE}$ input is HIGH, all I/O_n terminals are at the high-impedance state; sequential operation or clearing of the register is not affected.

NOTES

1. I_7-I_0 = The level of the steady-state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q_0) are isolated from the I/O terminal.
2. D_0, D_1 = The level of the steady-state inputs to the serial multiplexer input.
3. O_7-O_0 = The level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.
4. NC = No change; Z = High-Impedance Output State; H = HIGH Voltage Level; L = LOW Voltage Level; ↑ = LOW-to-HIGH Clock Transition.
5. ↑ = LOW-to-HIGH clock transition.

Preview

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−3	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

5

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F322			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V			2	70	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−650	μA
I_I	Inputcurrent at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	$\overline{SE}$ Input			−1.8	mA
			S Input			−1.2	mA
			Other Inputs		−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX, CP = HIGH, Output Disabled			60	84	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Preview

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	70	90				70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4 5	7 8.5	9 11			4 5	10 12	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_0	Waveform 1	3.5 3.5	7 7	9 9			3.5 3.5	10 10	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n	Waveform 3	6	10	13			6	14	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_0	Waveform 3	5.5	9.5	12.0			5.5	13	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to I/O_n	Waveform 4 Waveform 5	3 4	6.5 8.5	9 11			3 4	10 12	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to I/O_n	Waveform 4 Waveform 5	2 2	4.5 5	6 7			2 2	7 8	ns
t_{PZH} t_{PZL}	Output enable time $S/\overline{P}$ to I/O_n	Waveform 4 Waveform 5	4.5 5.5	8 10	10.5 14			4.5 5.5	11.5 15	ns
t_{PHZ} t_{PLZ}	Output disable time $S/\overline{P}$ to I/O_n	Waveform 4 Waveform 5	5 6	9 12	11.5 15.5			5 6	12.5 16.5	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

Preview

AC SETUP REQUIREMENTS

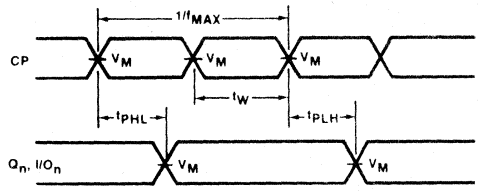
PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ Setup time, HIGH or LOW $t_s(L)$ $\overline{RE}$ to CP	Waveform 2	12 12					13 13		ns
$t_h(H)$ Hold time, HIGH or LOW $t_h(L)$ $\overline{RE}$ to CP	Waveform 2	0 0					0 0		ns
$t_s(H)$ Setup time, HIGH or LOW $t_s(L)$ D_0, D_1 or I/O_n to CP	Waveform 2	8 8					9 9		ns
$t_h(H)$ Hold time, HIGH or LOW $t_h(L)$ D_0, D_1 or I/O_n to CP	Waveform 2	2 2					3 3		ns
$t_s(H)$ Setup time, HIGH or LOW $t_s(L)$ $\overline{SE}$ to CP	Waveform 2	7 7					8 8		ns
$t_h(H)$ Hold time, HIGH or LOW $t_h(L)$ $\overline{SE}$ to CP	Waveform 2	2 2					2 2		ns
$t_s(H)$ Setup time, HIGH or LOW $t_s(L)$ S/$\overline{P}$ to CP	Waveform 2	12 12					13 13		ns
$t_s(H)$ Setup time, HIGH or LOW $t_s(L)$ S to CP	Waveform 2	8 8					9 9		ns
$t_h(H)$ Hold time, HIGH or LOW $t_h(L)$ S or S/$\overline{P}$ to CP	Waveform 2	0 0					0 0		ns
$t_w(H)$ CP pulse width HIGH	Waveform 1	7					7		ns
$t_w(L)$ $\overline{MR}$ pulse width LOW	Waveform 3	7					7		ns
t_{rec} Recovery time, $\overline{MR}$ to CP	Waveform 3	8					8		ns

5

Preview

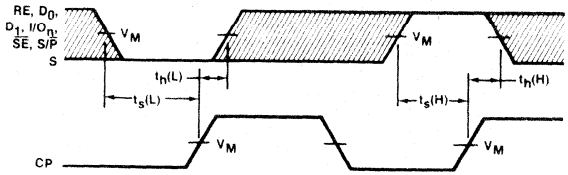
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



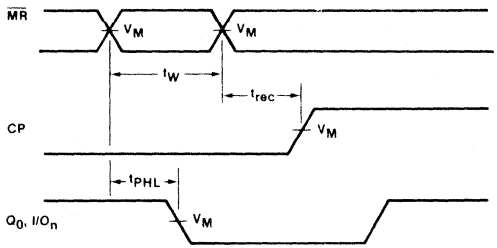
Waveform 1

DATA SETUP AND HOLD TIMES



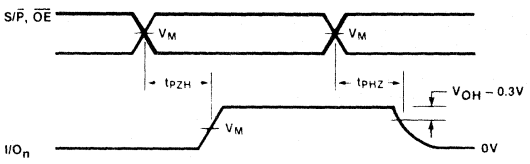
Waveform 2

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



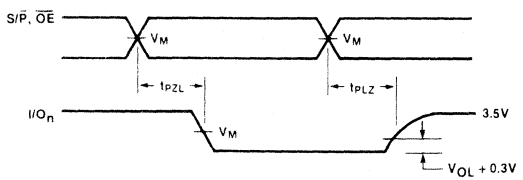
Waveform 3

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 4

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



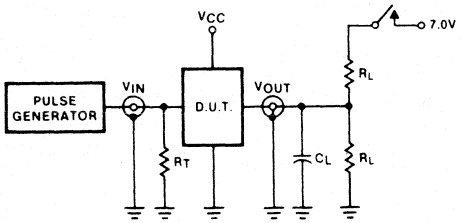
Waveform 5

$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



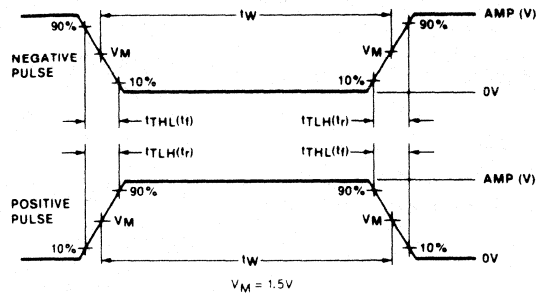
SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

Preview

8-Bit Universal Shift/Storage Register With Synchronous Reset and Common I/O Pins

- **Common parallel I/O for reduced pin count**
- **Additional Serial inputs and outputs for expansion**
- **Four operating modes: Shift Left, Shift Right, Load and Store**
- **3-State outputs for bus-oriented applications**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F323		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F323N	
Plastic SO	N74F323D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

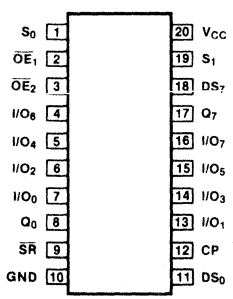
The 'F323 is an 8-bit universal shift/storage register with 3-state outputs. Its function is similar to the 'F299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

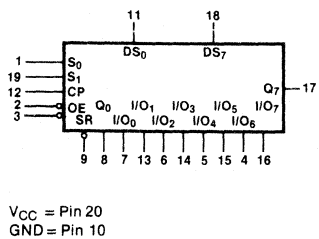
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
DS_0	Serial Data Input for Right Shift	1.0/1.0	20μA/0.6mA
DS_7	Serial Data Input for Left Shift	1.0/1.0	20μA/0.6mA
S_0, S_1	Mode Select Inputs	1.0/2.0	20μA/1.2mA
$\overline{SR}$	Synchronous Reset Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)	1.0/1.0	20μA/0.6mA
I/O_0–I/O_7	Multiplexed Parallel Data Inputs or	1.0/1.0	20μA/0.6mA
	3-State Parallel Data Outputs	150/33	3.0mA/20mA
Q_0, Q_7	Serial Outputs	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION

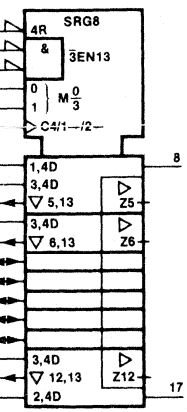


LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)



REGISTER

FAST 54/74F323

Preview

The 'F323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change with the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

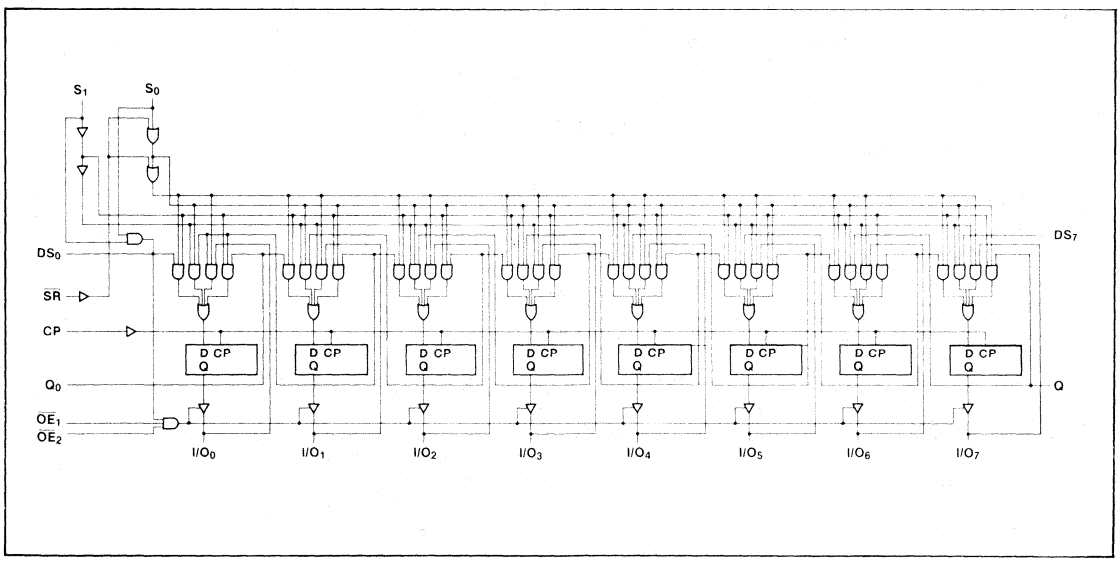
A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

FUNCTION TABLE

INPUTS				RESPONSE
$\overline{SR}$	S_1	S_0	CP	
L	X	X		Synchronous Reset; Q_0-Q_7 = LOW
H	H	H		Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H		Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.)
H	H	L		Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	H	H	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't care

LOGIC DIAGRAM



5

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + 5.5	− 0.5 to + 5.5	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

Preview

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 3	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	– 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F323			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX	I_{OH} = MAX	Mil	2.4			V
				Com'l	2.7			V
			I_{OH} = – 1mA	Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 0.73	– 1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V				2	0	μA
I_{OZL}	Off-state output current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				– 2	– 650	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	S_0, S_1				– 1.2	mA
			Other inputs			– 0.4	– 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 60	– 80	– 150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH				mA
			I_{CCL}	Outputs LOW			92	mA
			I_{CCZ}	Outputs OFF				mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Preview

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum input frequency	Waveform 1	70					70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_0 or Q_7	Waveform 1	4.0 3.5	7.0 6.5	9.0 8.5			4.0 3.5	10 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4.0 5.0	7.0 8.5	9.0 11			4.0 5.0	10 12	ns
t_{PZH} t_{PZL}	Output enable time	Waveform 3 Waveform 4	3.5 4.0	6.0 7.0	8.0 10			3.5 4.0	9.0 11	ns
t_{PHZ} t_{PLZ}	Output disable time	Waveform 3 Waveform 4	2.5 2.0	4.5 4.0	6.0 5.5			2.5 2.0	7.0 6.5	ns

AC SETUP REQUIREMENTS

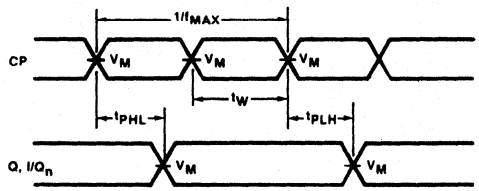
PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW S_0 or S_1 to CP	Waveform 2	8.5 8.5							ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW S_0 or S_1 to CP	Waveform 2	0 0							ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	Waveform 2	5.0 5.0							ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	Waveform 2	2.0 2.0							ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW $\overline{SR}$ to CP	Waveform 2	10 10							ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{SR}$ to CP	Waveform 2	0 0							ns
$t_w(H)$ $t_w(L)$	CP pulse width, HIGH or LOW	Waveform 1	7.0 7.0							ns

5

Preview

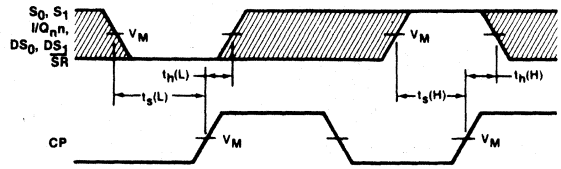
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



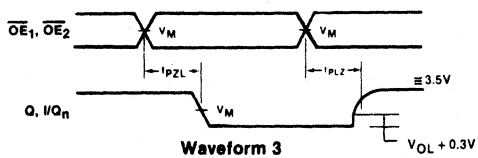
Waveform 1

DATA SETUP AND HOLD TIMES



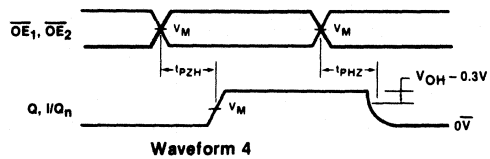
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 4

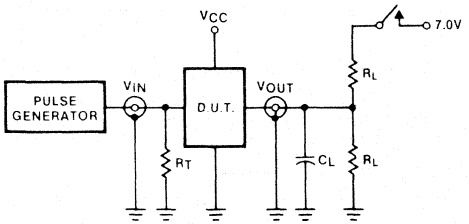
$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

Preview

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



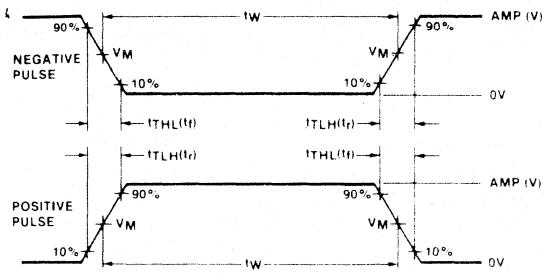
SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

SHIFTER — FAST 54/74F350

4-Bit Shifter (3-State)

- **Shifts 4 bits of data to 0, 1, 2, 3 places under control of two select lines**
- **3-State outputs for bus organized systems**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F350	5.2ns	24mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F350N	
Plastic SO	N74F350D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F350 is a combination logic circuit that shifts a 4-bit word from 0 to 3 places. No clocking is required as with shift registers.

The 'F350 can be used to shift any number of bits any number of places up or down by suitable interconnection. Shifting can be:

1. Logical — with logic zeros filled in at either end of the shifting field.
2. Arithmetic — where the sign bit is extended during a shift down.
3. End around — where the data word forms a continuous loop.

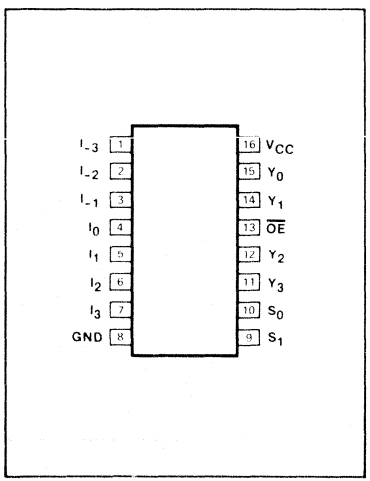
The 3-State outputs are useful for bus interface applications or expansion to a larger number of shift positions in end around shifting. The active LOW Output Enable ($\overline{OE}$) input controls the state of the outputs. The outputs are in the HIGH impedance "off" state when $\overline{OE}$ is HIGH, and they are active when $\overline{OE}$ is LOW.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

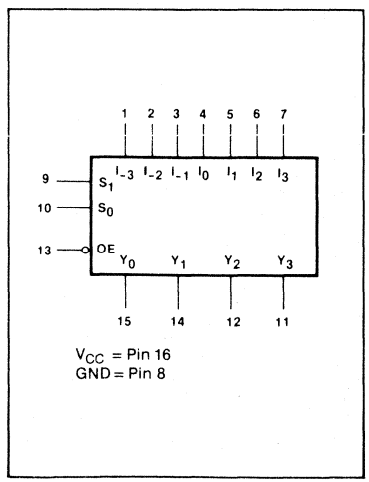
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
S_0, S_1	Select Inputs	1.0/2.0	20μA/1.2mA
I_{-3}-I_3	Data Inputs	1.0/2.0	20μA/1.2mA
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/2.0	20μA/1.2mA
Y_0-Y_3	3-State Outputs	50/33	1.0mA/20mA

Note:
One (1.0) FAST unit load (U.L.) is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

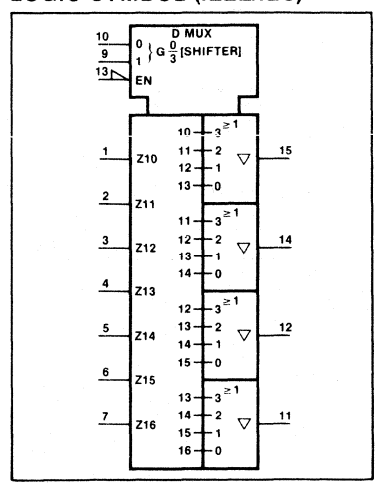
PIN CONFIGURATION



LOGIC SYMBOL

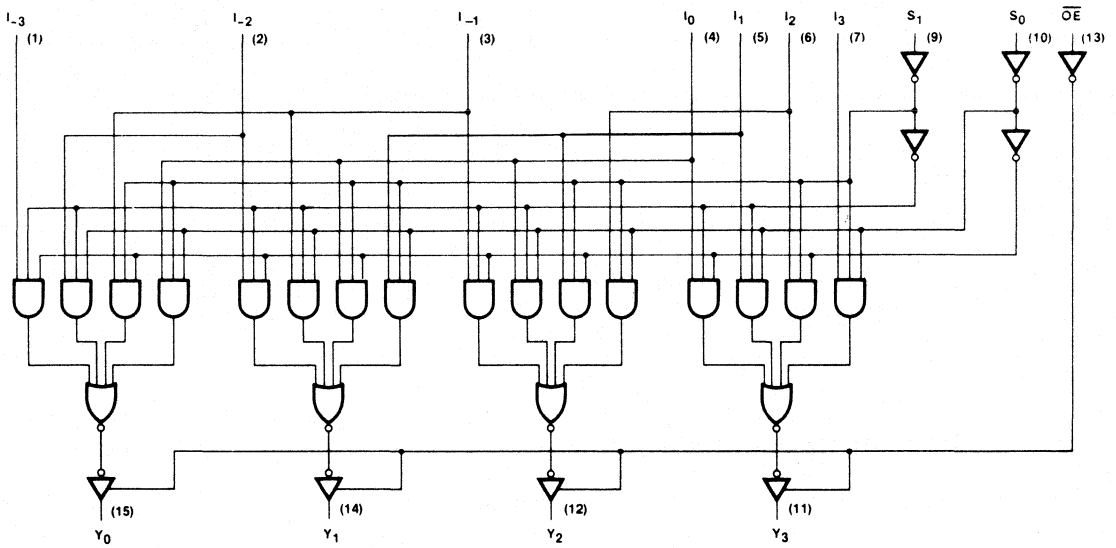


LOGIC SYMBOL (IEEE/IEC)



SHIFTER FAST 54/74F350

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

5

FUNCTION TABLE

OE	S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	D_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	X	D_2	D_1	D_0	D_{-1}	X	X	D_2	D_1	D_0	D_{-1}
L	H	L	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_1	D_0	D_{-1}	D_{-2}
L	H	H	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_0	D_{-1}	D_{-2}	D_{-3}

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state
D_n = HIGH or LOW state of referenced I_n input

LOGIC EQUATIONS

$$Y_0 = \bar{S}_0 \cdot \bar{S}_1 \cdot I_0 + S_0 \cdot \bar{S}_1 \cdot I_{-1} + \bar{S}_0 \cdot S_1 \cdot I_{-2} + S_0 \cdot S_1 \cdot I_{-3}$$
$$Y_1 = \bar{S}_0 \cdot \bar{S}_1 \cdot I_1 + S_0 \cdot \bar{S}_1 \cdot I_0 + \bar{S}_0 \cdot S_1 \cdot I_{-1} + S_0 \cdot S_1 \cdot I_{-2}$$
$$Y_2 = \bar{S}_0 \cdot \bar{S}_1 \cdot I_2 + S_0 \cdot \bar{S}_1 \cdot I_1 + \bar{S}_0 \cdot S_1 \cdot I_0 + S_0 \cdot S_1 \cdot I_{-1}$$
$$Y_3 = \bar{S}_0 \cdot \bar{S}_1 \cdot I_3 + S_0 \cdot \bar{S}_1 \cdot I_2 + \bar{S}_0 \cdot S_1 \cdot I_1 + S_0 \cdot S_1 \cdot I_0$$

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	48	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				-3	mA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	– 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F350			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = MAX	Mil	2.4	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 20mA	Mil		0.35	0.5	V
			I_{OL} = 24mA	Com'l		0.35	0.5	V
V_{IK}	Input clamp voltage (negative)	V_{CC} = MIN, I_I = I_{IK}				– 0.73	– 1.2	V
I_{OZH}	Off-stage output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V				2	50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				– 2	– 50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				– 0.9	– 1.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V			– 60	– 90	– 150	mA
I_{CC}	Supply current	V_{CC} = MAX	I_{CCH}	Outputs HIGH		22	35	mA
			I_{CCL}	Outputs LOW		26	41	mA
			I_{CCZ}	Outputs Disabled		26	42	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

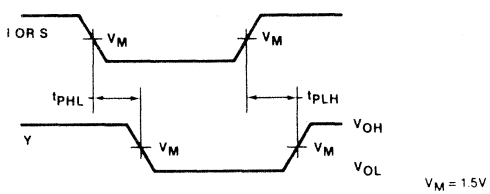
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			54F T_A, V_{CC} = Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} = Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} Data to output	Waveform 1	3.0 2.5	4.5 4.0	6.0 5.5	3.0 2.5	7.5 7.0	3.0 2.5	7.0 6.5	ns
t_{PLH} Propagation delay t_{PHL} Select to output	Waveform 1	4.0 3.0	7.8 6.5	10 8.5	4.0 3.0	13 10	4.0 3.0	11 9.5	ns
t_{PZH} Output enable time t_{PZL}	Waveform 2 Waveform 3	2.5 4.0	5.0 7.0	7.0 9.0	2.5 4.0	8.5 11	2.5 4.0	8.0 10	ns
t_{PHZ} Output disable time t_{PLZ}	Waveform 2 Waveform 3	2.0 2.0	3.9 4.0	5.5 5.5	2.0 2.0	7.0 8.5	2.0 2.0	6.5 6.5	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS

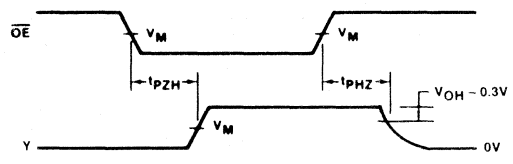
PROPAGATION DELAY DATA AND SELECT TO OUTPUT



$V_M = 1.5V$

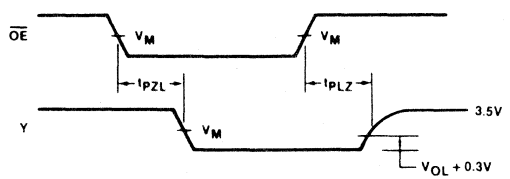
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL

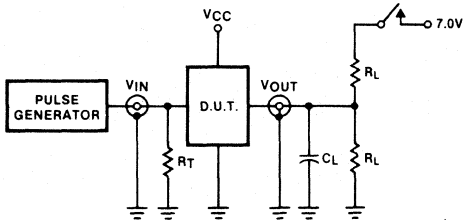


Waveform 3

5

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

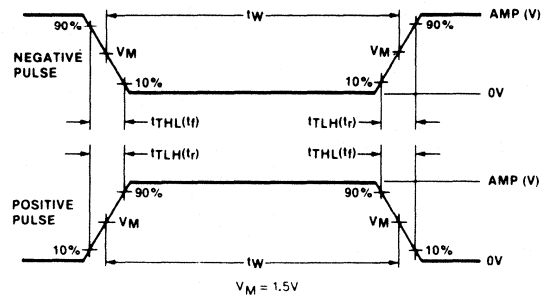
DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



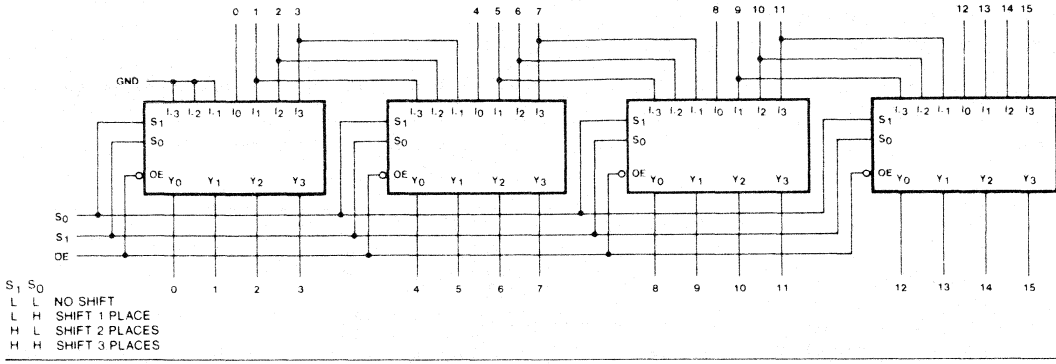
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

SHIFTER

FAST 54/74F350

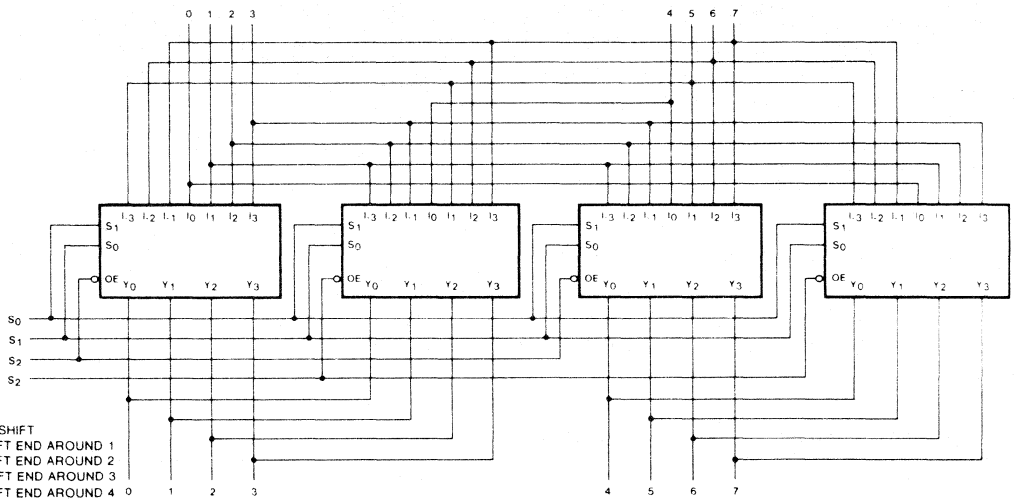
APPLICATIONS

16-BIT SHIFT-UP 0, 1, 2, OR 3 PLACES



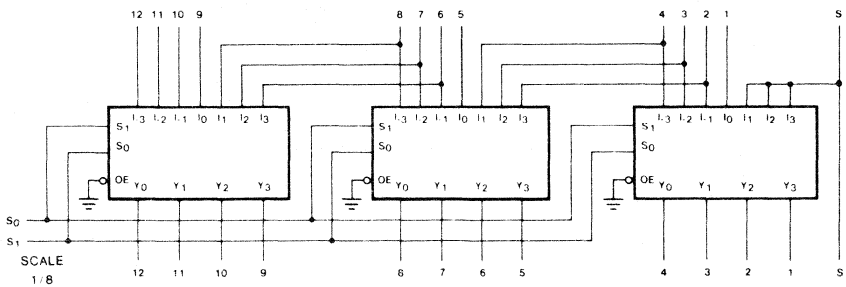
S_1	S_0	
L	L	NO SHIFT
L	H	SHIFT 1 PLACE
H	L	SHIFT 2 PLACES
H	H	SHIFT 3 PLACES

8-BIT END AROUND SHIFT 0, 1, 2, 3, 4, 5, 6, 7 PLACES



S_2	S_1	S_0	
L	L	L	NO SHIFT
L	L	H	SHIFT END AROUND 1
L	H	L	SHIFT END AROUND 2
L	H	H	SHIFT END AROUND 3
H	L	L	SHIFT END AROUND 4
H	L	H	SHIFT END AROUND 5
H	H	L	SHIFT END AROUND 6
H	H	H	SHIFT END AROUND 7

13-BIT 2's COMPLEMENT SCALER



S_1	S_0		SCALE
L	L	÷8	1/8
L	H	÷4	1/4
H	L	÷2	1/2
H	H	NO CHANGE	1

5

MULTIPLEXER — FAST 54/74F352

Preview

Dual 4-Line To 1-Line Multiplexer

- **Inverting version of 'F153**
- **Separate Enable for each multiplexer section**
- **Common Select inputs**
- **See 'F353 for 3-State version**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F352		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F352N	
Plastic SO	N74F352D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
I_{0a}–I_{3a}	Side A Data Inputs	1.0/1.0	20μA/0.6mA
I_{0b}–I_{3b}	Side B Data Inputs	1.0/1.0	20μA/0.6mA
S_0, S_1	Common Select Inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_a$, $\overline{E}_b$	Side A, B Enable Inputs (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{Y}_a$, $\overline{Y}_b$	Multiplexer Outputs (Inverted)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

DESCRIPTION

The 'F352 has a dual 4-input multiplexer that can select 2 bits of data from up to eight sources under control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. Outputs ($\overline{Y}_a$, $\overline{Y}_b$) are forced HIGH when the corresponding Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH.

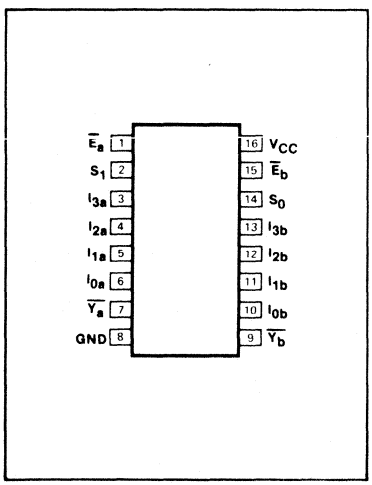
The device is the logical implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$\overline{Y}_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

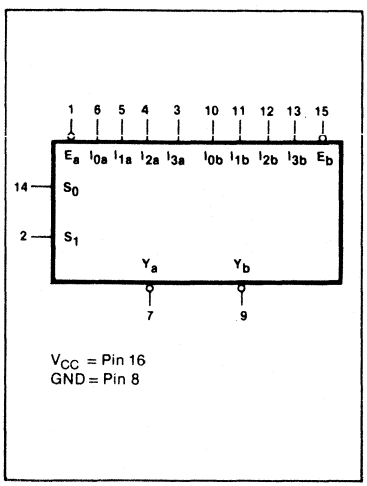
$$\overline{Y}_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The 'F352 can be used to move data to a common output bus from a group of registers. The state of the Select inputs would determine the particular register from which the data came. An alternative application is as a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

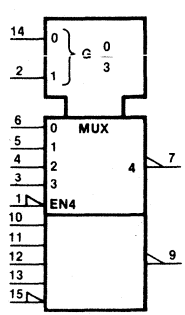
PIN CONFIGURATION



LOGIC SYMBOL



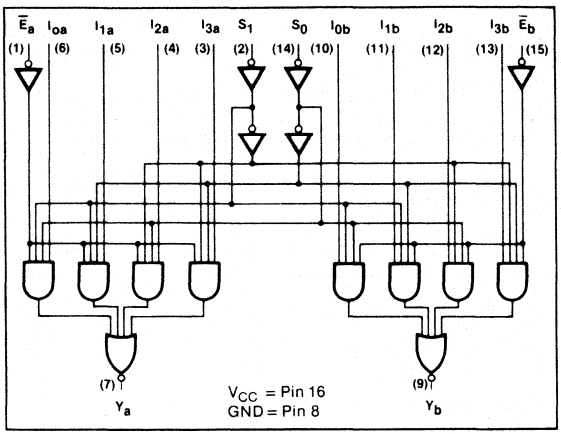
LOGIC SYMBOL (IEEE/IEC)



MULTIPLEXER FAST 54/74F352

Preview

LOGIC DIAGRAM



FUNCTION TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Y
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

5

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				+ 0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		+ 125	°C
		Com'l	0		70	°C

MULTIPLEXER FAST 54/74F352

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F352 Min	54/74F352 Typ[2]	54/74F352 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			– 0.73	– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			– 0.4	– 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		– 60	– 85	– 150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} V_{IN} = GND			14	mA
			I_{CCL} V_{IN} = HIGH			20	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

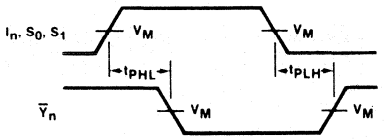
PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveforms 1 and 2	4.0 4.0		13 13	3.5 3.5	14.5 15	4.0 4.0	14 14	ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 2	5.0 4.0		14 11	4.5 4.0	17 13	5.0 4.0	15 12	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1	2.0 2.0		7.0 6.0	2.0 2.0	9.0 7.5	2.0 2.0	8.0 7.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

Preview

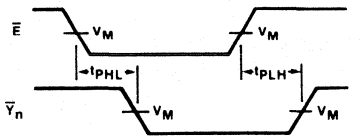
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS

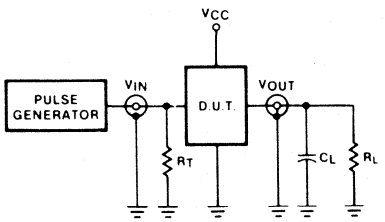


Waveform 2

$V_M = 1.5V$

TEST CIRCUITS AND WAVEFORMS

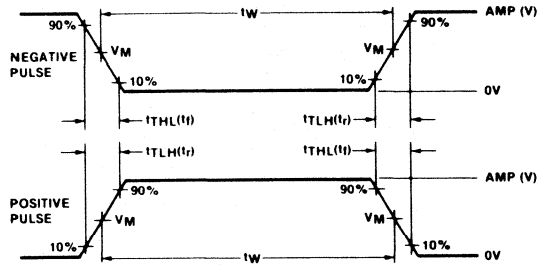
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

MULTIPLEXER — FAST 54/74F353

Preview

Dual 4-Input Multiplexer (3-State)

- **Inverting version of 'F253**
- **3-State outputs for bus interface and multiplex expansion**
- **Common Select inputs**
- **Separate Output Enable inputs**

TYPE	TYPICAL PROPAGATION DELAY (From Data)	TYPICAL SUPPLY CURRENT (Total)
74F353	12ns	8mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F353N	
Plastic SO	N74F353D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F353 has two identical 4-input multiplexers with 3-State outputs which select two bits from eight sources selected by common Select inputs (S_0, S_1). When the individual Output Enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs of the 4-input multiplexers are HIGH, the outputs are forced to a HIGH impedance (HIGH Z) state.

The 'F353 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two Select inputs. Logic equations for the outputs are shown below:

$$\overline{Y}_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$\overline{Y}_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

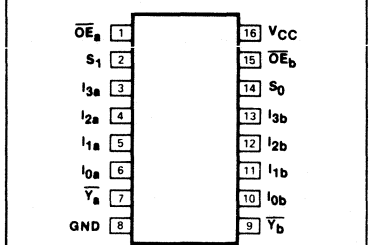
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
I_{0a}–I_{3a}	Side A Data Inputs	1.0/1.0	20μA/0.6mA
I_{0b}–I_{1b}	Side B Data Inputs	1.0/1.0	20μA/0.6mA
S_0, S_1	Common Select Inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}_a$, $\overline{OE}_b$	Side A, B Output Enable Inputs (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{Y}_a$, $\overline{Y}_b$	3-State Outputs (Inverted)	150/33	3.0mA/20mA

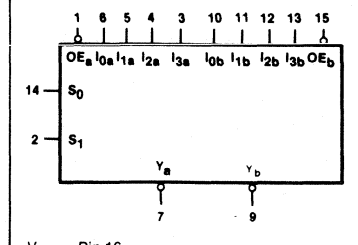
NOTE:
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

All but one device must be in the HIGH impedance state to avoid high currents exceeding the maximum ratings, if the outputs of the 3-State devices are tied together. Design of the Output Enable signals must ensure that there is no overlap.

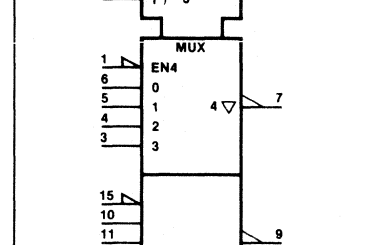
PIN CONFIGURATION



LOGIC SYMBOL



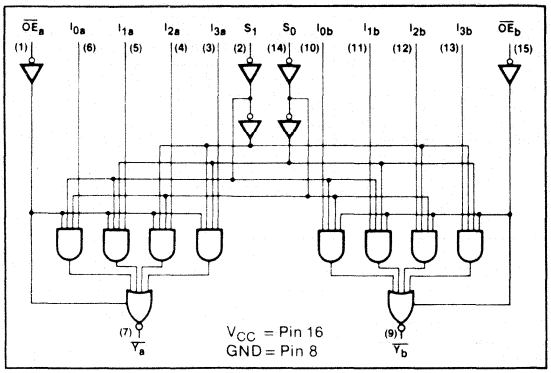
LOGIC SYMBOL (IEEE/IEC)



MULTIPLEXER FAST 54/74F353

Preview

LOGIC DIAGRAM



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Y
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + 5.5	− 0.5 to + 5.5	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

5

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 3	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

MULTIPLEXER FAST 54/74F353

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F353 Min	54/74F353 Typ[2]	54/74F353 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.4	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			− 0.73	− 1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V			2	50	μA
I_{OZL}	Off-state output current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			− 2	− 50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			− 0.4	− 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		− 60	− 90	− 150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} I_n, S_n, $\overline{OE}_n$ = GND			14	mA
			I_{CCL} I_n, S_n = GND			20	mA
			I_{CCZ} OE_a = 4.5V			23	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

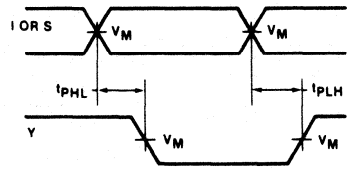
PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1	3.0 2.0		7.0 6.0	3.0 2.0	9.0 7.5	3.0 2.0	8.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1	5.0 4.0		14 11	5.0 4.0	16 14	5.0 4.0	15 12	ns
t_{PZH}	Output enable to HIGH level	Waveform 2	3.0		9.0	3.0	11	3.0	10	ns
t_{PZL}	Output enable to LOW level	Waveform 3	3.0		9.5	3.0	12	3.0	10.5	ns
t_{PHZ}	Output disable from HIGH level	Waveform 2	2.0		5.0	2.0	6.5	2.0	6.0	ns
t_{PLZ}	Output disable from LOW level	Waveform 3	2.0		6.0	2.0	8.5	2.0	7.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

Preview

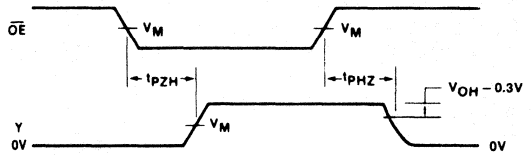
AC WAVEFORMS

PROPAGATION DELAY DATA OR SELECT TO OUTPUT



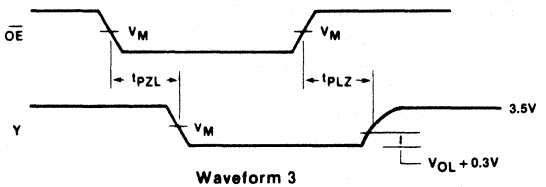
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL

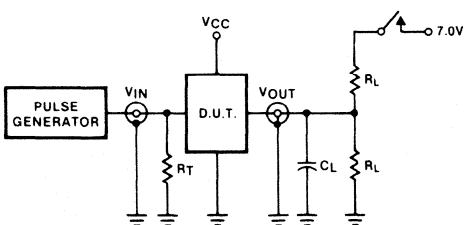


Waveform 3

5

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



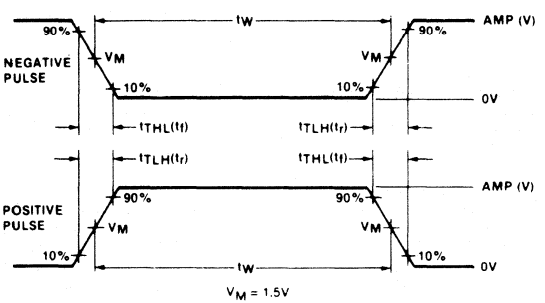
SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Preliminary

'F365, 'F367 Hex Buffer/Driver (3-State)
'F366, 'F368 Hex Inverter Buffer (3-State)

- **High impedance NPN base inputs for reduced loading (40μA in LOW and HIGH states)**
- **3-State buffer outputs sink 64mA**
- **High speed**
- **Bus oriented**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F365	ns	mA
74F366	ns	mA
74F367	ns	mA
74F368	ns	mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F365N • N74F366N N74F367N • N74F368N	
Plastic SO	N74F365D • N74F366D N74F367D • N74F368D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

FUNCTION TABLE, 'F365, 'F366

INPUTS			OUTPUTS	
$\overline{OE}_1$	$\overline{OE}_2$	I	Y	$\overline{Y}$
L	L	L	L	H
L	L	H	H	L
X	H	X	(Z)	(Z)
H	X	X	(Z)	(Z)

FUNCTION TABLE, 'F367, 'F368

INPUTS		OUTPUTS	
$\overline{OE}$	I	Y	$\overline{Y}$
L	L	L	H
L	H	H	L
H	X	(Z)	(Z)

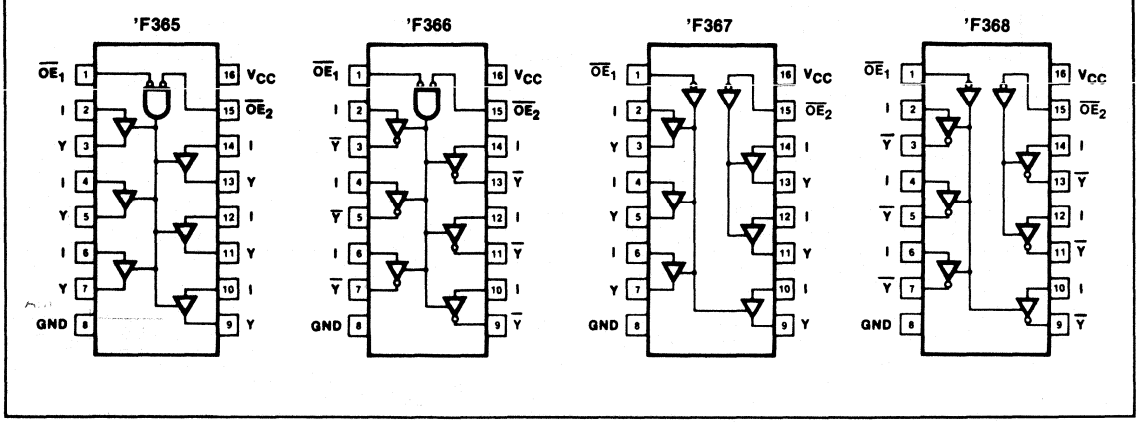
L = LOW voltage level
H = HIGH voltage level
X = Don't care
(Z) = HIGH impedance (off) state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Input (Active LOW)	2.0/0.066	40μA/40μA
I	Inputs	2.0/0.066	40μA/40μA
Y, $\overline{Y}$	Outputs	150/106.6	3mA/64mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

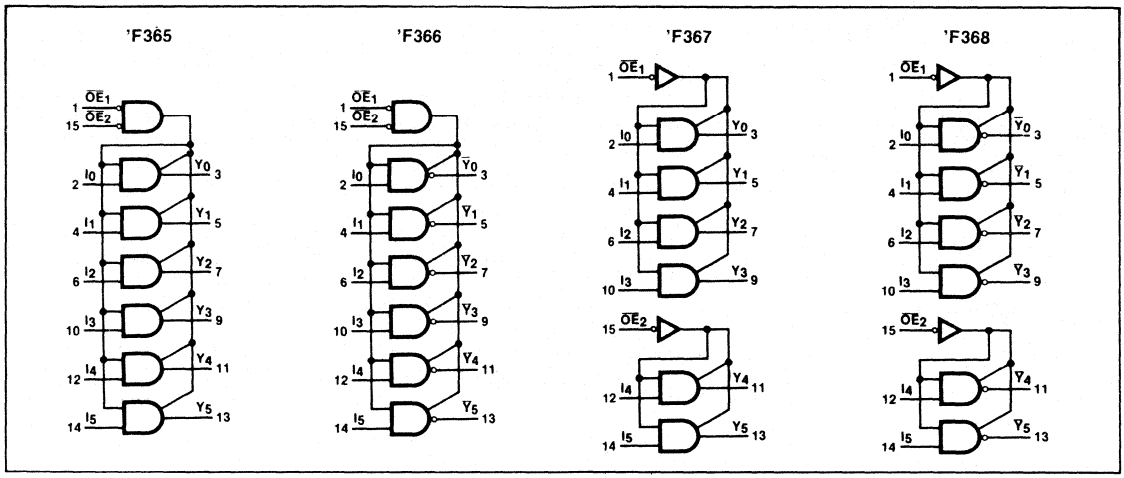
PIN CONFIGURATION



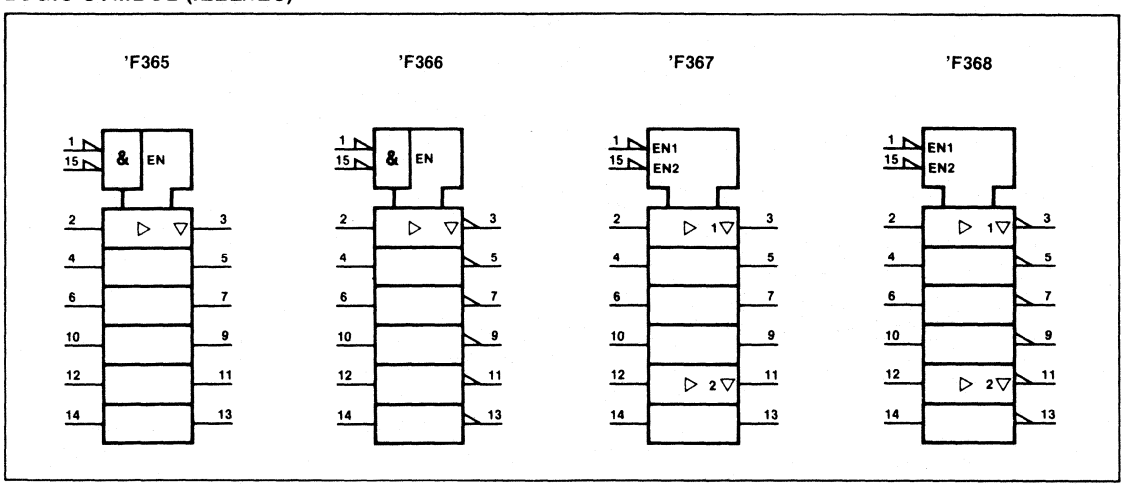
BUFFERS/DRIVERS FAST 54/74F365, F366, F367, F368

Preliminary

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



5

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	96	128	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

Preliminary

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	HIGH-level output current	Mil			-12	mA
		Com'l			-15	mA
I_{OL}	LOW-level output current	Mil			48	mA
		Com'l			64	mA
T_A	Operating free-air temperature	Mil	-55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F365, F366, F367, F368			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = 0.5V	I_{OH} = -12mA	Mil	2.0			V
			I_{OH} = -15mA	Com'l	2.0			V
		V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = -3mA	Mil	2.4	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 48mA	Mil		0.35	0.5	V
			I_{OL} = 64mA	Com'l		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					2	mA
I_{IH}	HIGH-level input current	V_I = 2.7V, V_{CC} = MAX				1	40	µA
I_{IL}	LOW-level input current	V_I = 0.5V, V_{CC} = MAX					- 40	µA
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{OUT} = 2.4V				2	50	µA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{OUT} = 0.5V				- 2	- 50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-100	-150	-225	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	'F365, 'F367	I_{CCH}		35	50	mA
				I_{CCL}		65	90	mA
				I_{CCZ}		65	90	mA
			'F366, 'F368	I_{CCH}		35	50	mA
				I_{CCL}		65	90	mA
				I_{CCZ}		65	90	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Preliminary

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

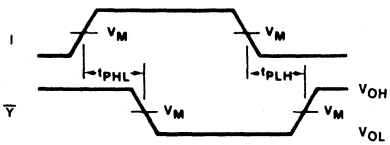
PARAMETER		TEST CONDITIONS		54F/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			54F T_A, V_{CC} = Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} = Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1, 'F366, 'F368		3.0 2.0		7.0 7.0			2.0 1.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2, 'F365, 'F367		3.0 2.0		7.0 7.0			2.0 1.0	8.0 8.0	ns
t_{PZH}	Enable to HIGH	Waveform 3		9.0		14.0			8.0	12.0	ns
t_{PZL}	Enable to LOW	Waveform 4	'F365, 'F367	7.0		11.0			6.0	12.0	ns
			'F366, 'F368	7.0		11.0			6.0	12.0	
t_{PHZ}	Disable from HIGH	Waveform 3	'F365, 'F367	4.0		9.0			3.0	10.0	ns
			'F366, 'F368	4.0		9.0			3.0	10.0	
t_{PLZ}	Disable from LOW	Waveform 4		12.0		17.0			11.0	12.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

5

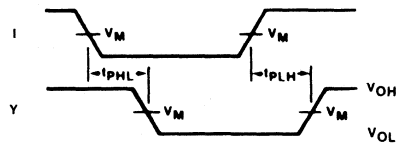
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



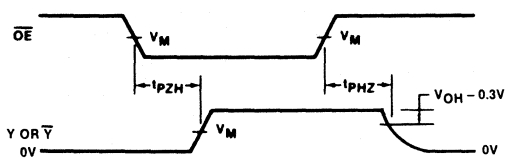
Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



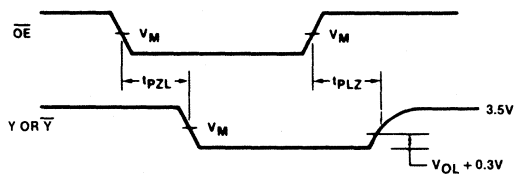
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



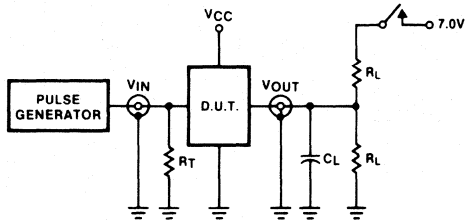
Waveform 4

$V_M = 1.5V$

Preliminary

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

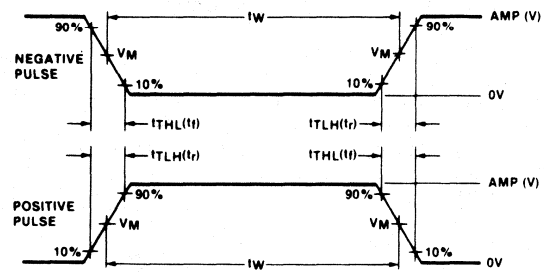
DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

'F373 Octal Transparent Latch (3-State)
'F374 Octal D Flip-Flop (3-State)

- **8-bit transparent latch — 'F373**
- **8-bit positive, edge-triggered register — 'F374**
- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F373	4.5ns	35mA
74F374	6.5ns	55mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F373N • N74F374N	
Plastic SO	N74F373D • N74F374D	
Ceramic DIP		S54F373F • S54F374F
Ceramic LLCC		S54F373G • S54F374G

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data that is present one set-up time before the HIGH-to-LOW enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

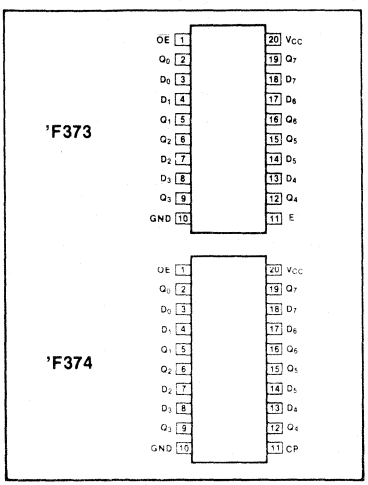
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
D_0-D_7 ('F373 & 'F374)	Data Inputs	1.0/1.0	20μA/0.6mA
E ('F373)	Latch Enable Input (Active HIGH)	1.0/1.0	20μA/0.6mA
$\overline{OE}$ ('F373 & 'F374)	Output Enable Input (Active LOW)	1.0/1.0	20μA/0.6mA
CP ('F374)	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
O_0-O_7 ('F373 & 'F374)	3-State Outputs	150/33	3mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

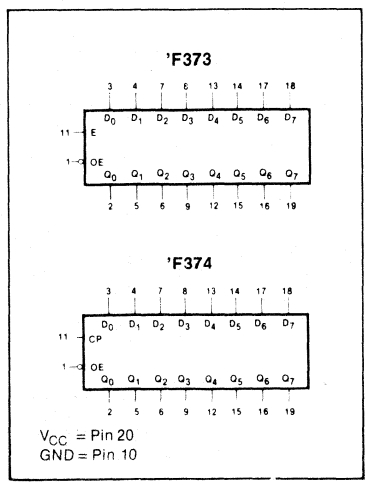
The 'F374 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

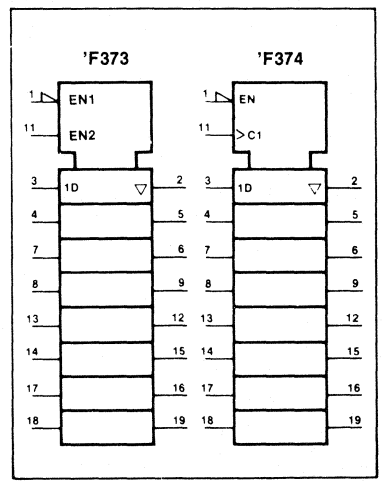
PIN CONFIGURATION



LOGIC SYMBOL



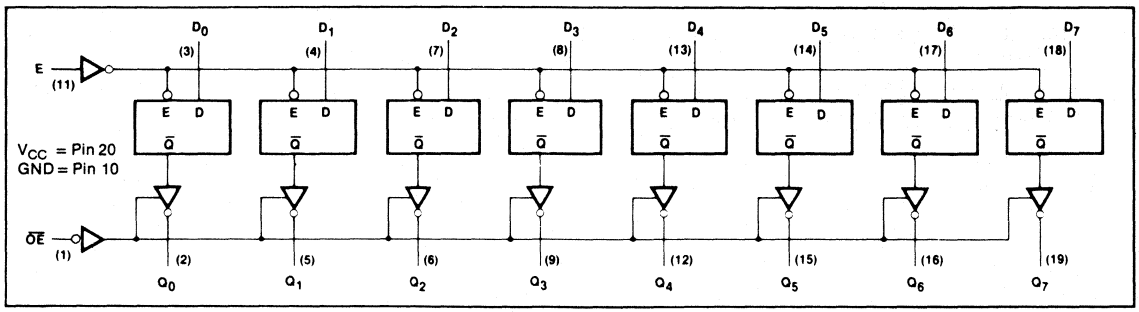
LOGIC SYMBOL (IEEE/IEC)



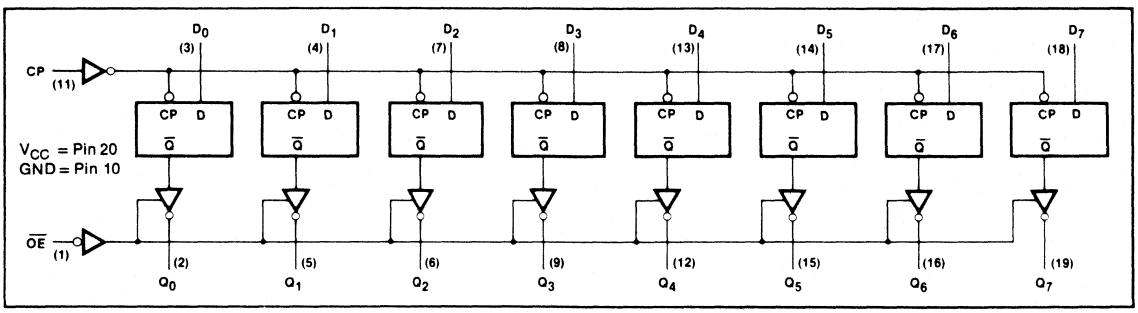
5

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 'F373



LOGIC DIAGRAM, 'F374



MODE SELECT — FUNCTION TABLE, 'F373

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		Q_0-Q_7
Enable and read register	L	H	X	L	L
	L	H	X	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	X	X	X	(Z)
	H	X	X	X	(Z)

MODE SELECT — FUNCTION TABLE, 'F374

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0-Q_7
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	X	X	X	(Z)
	H	X	X	X	(Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW $\overline{OE}$ transition
L = LOW voltage level
X = Don't care
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW $\overline{OE}$ transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	48	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				-3	mA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

5

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F373, 374			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 20mA	Mil		0.35	0.5	V
			I_{OL} = 24mA	Com'l		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V					50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V			−60		−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCZ} $\overline{OE}$ = 4.5V, D inputs, E = GND	'F373		35	55	mA
			I_{CCZ} CP, $\overline{OE}$ = 4.5V, D inputs = GND	'F374		57	86	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			54F T_A, V_{CC} = Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} = Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 6, 'F374	100			60		70		MHz
t_{PLH} t_{PHL}	Propagation delay Latch Enable to output	Waveform 1, 'F373	3.0 2.0	9.0 4.0	11.5 7.0	3.0 2.0	17.0 8.5	5.0 3.0	13.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4, 'F373	3.0 2.0	5.3 3.7	7.0 5.0	3.0 1.7	8.5 6.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 6, 'F374	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.5 13.0	4.0 4.0	10.0 10.0	ns
t_{PZH}	Enable time to HIGH level	Waveform 2 'F373 'F374	2.0 2.0	5.0 9.0	11.0 11.5	2.0 2.0	13.5 14.0	2.0 2.0	12.0 12.5	ns
t_{PZL}	Enable time to LOW level	Waveform 3 'F373 'F374	2.0 2.0	5.6 5.3	7.5 7.5	2.0 2.0	10.5 10.0	2.0 2.0	8.5 8.5	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2 'F373 'F374	2.0 2.0	4.5 5.3	6.5 7.0	2.0 2.0	10.0 8.0	2.0 2.0	7.5 8.0	ns
t_{PLZ}	Disable time from LOW level	Waveform 3 'F373 'F374	2.0 2.0	3.8 4.3	5.0 5.5	2.0 2.0	7.0 7.5	2.0 2.0	6.0 6.5	ns

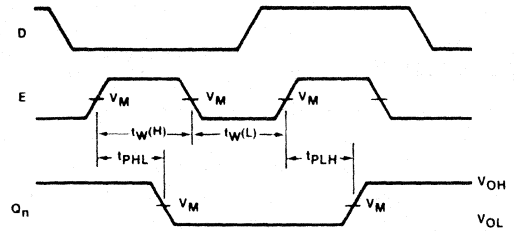
AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			54F T_A, V_{CC} = Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} = Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_W (H) t_W (L)	Latch Enable pulse width	Waveform 1, 'F373	6.0 6.0			6.0 6.0		6.0 6.0		ns
t_s (H) t_s (L)	Setup time, Data to Latch Enable	Waveform 5, 'F373	2.0 2.0			2.0 2.0		2.0 2.0		ns
t_h (H) t_h (L)	Hold time, Data to Latch Enable	Waveform 5, 'F373	3.0 3.0			3.0 3.0		3.0 3.0		ns
t_w (H) t_w (L)	Clock Pulse width	Waveform 6, 'F374	7.0 6.0			7.0 6.0		7.0 6.0		ns
t_s (H) t_s (L)	Setup time, Data to Clock	Waveform 7, 'F374	2.0 2.0			2.5 2.0		2.0 2.0		ns
t_h (H) t_h (L)	Hold time, Data to Clock	Waveform 7, 'F374	2.0 2.0			2.0 2.5		2.0 2.0		ns

NOTE
Subtract 0.2ns from minumum values for SO package.

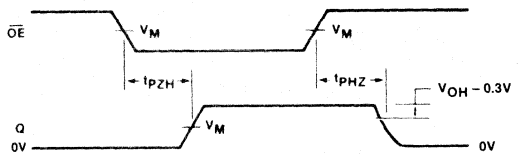
AC WAVEFORMS

LATCH ENABLE TO OUTPUT DELAYS
AND LATCH ENABLE PULSE WIDTH



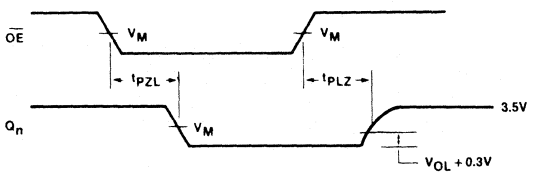
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL
AND DISABLE TIME FROM HIGH LEVEL



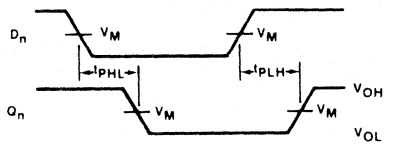
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL
AND DISABLE TIME FROM LOW LEVEL



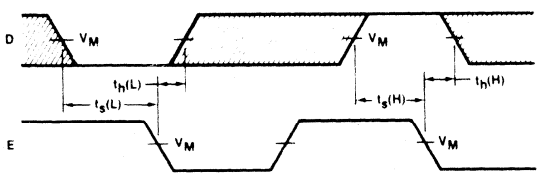
Waveform 3

PROPAGATION DELAY DATA
TO Q OUTPUTS



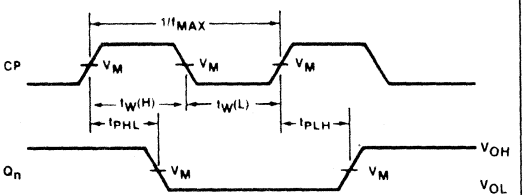
Waveform 4

DATA SETUP AND HOLD TIMES



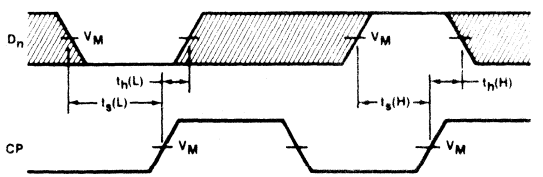
Waveform 5

CLOCK TO OUTPUT DELAYS
AND CLOCK PULSE WIDTH



Waveform 6

DATA SETUP AND HOLD TIMES



Waveform 7

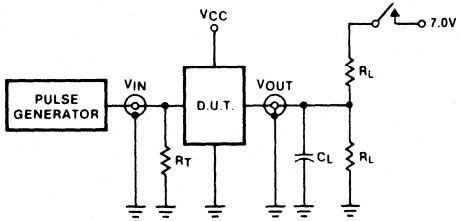
V_M = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.

5

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

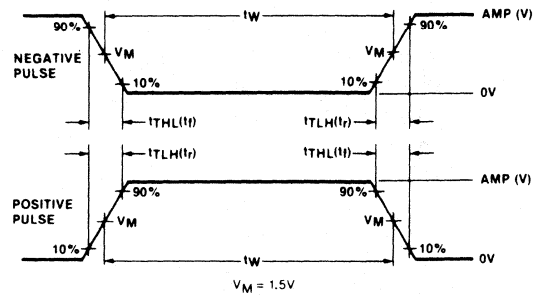
DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Preliminary

Octal D Flip-Flop With Clock Enable

- High impedance NPN Base Inputs for reduced loading (20μA in HIGH and LOW states)
- Ideal for addressable register applications
- Clock Enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- See 'F273 for Master Reset version
- See 'F373 for transparent latch version
- See 'F374 for 3-state version

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F377	100MHz	45mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F377N	
Plastic SO	N74F377D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
D_0-D_7	Data Inputs	1.0/0.033	20μA/20μA
$\overline{CE}$	Clock Enable Input (Active LOW)	1.0/0.033	20μA/20μA
CP	Clock Pulse Input (Active Rising Edge)	1.0/0.033	20μA/20μA
Q_0-Q_7	Data Outputs	50/33	1mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

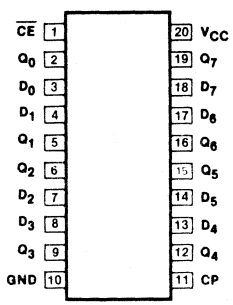
5

DESCRIPTION

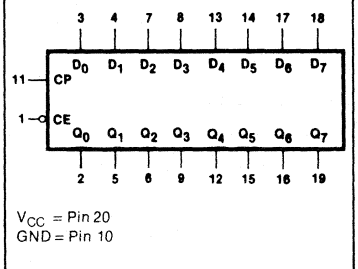
The 'F377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

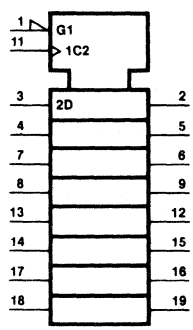
PIN CONFIGURATION



LOGIC SYMBOL



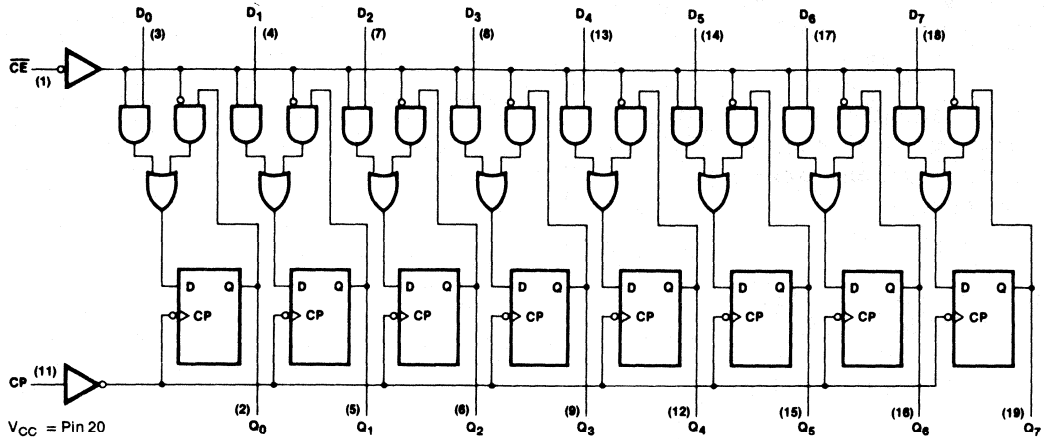
LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOP FAST 54/74F377

Preliminary

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{CE}$	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑	h	X	no change
	X	H	X	no change

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
i_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state with V_{CC} = OV	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

FLIP-FLOP — FAST 54/74F377

Preliminary

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F Min	54/74F Nom	54/74F Max	UNIT
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	– 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F377 Min	54/74F377 Typ[2]	54/74F377 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = MAX, V_{IL} = MAX	Mil	2.5	3.5		V
			Com'l	2.7	3.5		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			– 0.73	– 1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				1.0	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				– 20	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		– 60		– 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		40	50	mA
			I_{CCL} Outputs LOW		50	60	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With all outputs open.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100			70		80		MHz
t_{PLH}	Clock to output	Waveform 1		7.0		4.5		4.5	11	ns
t_{PHL}	Clock to output	Waveform 1		8.0		6.5		5.5	12	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

5

FLIP-FLOP

FAST 54/74F377

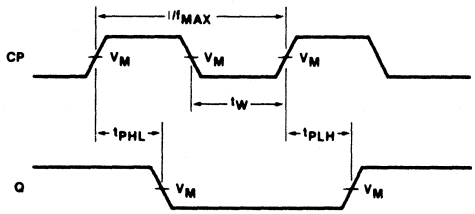
Preliminary

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_w(L)$	Clock pulse width (LOW)	Waveform 1	4	4				4		ns
t_s	Setup time, Data to CP	Waveform 2	3	3				3		ns
t_h	Hold time, Data to CP	Waveform 2	1	1				1		ns
t_s	Setup time, $\overline{CE}$ to CP	Waveform 2	3	3				3		ns
t_h	Hold time, $\overline{CE}$ to CP	Waveform 2	1	1				1		ns

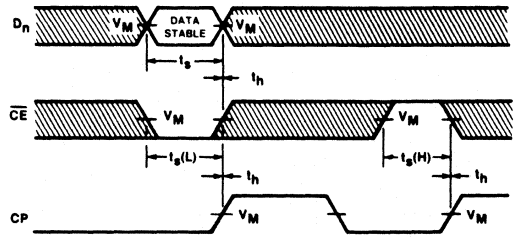
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

DATA AND CLOCK ENABLE SETUP AND HOLD TIMES



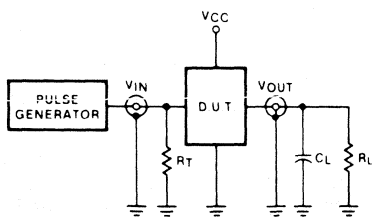
Waveform 2

$V_M = 1.5V$

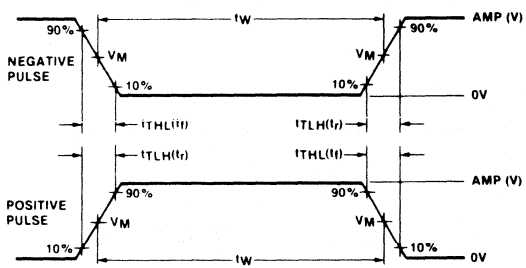
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



$V_M = 1.5V$

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FLIP-FLOP

FAST 54/74F378

Preview

Hex D Flip-Flop With Clock Enable

- 6-bit high-speed parallel register
- Positive edge-triggered D-type inputs
- Fully buffered common Clock and Enable inputs
- Input clamp diodes limit high-speed termination effects
- Fully TTL and CMOS compatible
- Ideal for addressable register applications
- Clock Enable for address and data synchronization applications

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F378	100MHz	

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F378N	
Plastic SO	N74F378D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F378 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is low.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input is also edge-triggered and must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

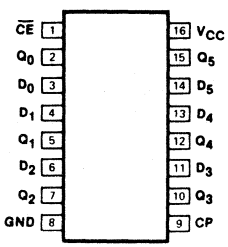
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{CE}$	Enable Input (Active LOW)	1.0/1.0	20μA/0.6mA
D_0-D_5	Data Inputs	1.0/1.0	20μA/0.6mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
Q_0-Q_5	Outputs	50/33	1.0mA/20mA

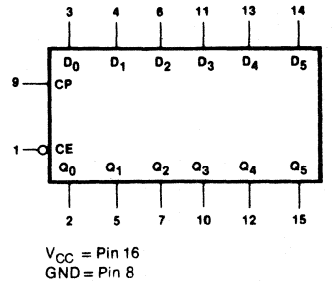
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

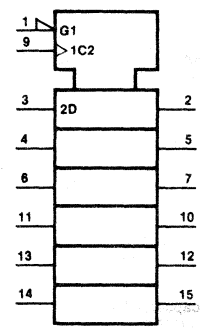
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

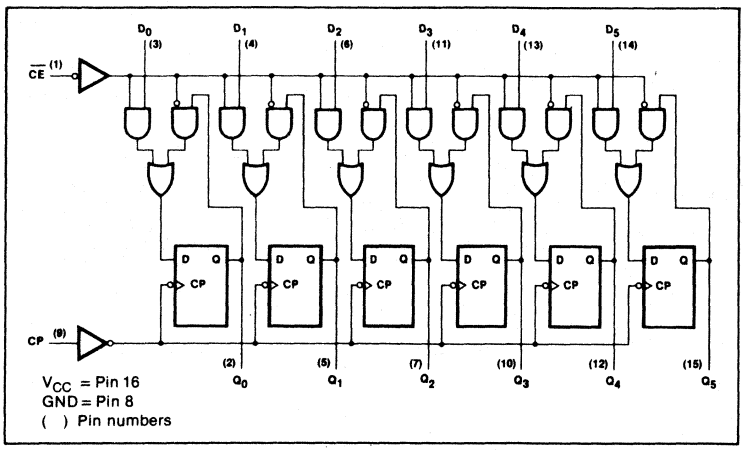


FLIP-FLOP

FAST 54/74F378

Preview

LOGIC DIAGRAM



MODE SELECT— FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{CE}$	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑	h	X	no change
	X	H	X	no change

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

FLIP-FLOP — FAST 54/74F378

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F378 Min	54/74F378 Typ[2]	54/74F378 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			– 0.73	– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			– 0.4	– 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		– 60	– 80	– 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH				mA
			I_{CCL} Outputs LOW			45	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at at time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techinques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With ground applied to all data inputs and the Clock Enable input and all outputs open, I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100						MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1	3.0 3.5	5.5 6.0	7.5 8.5			3.0 3.5	8.5 9.5	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to CP	Waveform 2	4.0 4.0					4.0 4.0		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to CP	Waveform 2	2.0 2.0					2.0 2.0		ns
t_s (H) t_s (L)	Setup Time, HIGH or LOW $\overline{CE}$ to CP	Waveform 2	4.0 10.0					4.0 10.0		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{CE}$ to CP	Waveform 2	0 0					0 0		ns
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	Waveform 1	4.0 6.0					4.0 6.0		ns

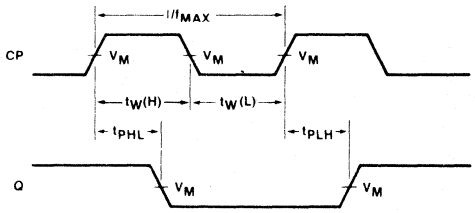
5

FLIP-FLOP FAST 54/74F378

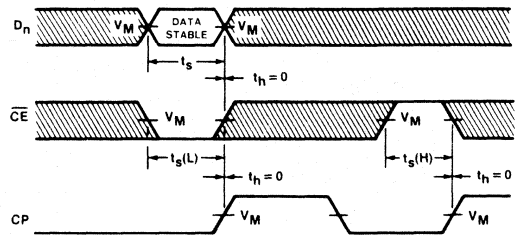
Preview

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



DATA AND CLOCK ENABLE SETUP AND HOLD TIMES



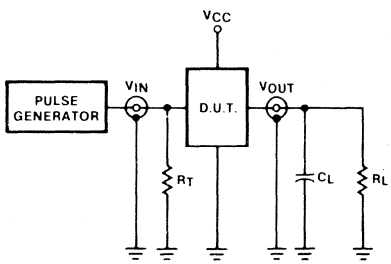
$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 1 **Waveform 2**

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



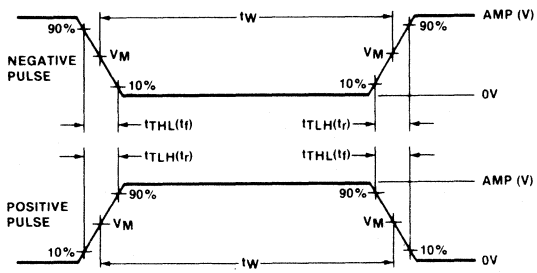
DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

QUAD REGISTER — FAST 54/74F379

Preview

Quad Parallel Register (with Enable)

- Edge-triggered D-type inputs
- Buffered positive edge-triggered Clock
- Buffered common Enable input
- True and Complement outputs

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F379		28mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F379N	
Plastic SO	N74F379D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F379 is a 4-bit register with buffered common Enable. This device is similar to the 'F175 but features the common Enable rather than common Master Reset.

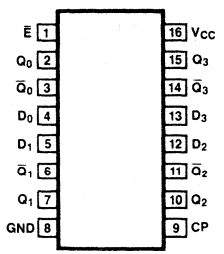
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{E}$	Enable Input (Active LOW)	1.0/1.0	20μA/0.6mA
D_0-D_3	Data Inputs	1.0/1.0	20μA/0.6mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
Q_0-Q_3	Flip-Flop Outputs	50/33	1.0mA/20mA
$\overline{Q}_0$-$\overline{Q}_3$	Complement Outputs	50/33	1.0mA/20mA

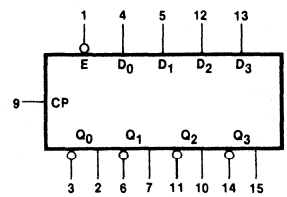
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

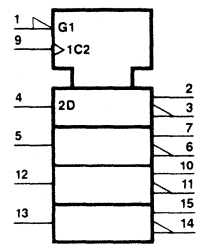
PIN CONFIGURATION



LOGIC SYMBOL



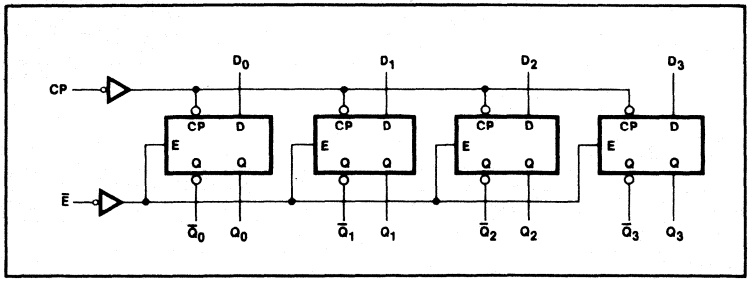
LOGIC SYMBOL (IEEE/IEC)



QUAD REGISTER — FAST 54/74F379

Preview

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{E}$	CP	D_n	$\overline{Q}_n$	Q_n
H	↑	X	NC	NC
L	↑	H	H	L
L	↑	L	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
NC = No change
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

QUAD REGISTER FAST 54/74F379

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F379 Min	54/74F379 Typ[2]	54/74F379 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			− 0.73	− 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			− 0.4	− 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		− 60	− 80	− 150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX; D, E = GND; CP = ↑				40	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	140				100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveform 1	4.0 5.0	5.0 6.5	6.5 8.5			4.0 5.0	7.5 9.5	ns

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_s (H) t_s (L)	Setup time, HIGH or LOW D_n to CP	Waveform 2	3.0 3.0					3.0 3.0		ns
t_h (H) t_h (L)	Hold time, HIGH or LOW D_n to CP	Waveform 2	1.0 1.0					1.0 1.0		ns
t_s (H) t_s (L)	Setup time, HIGH or LOW $\overline{E}$ to CP	Waveform 2	6.0 6.0					6.0 6.0		ns
t_h (H) t_h (L)	Hold time, HIGH or LOW $\overline{E}$ to CP	Waveform 2	0 0					0 0		ns
t_w (H) t_w (L)	CP pulse width, HIGH or LOW	Waveform 1	4.0 5.0					4.0 5.0		ns

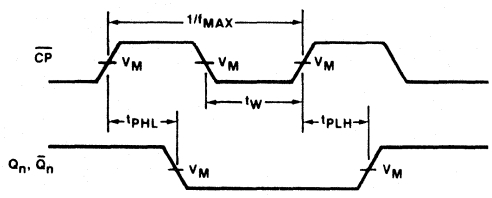
5

QUAD REGISTER — FAST 54/74F379

Preview

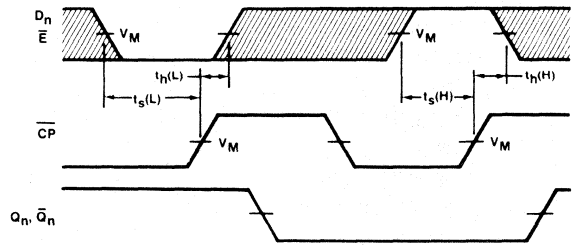
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

DATA SETUP AND HOLD TIMES



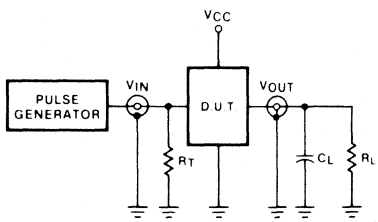
Waveform 2

$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

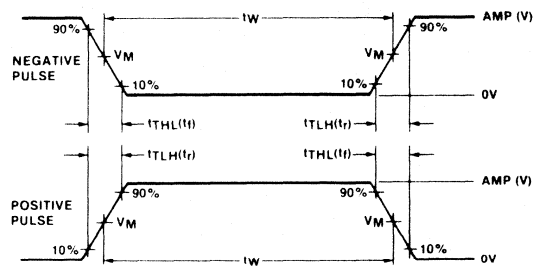
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

ARITHMETIC LOGIC UNIT (ALU) FAST 54/74F381

Preview

4-Bit Arithmetic Logic Unit

- **Low input loading minimizes drive requirements**
- **Performs six arithmetic and logic functions**
- **Selectable LOW (clear) and HIGH (preset) functions**
- **Carry Generate and Propagate outputs for use with carry lookahead generator**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F381		59mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F381N	
Plastic SO	N74F381D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F381 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select input codes force the Function outputs LOW or HIGH. Carry Propagate and Generate outputs are provided for use with the 'F182 Carry Lookahead Generator for high-speed expansion to longer word lengths. For ripple expansion, refer to the 'F382 ALU data sheet.

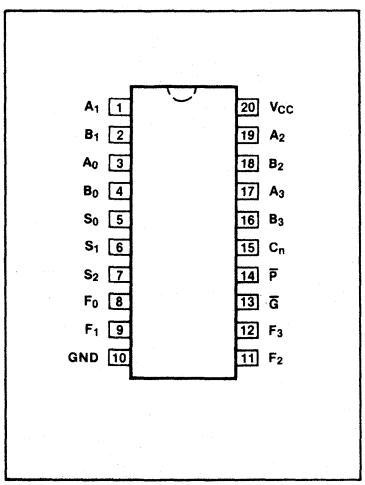
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A_0-A_3	A Operand Inputs	1/4	20μA/2.4mA
B_0-B_3	B Operand Inputs	1/4	20μA/2.4mA
S_0-S_1	Function Select Inputs	1/1	20μA/0.6mA
C_n	Carry Input	1/4	20μA/2.4mA
$\overline{G}$	Carry Generate Output (Active LOW)	50/33.3	1mA/20mA
$\overline{P}$	Carry Propagate Output (Active LOW)	50/33.3	1mA/20mA
F_0-F_3	Function Outputs	50/33.3	1mA/20mA

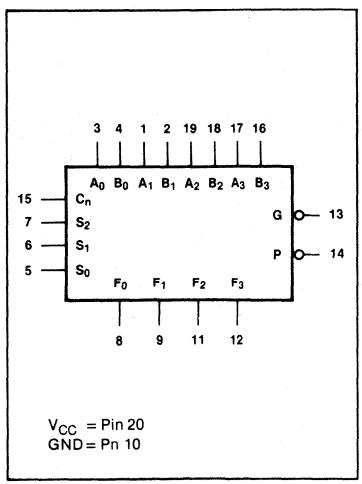
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

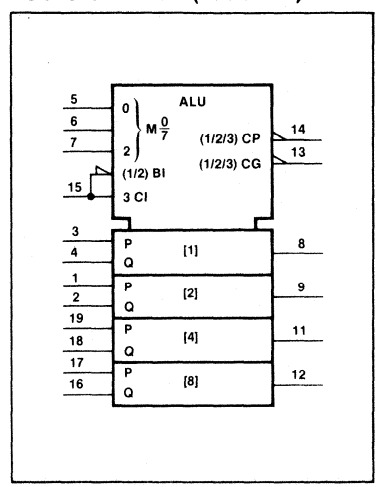
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ARITHMETIC LOGIC UNIT (ALU) FAST 54/74F382

Preview

4-Bit Arithmetic Logic Unit

- Performs six arithmetic logic functions
- Selectable LOW (clear) and HIGH (preset) functions
- Low input loading minimizes drive requirements
- Carry output for ripple expansion
- Overflow output for two's complement arithmetic

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F382		62mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F382N	
Plastic SO	N74F382D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

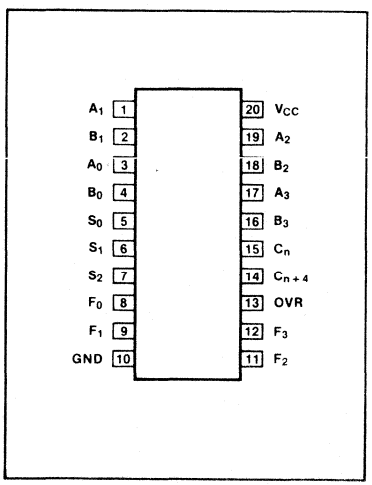
The 'F382 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select input codes force the Function outputs LOW or HIGH. An Overflow output is provided for convenience in two's complement arithmetic. A Carry output is provided for ripple expansion for high-speed expansion using a carry lookahead generator (refer to the 'F381 data sheet).

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

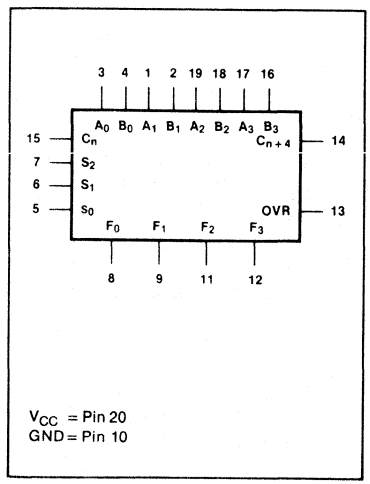
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A_0-A_3	A Operand Inputs	1/4	20μA/2.4mA
B_0-B_3	B Operand Inputs	1/4	20μA/2.4mA
S_0-S_2	Function Select Inputs	1/1	20μA/0.6mA
C_n	Carry Input	1/5	20μA/3mA
C_{n+4}	Carry Output	50/33.3	1mA/20mA
OVR	Overflow Output	50/33.3	1mA/20mA
F_0-F_3	Function Outputs	50/33.3	1mA/20mA

One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

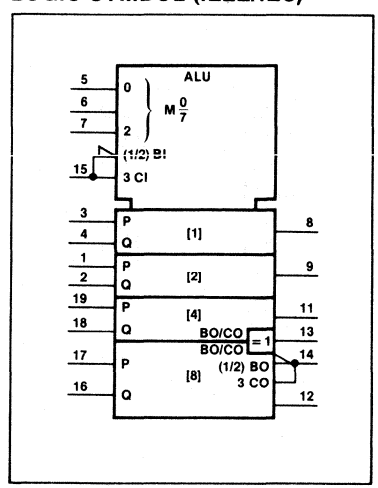
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



MULTIPLIER FAST 54/74F384

Preview

8-Bit Serial/Parallel Two's Complement Multiplier

DESCRIPTION

The 'F384 is an 8-bit sequential logic element that multiplies two numbers represented in two's complement notation. The device implements Booth's algorithm internally to produce a two's complement product that needs no subsequent correction. Parallel inputs accept and store an 8-bit multiplicand (X_0-X_7). The multiplier word is applied to the Y input in a serial bit stream, least significant bit first. The product is clocked out at the SP output, least significant bit first.

The K input is used for expansion to longer X words, using two or more 'F384 devices. The Mode Control (M) input is used to establish the most significant device. An asynchronous Parallel Load (PL) input clears the internal flip-flops to the start condition and enables the X latches to accept new multiplicand data.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F384		67mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F384N	
Plastic SO	N74F384D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

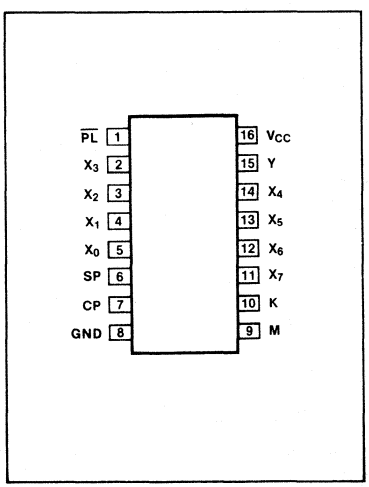
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
K	Serial Expansion Input	1.0/1.0	20μA/0.6mA
M	Mode Control Input	1.0/1.0	20μA/0.6mA
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	20μA/0.6mA
X_0-X_7	Multiplicand Data Inputs	1.0/1.0	20μA/0.6mA
Y	Serial Multiplier Input	1.0/1.0	20μA/0.6mA
SP	Serial X•Y Product Output	50/33.3	1mA/20mA

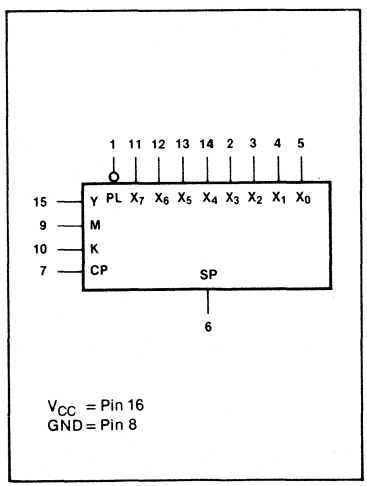
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

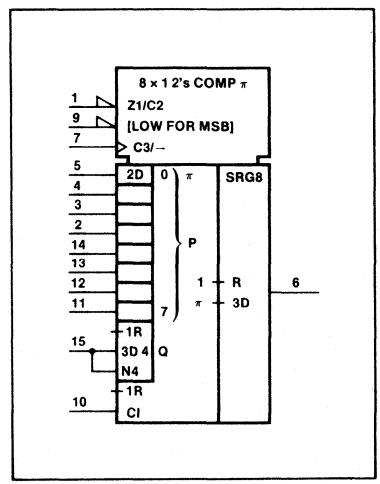
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ADDER FAST 54/74F385

Preview

Quad Serial Adder/Subtractor

- **Four independent adder/subtractors**
- **Two's complement arithmetic**
- **Synchronous operation**
- **Common Clear and Clock**
- **One's complement or magnitude-only capability**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F385	100MHz	68mA

DESCRIPTION

The 'F385 contains four serial adder/subtractors with common Clock and Clear inputs, but independent Operand and Mode Select inputs. Each adder/subtractor contains a sum flip-flop and a carry-save flip-flop for synchronous operations. Each circuit performs either A plus B or A minus B in two's complement notation, but can also be used for magnitude-only or one's complement operation. The 'F385 is designed for use with the 'F384 and 'F784 serial multipliers in implementing digital filters or butterfly networks in fast Fourier transforms.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74F385N	
Plastic SO	N74F385D	
Ceramic DIP		
Ceramic LLCC		

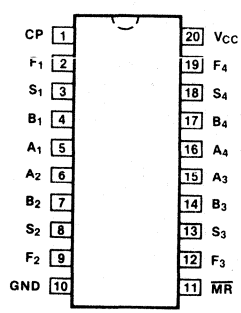
NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

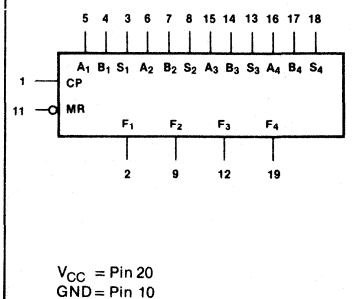
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A_1-A_4	A Operand Inputs	1.0/1.0	20μA/0.6mA
B_1-B_4	B Operand Inputs	1.0/1.0	20μA/0.6mA
S_1-S_4	Function Select Inputs	1.0/1.0	20μA/0.6mA
C_P	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20μA/0.6mA
F_1-F_4	Sum or Difference Outputs	50/33.3	1mA/20mA

One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

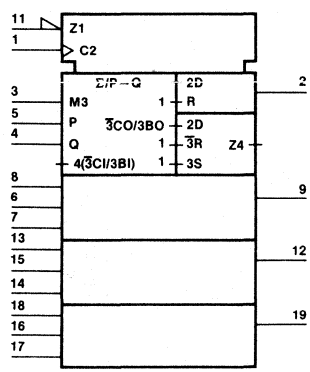
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ADDER FAST 54/74F385

Preview

Each adder contains two edge-triggered flip-flops to store the sum and carry, as shown in the Logic Diagram. Flip-flop state changes occur on the rising edge of the Clock Pulse (CP) input signal. The Select (S) input should be LOW for the Add (A plus B) mode and HIGH for the Subtract (A minus B) mode. A LOW signal on the asynchronous Master Reset (MR) input clears the sum flip-flop and resets the carry flip-flop to zero in the Add more or presets it to one in the Subtract mode.

In the Subtract mode, the B operand is internally complemented. Presetting the carry flip-flop to one completes the two's complement transformation by adding one to "A plus B" during the first (LSB) operation after MR is released. For one's complement subtraction, the carry flip-flop can be set to zero by making S LOW during the reset, then making S HIGH after the reset but before the next clock.

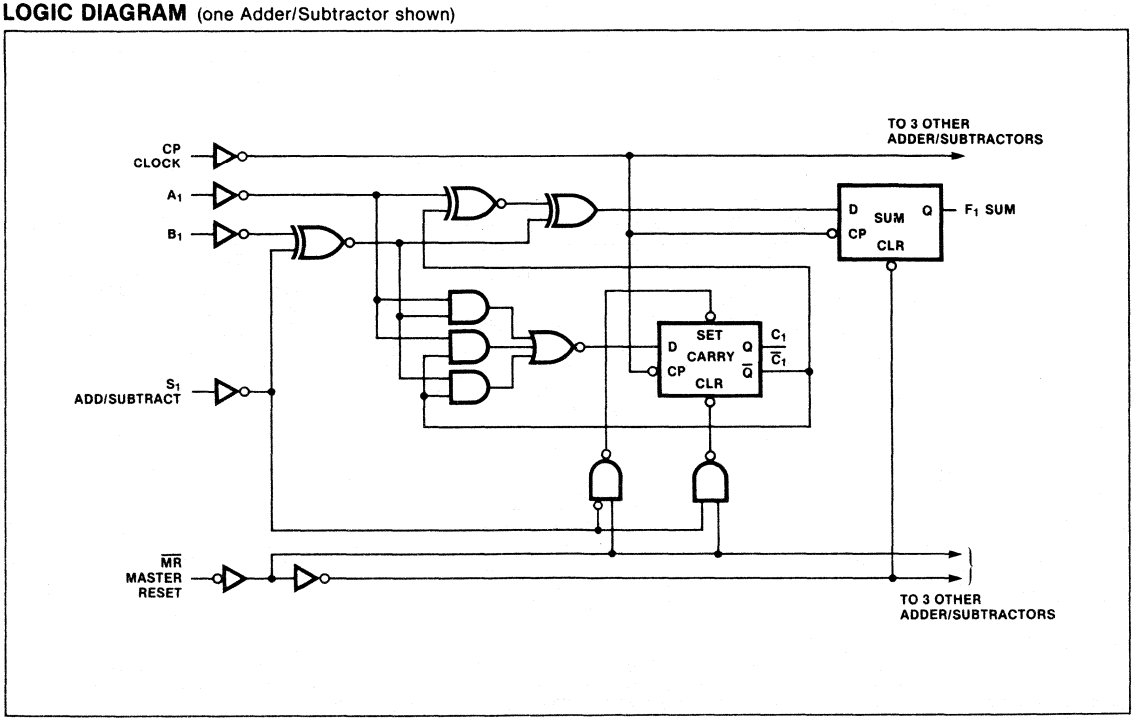
TRUTH TABLE

INPUTS*				INTERNAL CARRY		OUTPUT*	FUNCTION
$\overline{MR}$	S	A	B	C	C_1	F	
L	L	X	X	L	L	L	Clear
L	H	X	X	H	H	L	
H	L	L	L	L	L	L	Add
H	L	L	L	H	L	H	
H	L	L	H	L	L	H	
H	L	L	H	H	H	L	
H	L	H	L	L	L	H	
H	L	H	L	H	H	L	
H	L	H	H	L	H	L	
H	L	H	H	H	H	H	
H	H	L	L	L	L	H	Subtract
H	H	L	L	H	H	L	
H	H	L	H	L	L	L	
H	H	L	H	H	L	H	
H	H	H	L	L	H	L	
H	H	H	L	H	H	H	
H	H	H	H	L	L	H	
H	H	H	H	H	H	L	

H = HIGH voltage level
L = LOW voltage level
X = Don't care
* = Inputs before CP transition, output after C
C_1 = Carry flip-flop state before (C) and after (C_1) Clock transition

5

LOGIC DIAGRAM (one Adder/Subtractor shown)



ADDER FAST 54/74F385

Preview

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F385			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			68	95	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

ADDER FAST 54/74F385

Preview

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	70	100				70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to F_n	Waveform 1	3.5 4.0		8.0 9.0			3.5 4.0	9.0 10	ns
t_{PHL}	Propagation delay, $\overline{MR}$ to F_n	Waveform 2	5.5		12			5.5	13	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW A_n to CP	Waveform 3	15 15					15 15		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW A_n to CP	Waveform 3	0 0					0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW B_n or S_n to CP	Waveform 3	15 15					15 15		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW B_n or S_n to CP	Waveform 3	0 0					0 0		ns
$t_W(H)$ $t_W(L)$	CP pulse width, HIGH or LOW	Waveform 1	6.0 6.0					6.0 6.0		ns
$t_W(L)$	$\overline{MR}$ pulse width, LOW	Waveform 2	6.0					6.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	8.5					9.5		ns

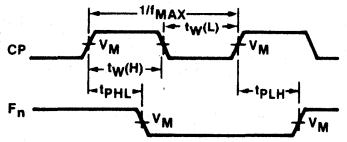
5

ADDER FAST 54/74F385

Preview

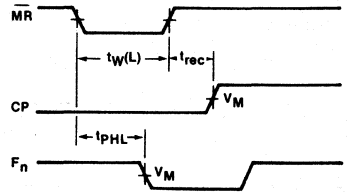
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



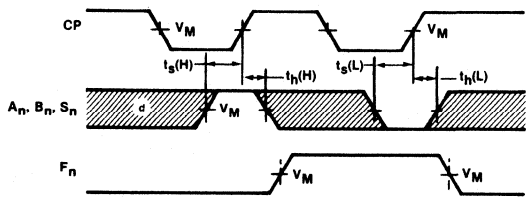
Waveform 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



Waveform 2

DATA SETUP AND HOLD TIMES



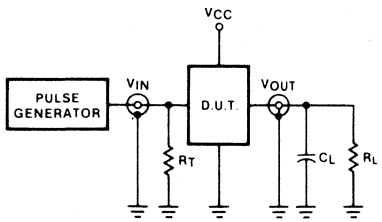
$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 3

TEST CIRCUITS AND WAVEFORMS

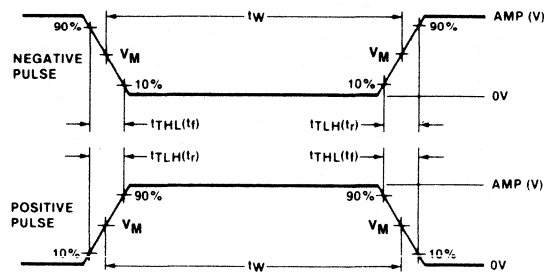
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

SHIFT REGISTER — FAST 54/74F395

Preliminary

4-Bit Cascadable Shift Register (3-State)

- **4-bit parallel load shift register**
- **Independent 3-State buffer outputs**
- **Separate Q_3' output for serial expansion**
- **Asynchronous Master Reset**

TYPE	TYPICAL, f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F395	105MHz	36mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F395N	
Plastic SO	N74F395D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
D_0–D_3	Data Inputs	1.0/1.0	20μA/0.6mA
PE	Enable Input	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	1.0/1.0	20μA/0.6mA
Q_3'	Serial Expansion Output	50/33	1.0mA/20mA
Q_0–Q_3	Data Outputs	150/33	3.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

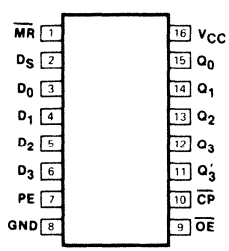
DESCRIPTION

The 'F395 is a 4-Bit Shift Register with serial and parallel synchronous operating modes and four 3-state buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is HIGH, data is loaded from the Parallel Data inputs (D_0–D_3) into the register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). When PE is LOW, the data at the Serial Data input (D_S) is loaded into the Q_0 flip-flop, and the data in the register is shifted one bit to the right in the direction ($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$) synchronous with the negative clock transition. The PE and Data inputs are fully edge-triggered and must be stable only one setup prior to the HIGH-to-LOW transition of the clock.

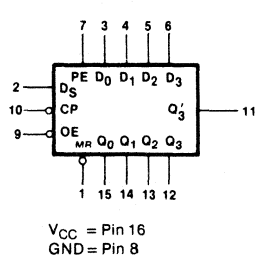
The Master Reset ($\overline{MR}$) is an asynchronous active-LOW input. When LOW, the $\overline{MR}$ overrides the clock and all other inputs and clears the register.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, or large capacitive loads. The active-LOW Output Enable ($\overline{OE}$) controls all four 3-state buffers independent of the register operation. The data in the register appears at the outputs when $\overline{OE}$ is LOW. The outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus when $\overline{OE}$ is HIGH. The output from the last stage is brought out separately. This output (Q_3') is tied to the Serial Data input (D_S) of the next register for serial expansion applications. The Q_3' output is not affected by the 3-state buffer operation.

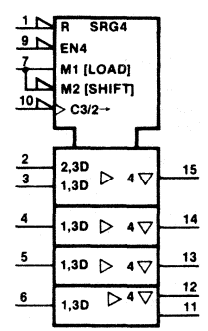
PIN CONFIGURATION



LOGIC SYMBOL



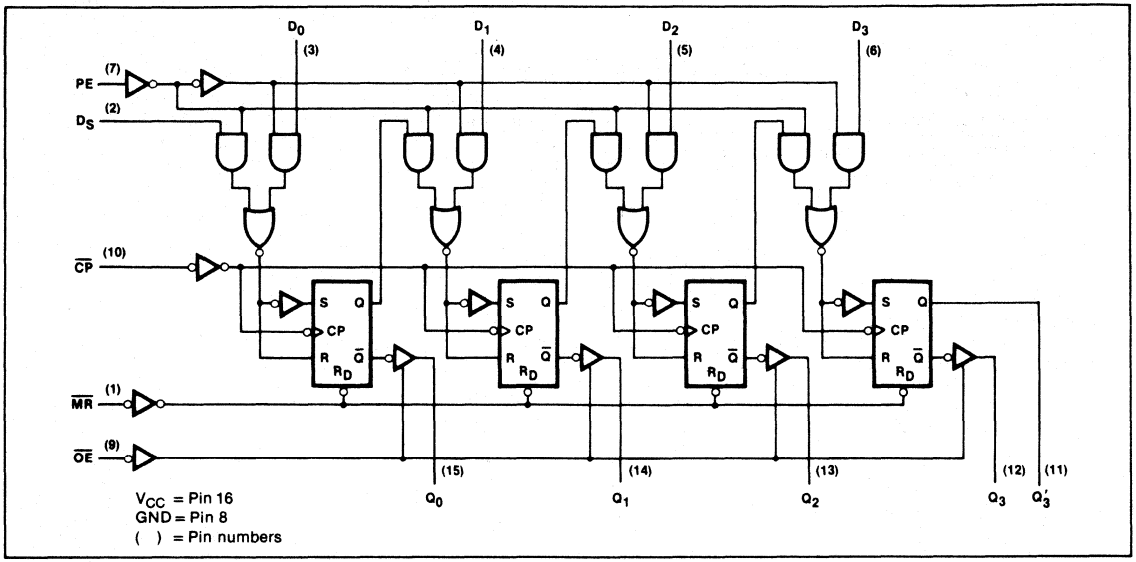
LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTER — FAST 54/74F395

Preliminary

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS			
	$\overline{MR}$	$\overline{CP}$	PE	D_S	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	L	X	X	X	X	L	L	L	L
Shift right	H	↓	l	l	X	L	q_0	q_1	q_2
	H	↓	l	h	X	H	q_0	q_1	q_2
Parallel load	H	↓	h	X	l	L	L	L	L
	H	↓	h	X	h	H	H	H	H

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS	
	$\overline{OE}$	Q_n (Register)	Q_0, Q_1, Q_2, Q_3	Q_3'
Read	L	L	L	L
	L	H	H	H
Disable buffers	H	L	(Z)	L
	H	H	(Z)	H

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the HIGH-to-LOW clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition
q_n = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW clock transition
X = Don't care
(Z) = HIGH impedance "off" state
↓ = HIGH-to-LOW transition

SHIFT REGISTER FAST 54/74F395

Preliminary

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER		54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−3	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

SHIFT REGISTER — FAST 54/74F395

Preliminary

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F395 Min	54/74F395 Typ[2]	54/74F395 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Q_3'	Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
			Q_0, Q_1, Q_2, Q_3		2.7			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	Q_3'	I_{OL} = MAX Com'l		0.35	0.5	V
			Q_0, Q_1, Q_2, Q_3	I_{OL} = MAX		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MIN, V_{IH} = MIN, V_O = 2.4V	Q_0, Q_1, Q_2, Q_3				50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MIN, V_{IH} = MIN, V_O = 0.5V	Q_0, Q_1, Q_2, Q_3				−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	Q_3'		−60		−150	mA
			Q_0, Q_1, Q_2, Q_3					mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	Condition 1					mA
			Condition 2					mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with D_S and Master Reset at 4.5V. The Data inputs grounded and outputs open under the following conditions: *Condition 1:* $\overline{OE}$ at 4.5V. A momentary 3V, then ground, applied to $\overline{CP}$. *Condition 2:* Ground $\overline{OE}$ and $\overline{CP}$ inputs.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	105			90		90		MHz
t_{PLH}	Propagation delay Clock to Buffer outputs	Waveform 1	3.5		7.0	3.0	10.0	3.5	9.0	ns
t_{PHL}			3.5		7.0	3.0	10.0	3.5	9.0	
t_{PLH}	Propagation delay Clock to Q_3' output	Waveform 1	3.5		7.0	3.0	10.0	3.5	9.0	ns
t_{PHL}			3.5		7.0	3.0	10.0	3.5	9.0	
t_{PHL}	Propagation delay, $\overline{MR}$ to output	Waveform 2	4.5		12.0	4.5	14.5	4.5	14.0	ns
t_{PZH}	Enable time to HIGH level	Waveform 3	2.0		11.5	2.0	14.0	2.0	12.5	ns
t_{PZL}	Enable time to LOW level	Waveform 4	2.0		7.5	2.0	10.0	2.0	8.5	ns
t_{PHZ}	Disable time from HIGH level	Waveform 3	2.0		7.0	2.0	8.0	2.0	8.0	ns
t_{PLZ}	Disable time from LOW level	Waveform 4	2.0		5.5	2.0	7.5	2.0	6.5	ns

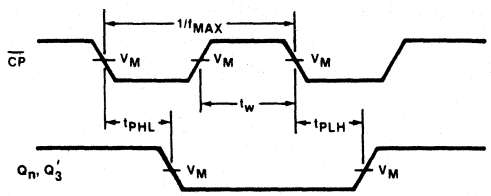
NOTE

Subtract 0.2ns from minimum values for SO package.

Preliminary

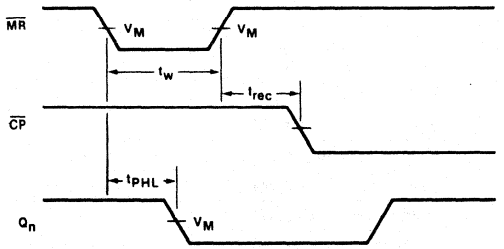
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS
AND CLOCK PULSE WIDTH



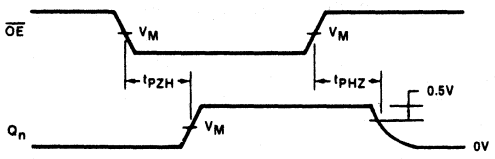
Waveform 1

MASTER RESET PULSE WIDTH,
MASTER RESET TO OUTPUT DELAY AND
MASTER RESET TO CLOCK RECOVERY TIME



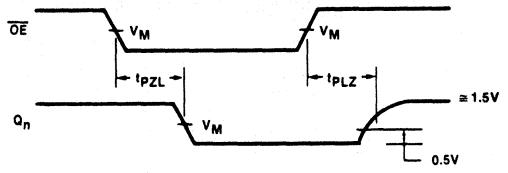
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND
DISABLE TIME FROM HIGH LEVEL



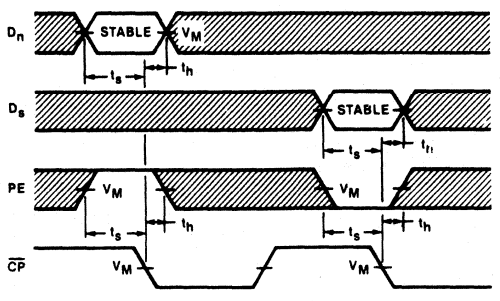
Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND
DISABLE TIME FROM LOW LEVEL



Waveform 4

PARALEL ENABLE AND DATA
SETUP AND HOLD TIMES



Waveform 5

$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

5

SHIFT REGISTER — FAST 54/74F395

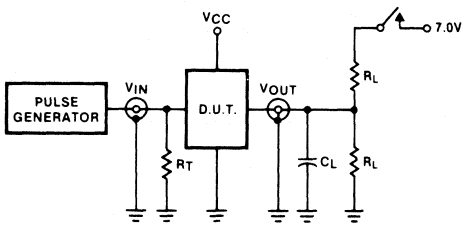
Preliminary

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_w	Clock pulse width	Waveform 1	5.0			5.0		5.0		ns
t_w	Master Reset pulse width	Waveform 2	5.0			5.0		5.0		ns
t_s	Setup time, Data to clock	Waveform 5	4.0			4.0		4.0		ns
t_h	Hold time, Data to clock	Waveform 5	0			1.0		1.0		ns
t_s	Setup time, PE to clock	Waveform 5	8.0			9.0		9.0		ns
t_h	Hold time, PE to clock	Waveform 5	0			0		0		ns
t_{rec}	Recovery time, $\overline{MR}$ to clock	Waveform 2	7.0			9.0		8.0		ns

TEST CIRCUITS AND WAVEFORMS

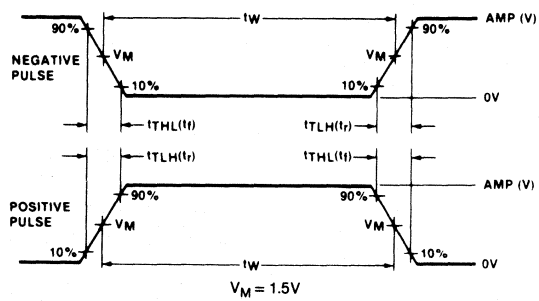
TEST CIRCUIT FOR 3-STATE OUTPUTS



SWITCH POSITION

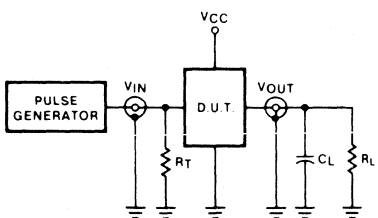
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

INPUT PULSE DEFINITIONS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

TEST CIRCUIT FOR TOTEM-POLE OUTPUT (Q_3' ONLY)



DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Preview

'F398 — Quad 2-Port Register With True & Complement Outputs
'F399 — Quad 2-Port Register

- **Select inputs from two data sources**
- **Fully positive edge-triggered operation**
- **Both True and Complement outputs — 'F398**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F398		25mA
74F399		22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F398N • N74F399N	
Plastic SO	N74F398D • N74F399D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F398 and 'F399 are the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock. The 'F399 is the 16-pin version of the 'F398, with only the Q outputs of the flip-flops available.

The 'F398 and 'F399 are high-speed quad 2-port registers. They select 4 bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x}, I_{1x}) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The 'F398 has both Q and $\overline{Q}$ outputs.

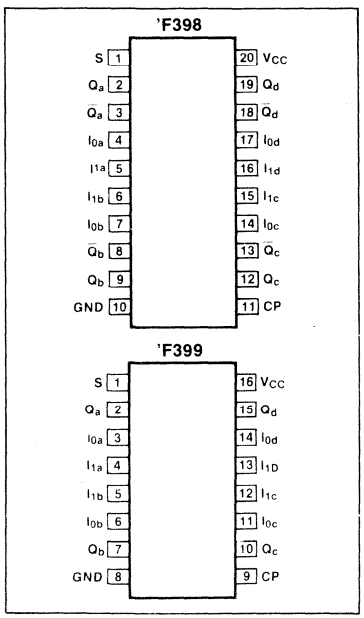
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
S	Common select input	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
I_{0a}-I_{0d}	Data inputs from source 0	1.0/1.0	20μA/0.6mA
I_{1a}-I_{1d}	Data inputs from source 1	1.0/1.0	20μA/0.6mA
Q_a-Q_d	Register true outputs	50/33	1.0mA/20mA
$\overline{Q}_a$-$\overline{Q}_d$	Register complementary outputs ('F398)	50/33	1.0mA/20mA

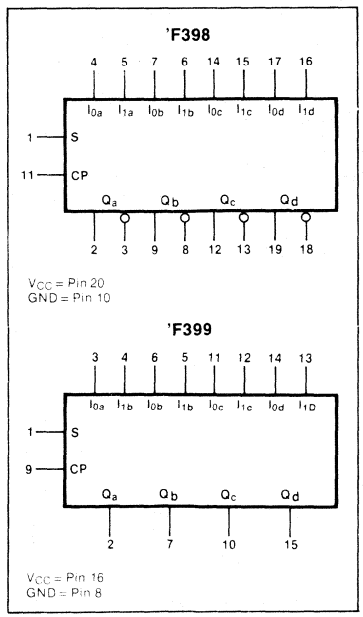
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

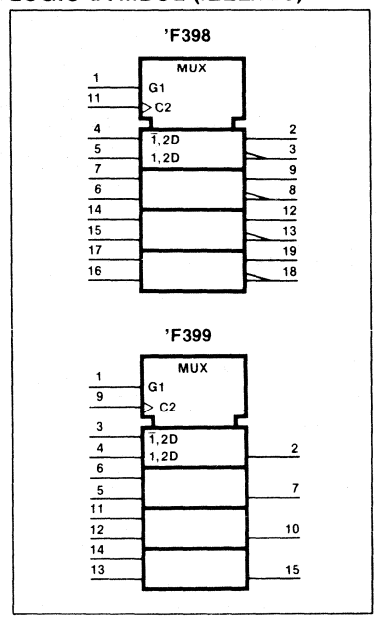
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



REGISTERS — FAST 54/74F398, 54/74F399

Preview

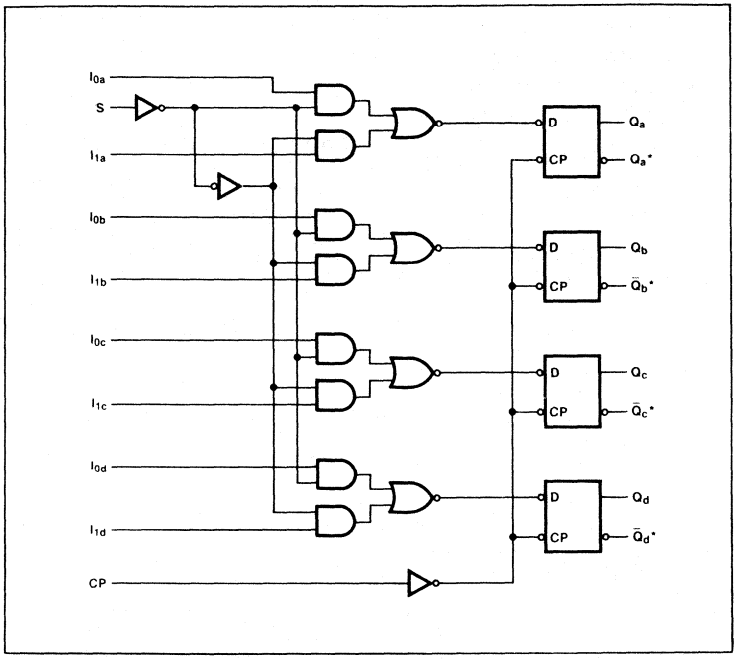
FUNCTION TABLE

INPUTS			OUTPUTS	
S	I_0	I_1	Q	$\overline{Q}$*
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

*'F398 only.

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
H = HIGH voltage level
X = Don't Care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F398, 'F399			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-60	-80	-150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	'F398		25	38	mA
			'F399		22	34	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH}, V_{IN} = GND, I_{CCL}, V_{IN} = Open.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F			54F		74F		UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Input clock frequency	Waveform 1	100	140				100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q or $\overline{Q}$	Waveform 1	3.5 5.0	6.0 8.5	8.0 11			3.5 5.0	9.0 12	ns

NOTE
Subtract 0.2 ns from minimum values for SO Package.

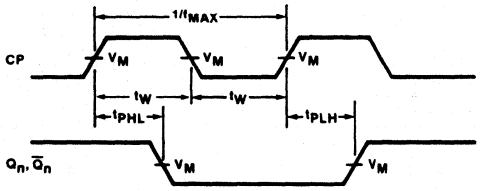
AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F			54F		74F		UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW I_n to CP	Waveform 2	4.0 4.0					4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW I_n to CP	Waveform 2	1.0 1.0					1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW S to CP	Waveform 2	7.5 7.5					8.5 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW S to CP	Waveform 2	0 0					0 0		ns
$t_W(H)$ $t_W(L)$	Clock pulse width, HIGH or LOW	Waveform 1	6.0 6.0					6.0 6.0		ns

Preview

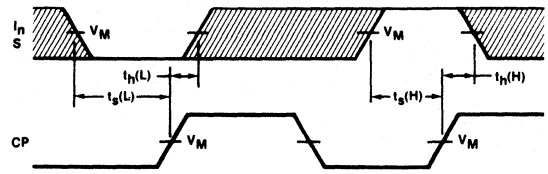
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

DATA SETUP AND HOLD TIMES

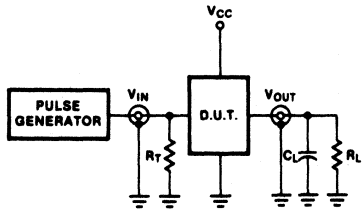


Waveform 2

V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

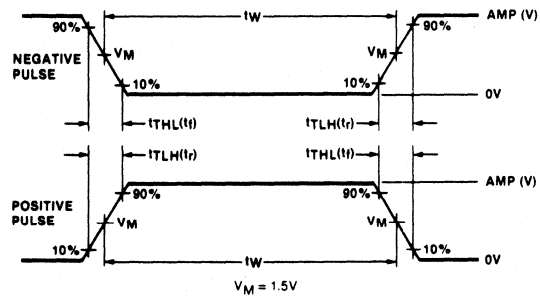
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND, see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

MULTI-MODE BUFFERED LATCH

FAST 54/74F412

Preview

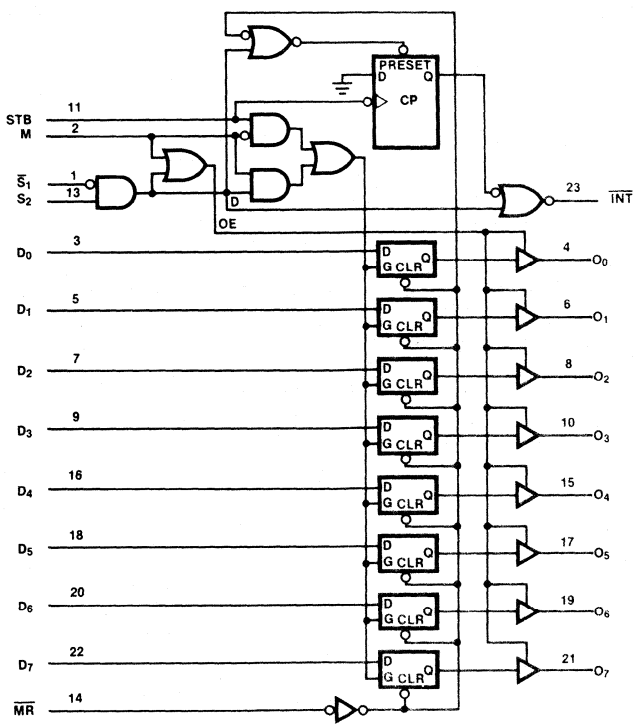
This high-performance 8-bit parallel expandable buffer register incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus-organized input/output ports. The 3-State Data outputs can be connected to a common data bus and controlled from the appropriate Select inputs to receive or transmit data. An integral status flip-flop provides package-busy or request-interrupt commands.

The eight data latches are fully transparent when the internal Gate Enable (G) input is HIGH and the outputs are enabled (OE = H). Latch transparency is selected by the Mode control (M), Select (S_1 and S_2), and the Strobe (STB) inputs, and during transparency each Data output (O_n) follows its respective Data input (D_n). This mode of operation can be terminated by clearing, deselecting, or holding the data latches.

An input mode or an output mode is selectable from this single input line. In the input mode (MD = L), the eight data latch inputs are enabled when the strobe is HIGH, regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken LOW, the latches will store the most-recently setup data.

In the output mode (M = H), the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the Select (S_1 and S_2) inputs.

LOGIC DIAGRAM



5

MULTI-MODE BUFFERED LATCH — FAST 54/74F412

Preview

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−3	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F412			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.4	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V			2	50	μA
I_{OZL}	Off-state output current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		38	50	mA
			I_{CCL} Outputs LOW		45	60	mA
			I_{CCZ} Outputs OFF		45	60	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

MULTI-MODE BUFFERED LATCH FAST 54/74F412

Preview

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to O_n	Waveform 4	3.5 2.5		8.5 6.5			3.0 2.0	9.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_1$, S_2 or STB to O_n	Waveform 4	8.5 7.5		18.5 16.0			7.5 6.5	20.5 17.5	ns
t_{PZH} t_{PZL}	Enable time, HIGH or LOW $\overline{S}_1$ to O_n	Waveforms 2 & 3	7.5 6.5		16.0 14.0			6.5 5.5	17.5 15.0	ns
t_{PHZ} t_{PLZ}	Disable time, HIGH or LOW $\overline{S}_1$ to O_n	Waveforms 2 & 3	4.5 6.5		10.5 14.0			4.0 5.5	11.5 15.0	ns
t_{PZH} t_{PZL}	Enable time, HIGH or LOW S_2 to O_n	Waveforms 2 & 3	7.5 5.0		16.0 11.5			6.5 4.5	17.5 12.5	ns
t_{PHZ} t_{PLZ}	Disable time, HIGH or LOW S_2 O_n	Waveforms 2 & 3	4.5 5.5		9.5 12.0			4.0 4.5	10.5 13.0	ns
t_{PZH} t_{PZL}	Enable time, HIGH or LOW M to O_n	Waveforms 2 & 3	5.0 5.0		11.0 11.0			4.5 4.5	12.0 12.0	ns
t_{PHZ} t_{PLZ}	Disable time, HIGH or LOW M to O_n	Waveforms 2 & 3	4.0 5.0		9.0 11.0			3.5 4.5	10.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_1$ or $\overline{S}_2$ to $\overline{INT}$	Waveform 1	4.5 4.5		9.5 10.5			4.0 4.0	10.5 11.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to O_n	Waveform 4	7.5		16.0			6.5	17.5	ns
t_{PHL}	Propagation delay STB to $\overline{INT}$	Waveform 1	6.5		14.0			5.5	15.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time D_n to $\overline{S}_1$, S_2, or STB	Waveform 5	0 0					0 0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to $\overline{S}_1$, S_2 or STB	Waveform 5	8.0 8.0					7.0 7.0		ns
$t_w(H)$ $t_w(L)$	$\overline{S}_1$, S_2 or STB Pulse width	Waveform 1	8.0 8.0					9.0 9.0		ns
$t_w(L)$	$\overline{MR}$ pulse width	Waveform 4	8.0					9.0		ns

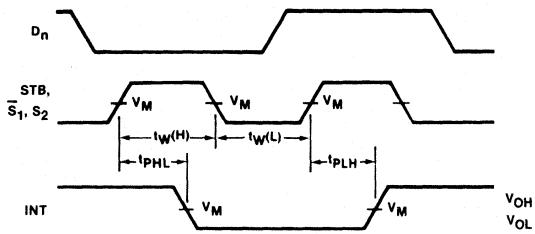
5

MULTI-MODE BUFFERED LATCH FAST 54/74F412

Preview

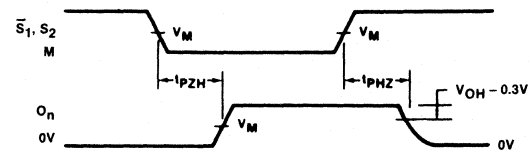
AC WAVEFORMS

STB, S_1, S_2 TO $\overline{INT}$ DELAYS AND STB, S_1, S_2 PULSE WIDTH



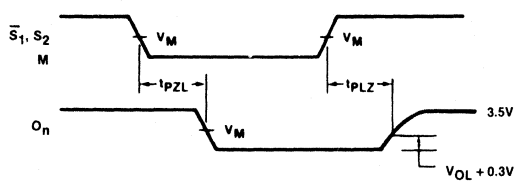
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



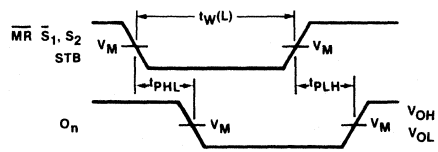
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



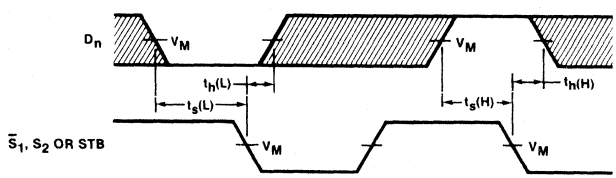
Waveform 3

PROPAGATION DELAY DATA TO O OUTPUTS



Waveform 4

DATA SETUP AND HOLD TIMES



Waveform 5

$V_M = 1.5V$

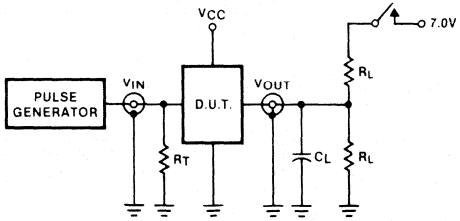
The shaded areas indicate when the input is permitted to change for predictable output performance.

MULTI-MODE BUFFERED LATCH FAST 54/74F412

Preview

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



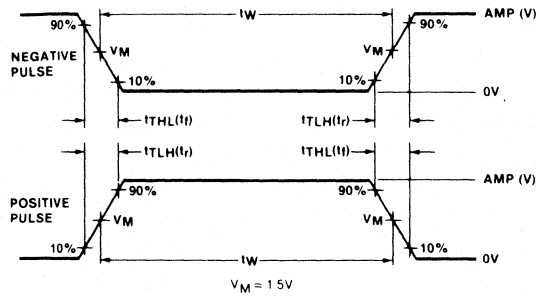
SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

COMPARATOR — FAST 54/74F521

8 Bit Identity Comparator

- **Compares two 8-bit words in 6.5ns typical**
- **Expandable to any word length**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F521	7.0ns	20.0mA

DESCRIPTION

The 'F521 is an expandable 8-bit comparator. It compares two words of up to 8 bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active-LOW enable input.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F521N	
Plastic SO	N74F521D	
Ceramic DIP		S54F521F
Ceramic LLCC		S54F521G

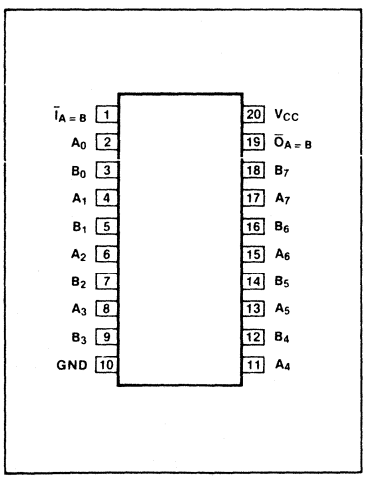
NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

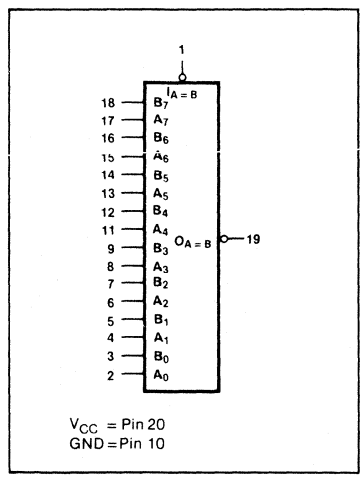
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A_0-A_7	Word A Inputs	1.0/1.0	20μA/0.6mA
B_0-B_7	Word B Inputs	1.0/1.0	20μA/0.6mA
$\overline{I}_{A=B}$	Expansion or Enable Input (Active-LOW)	1.0/1.0	20μA/0.6mA
$\overline{O}_{A=B}$	Identity Output (Active-LOW)	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION

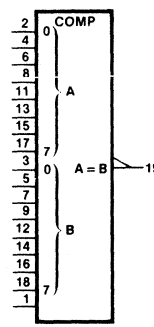


LOGIC SYMBOL



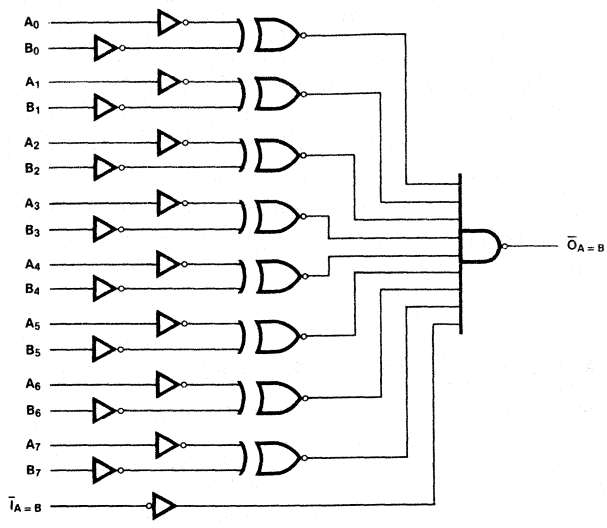
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)



COMPARATOR FAST 54/74F521

LOGIC DIAGRAM



5

TRUTH TABLE

Inputs		Output
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	– 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F521			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 0.73	– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				– 0.4	– 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V			– 60	– 90	– 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		24	36	mA
			I_{CCL}	Outputs LOW		15.5	23	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. For I_{CCH} all inputs are grounded except B_0, which is at 4.5V. For I_{CCL} all inputs are grounded.

COMPARATOR FAST 54/74F521

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

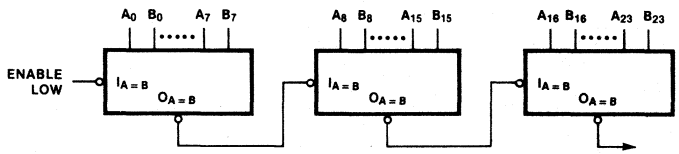
PARAMETER	TEST CONDITIONS	54/74F			54F		74F		UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			T_A, V_{CC} = Mil $C_L = 50pF$ $R_L = 500\Omega$		T_A, V_{CC}=Com'l $C_L = 50pF$ $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} A_N or B_N to $\overline{O}_{A=B}$	Waveform 1, 2	3.5 4.0	8.0 8.0	9.5 9.0	3.5 2.5	15 12	3.5 4.0	11 10.5	ns
t_{PLH} Propagation delay t_{PHL} $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	Waveform 2	3.0 3.5	5.0 6.5	6.5 7.0	3.0 3.5	12.0 9.0	3.0 3.5	7.5 8.0	ns

LOAD

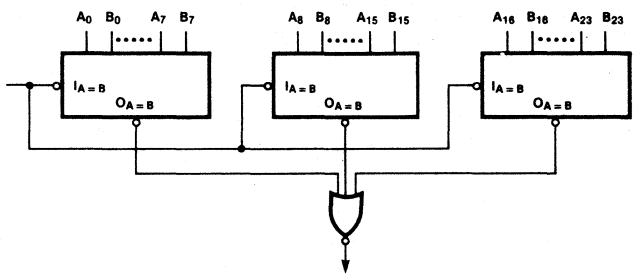
Subtract 0.2ns from minimum values for SO package.

APPLICATIONS

RIPPLE EXPANSION



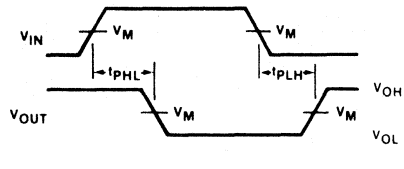
PARALLEL EXPANSION



5

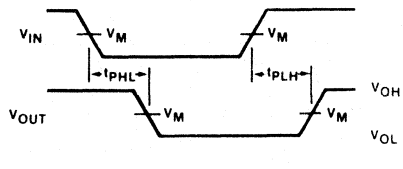
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS

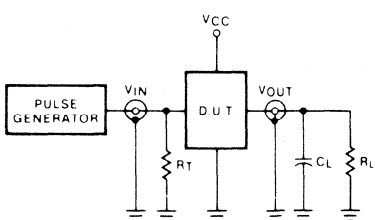


Waveform 2

$V_M = 1.5V$

TEST CIRCUITS AND WAVEFORMS

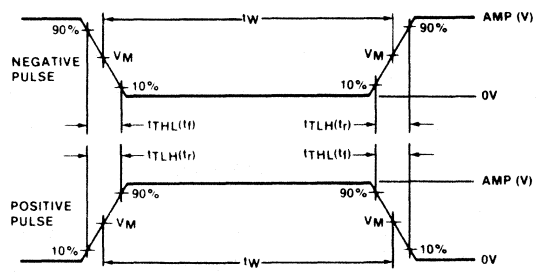
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

COMPARATOR FAST 54/74F524

Preview

8-Bit Register Comparator (Open-Collector + 3-State)

- 8-bit bidirectional register with bus-oriented input-output
- Independent serial input-output to register
- Register bus comparator with 'equal to', 'greater than' and 'less than' outputs
- Cascadable in groups of 8 bits
- Open-collector comparator outputs for AND-wired expansion
- Two's complement or magnitude compare

TYPE	TYPICAL, f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F524		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F524N	
Plastic SO	N74F524D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
S_0, S_1	Mode Select Inputs	1.0/1.0	20μA/0.6mA
C/SI	Status Priority or Serial Data Input	1.0/1.0	20μA/0.6mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
$\overline{SE}$	Status Enable Input (Active LOW)	1.0/1.0	20μA/0.6mA
M	Compare Mode Select Input	1.0/1.0	20μA/0.6mA
I/O_0–I/O_7	Parallel Data Inputs or	2.5/1.0	50μA/0.6mA
	3-State Parallel Data Outputs	150/33	3.0mA/20mA
C/SO	Status Priority or Serial Data Output	50/33	1.0mA/20mA
LT	Register Less Than Bus Output	OC*/33	OC*/20mA
EQ	Register Equal To Bus Output	OC*/33	OC*/20mA
GT	Register Greater Than Bus Output	OC*/33	OC*/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.
*OC = Open Collector.

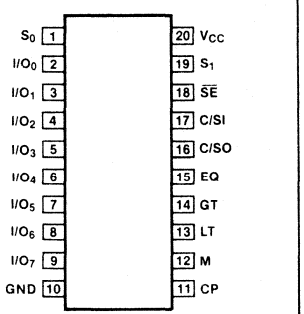
5

DESCRIPTION

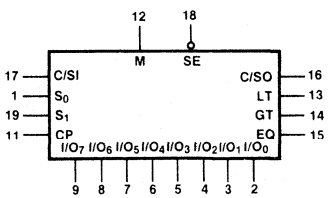
The 'F524 is an 8-bit bidirectional register with parallel input and output plus serial input and output progressing from LSB to MSB. All data inputs, serial and parallel, are loaded by the rising edge of the input clock. The device functions are controlled by two control lines (S_0, S_1) to execute shift, load, hold and read out.

An 8-bit comparator examines the data stored in the registers and on the data bus. Three true-HIGH, open-collector outputs representing 'register equal to bus', 'register greater than bus' and 'register less than bus' are provided. These outputs can be disabled to the OFF state by the use of Status Enable ($\overline{SE}$). A mode control has also been provided to allow two's complement as well as magnitude compare. Linking inputs are provided for expansion to longer words.

PIN CONFIGURATION



LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)

COMPARATOR

FAST 54/74F524

Preview

FUNCTIONAL DESCRIPTION

The 'F524 contains eight D-type flip-flops connected as a shift register with provision for either parallel or serial loading. Parallel data may be read from or loaded into the registers via the data bus I/O_0-I/O_7. Serial data is entered from the C/SI input and may be shifted into the register and out through the C/SO output. Both parallel and serial data entry occurs on the rising edge of the input clock (CP). The operation of the shift register is controlled by two signals, S_0 and S_1, according to the Select Truth Table. The 3-state parallel output buffers are enabled only in the Read mode.

SELECT TRUTH TABLE

S_0	S_1	OPERATION
L	L	HOLD—Retains data in shift register
L	H	READ—Read contents in register onto data bus
H	L	SHIFT—Allows serial shifting on next rising clock edge
H	H	LOAD—Load data on bus into register.

H = HIGH Voltage Level
L = LOW Voltage Level

One port of an 8-bit comparator is attached to the data bus while the other port is tied to the outputs of the internal register. Three active-OFF, open-collector outputs indicate whether the contents held in the shift register are 'greater than' (GT), 'less than' (LT), or 'equal to (EQ) the data on the input bus. A HIGH signal on the Status Enable ($\overline{SE}$) input disables these outputs to the OFF state. A Mode control input (M) allows selection between a straightforward magnitude compare or a comparison between two's complement numbers.

NUMBER REPRESENTATION SELECT TABLE

M	OPERATION
L	Magnitude compare
H	Two's complement compare

H = HIGH Voltage Level
L = LOW Voltage Level

For 'greater than' or 'less than' detection, the C/SI input must be held HIGH, as indicated in the Status Truth Table. The internal logic is arranged such that a LOW signal on the C/SI input disables the 'greater than' and 'less than' outputs. The C/SO output will be forced HIGH if the 'equal to' status condition exists, otherwise C/SO will be held LOW. These facilities enable the 'F524 to be cascaded for word lengths greater than 8 bits.

STATUS TRUTH TABLE (Hold Mode)

INPUTS			OUTPUTS			
$\overline{SE}$	C/SI	Data Comparison	EQ	GT	LT	C/SO
H	X	X	H	H	H	①
L	H	O_A-O_H > I/O_0-I/O_7	L	H	H	L
L	L	O_A-O_H = I/O_0-I/O_7	H	H	H	H
L	H	O_A-O_H < I/O_0-I/O_7	L	H	H	L
L	H	O_A-O_H > I/O_0-I/O_7	L	H	L	L
L	H	O_A-O_H = I/O_0-I/O_7	H	L	L	H
L	H	O_A-O_H < I/O_0-I/O_7	L	L	H	L

① = HIGH if data are not equal, otherwise LOW
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Word length expansion (in groups of 8 bits) can be achieved by connecting the C/SO output of the more significant byte to the C/SI input of the next less significant byte and also to its own $\overline{SE}$ input (see Figure a). The C/SI input of the most significant device is held HIGH while the $\overline{SE}$ input of the least significant device is held LOW. The corresponding status outputs are AND-wired together. In the case of two's complement number compare, only the Mode input to the most significant device should be HIGH. The Mode inputs to all other cascaded devices are held LOW.

Suppose that an inequality condition is detected in the most significant device. Assuming that the byte stored in the register is greater than the byte on the data bus, then the EQ and LT outputs will be pulled LOW, whereas the GT output will float HIGH. Also, the C/SO output of the most significant device will be forced LOW, disabling the subsequent devices but enabling its own status outputs. The correct status condition is thus indicated. The same applies if the registered byte is less than the data byte, only in this case the EQ and GT outputs go LOW, whereas LT output floats HIGH.

If an equality condition is detected in the most significant device, its C/SO output is forced HIGH. This enables the next less significant device and also disables its own status outputs. In this way, the status output priority is handed down to the next less significant device which now effectively becomes the most significant byte. The worst case propagation delay for a compare operation involving 'n' cascaded 'F524s will be when an equality condition is detected in all but the least significant byte. In this case, the status priority has to ripple all the way down the chain before the correct status output is established. Typically, this will take 35 + 6 (n-s) ns.

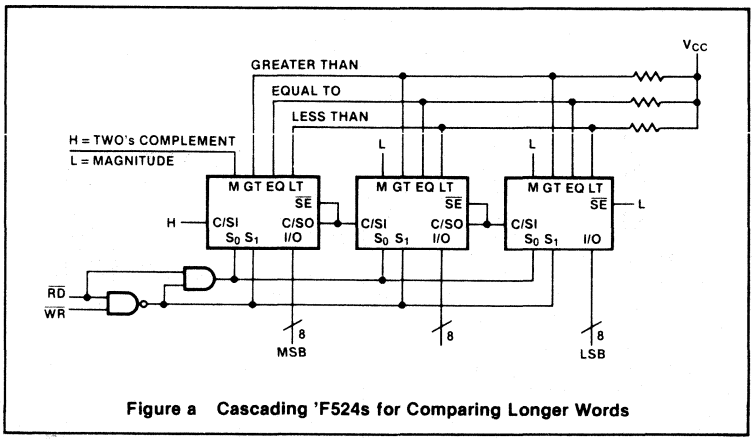
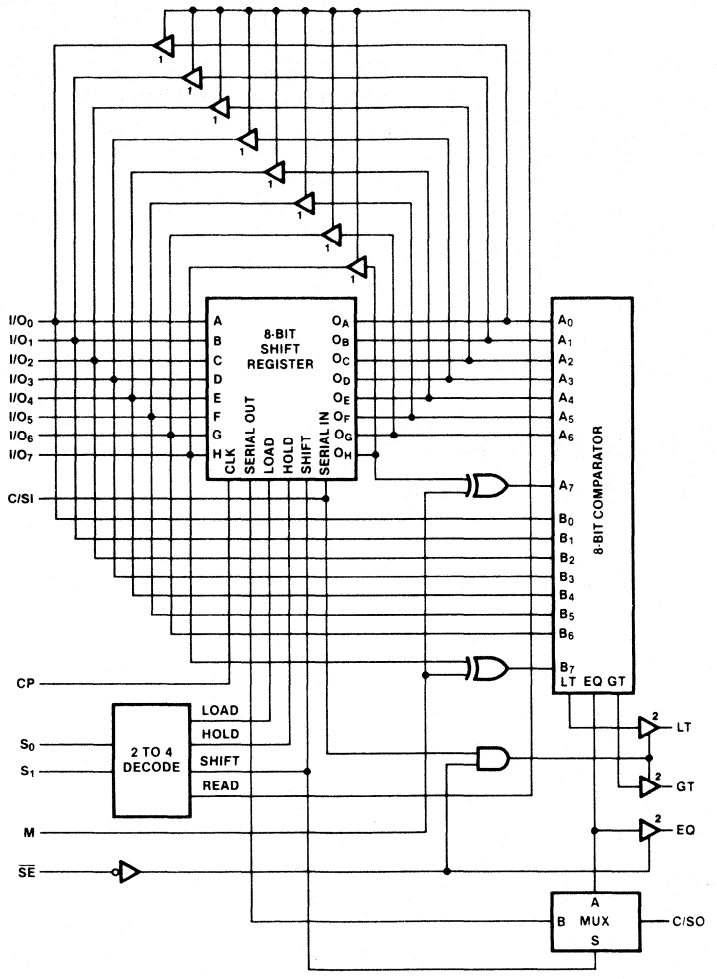


Figure a Cascading 'F524s for Comparing Longer Words

COMPARATOR FAST 54/74F524

Preview

LOGIC DIAGRAM



NOTES
1. 3-State Output
2. Open-Collector Output

5

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

COMPARATOR FAST 54/74F524

Preview

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 3	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	– 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F524			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	Mil	2.4	3.4		V
				Com'l	2.7	3.4		V
			I_{OH} = – 1mA	Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 0.73	– 1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V				2	50	μA
I_{OZL}	Off-state output current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				– 2	– 50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				– 0.4	– 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 60	– 80	– 150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH				mA
			I_{CCL}	Outputs LOW			180	mA
			I_{CCZ}	Outputs OFF				mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

COMPARATOR FAST 54/74F524

Preview

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum shift frequency	Waveform 4	50					50		MHz
t_{PLH} t_{PHL}	Propagation delay I/O_n to EQ	Waveform 2	9.5 6.0		20 12			9.5 6.0	22.5 13	ns
t_{PLH} t_{PHL}	Propagation delay I/O_n to GT	Waveform 2	8.5 7.0		18 14.5			8.5 7.0	19 15.5	ns
t_{PLH} t_{PHL}	Propagation delay I/O_n to LT	Waveform 2	7.0 6.0		16 14			7.0 6.0	18 15	ns
t_{PLH} t_{PHL}	Propagation delay I/O_n to C/SO	Waveform 2	9.0 6.0		19.5 13			9.0 6.0	21.5 14	ns
t_{PLH} t_{PHL}	Propagation delay CP to EQ	Waveform 4	10.5 4.0		22 9.0			10.5 3.5	24.5 10	ns
t_{PLH} t_{PHL}	Propagation delay GP to GT	Waveform 4	10 9.0		21 20			10 9.0	22 21.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to LT	Waveform 4	9.0 6.0		19.5 12.5			9.0 6.0	21 13.5	ns
t_{PLH}	Propagation delay CP to C/SO (compare)	Waveform 4	8.5		18.5			8.5	21.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to C/SO (serial shift)	Waveform 4	5.0 5.0		10.5 10			5.0 5.0	11.5 11	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to GT	Waveform 1	9.0 3.5		19 8.5			9.0 3.0	20 9.5	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to LT	Waveform 1	8.0 4.0		17 8.5			8.0 4.0	18 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to C/SO	Waveform 2	7.0 6.0		14.5 12			7.0 6.0	15.5 13	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to EQ	Waveform 2	4.0 2.5		8.0 6.0			4.0 2.5	9.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to GT	Waveform 2	7.5 3.5		16 8.0			7.5 3.5	17 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to LT	Waveform 2	5.0 3.5		11 8.0			5.0 3.5	12 9.0	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to C/SO	Waveform 2	4.5 4.0		9.5 9.5			4.5 4.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay M to GT	Waveform 2	8.0 7.0		17 15.5			8.0 7.0	18 17	ns
t_{PLH} t_{PHL}	Propagation delay M to LT	Waveform 2	8.5 5.5		19 12			8.5 5.5	21 13	ns
t_{PZH} t_{PZL}	Output enable time S_0, S_1 to I/O_n	Waveform 5 Waveform 6	6.0 6.5		13 14.5			6.0 6.5	14 15.5	ns
t_{PHZ} t_{PLZ}	Output disable time S_0, S_1 to I/O_n	Waveform 5 Waveform 6	5.0 5.5		10 12.5			5.0 5.5	11 13.5	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

5

COMPARATOR FAST 54/74F524

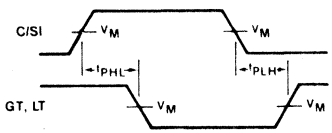
Preview

AC SETUP REQUIREMENTS

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ Setup time, HIGH or LOW $t_s(L)$ I/O_n to CP	Waveform 3	5.0 5.0						5.0 5.0	ns
$t_h(H)$ Hold time, HIGH or LOW $t_h(L)$ I/O_n to CP	Waveform 3	0 0						0 0	ns
$t_s(H)$ Setup time, HIGH or LOW $t_s(L)$ S_0, S_1 to CP	Waveform 3	10 10						10 10	ns
$t_s(H)$ Setup time, HIGH or LOW $t_s(L)$ C/SI to CP	Waveform 3	5.0 7.0						5.0 7.0	ns
$t_h(H)$ Hold time, HIGH or LOW $t_h(L)$ C/SI to CP	Waveform 3	0 0						0 0	ns
$t_w(H)$ Clock pulse width HIGH	Waveform 4	4.0						4.0	ns

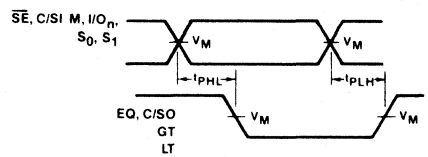
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



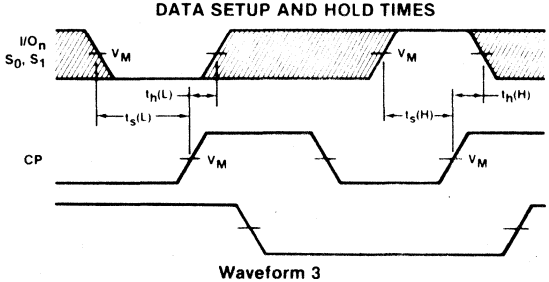
Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



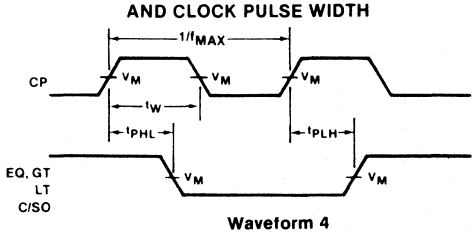
Waveform 2

DATA SETUP AND HOLD TIMES



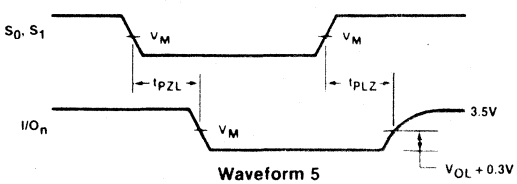
Waveform 3

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



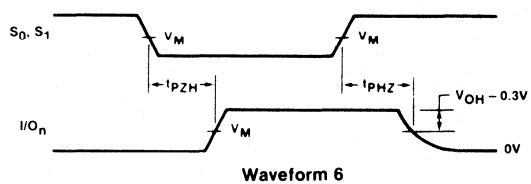
Waveform 4

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 5

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



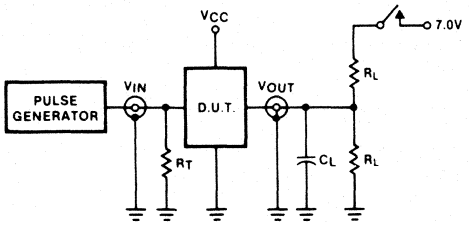
Waveform 6

$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE AND OPEN COLLECTOR (OC) OUTPUTS



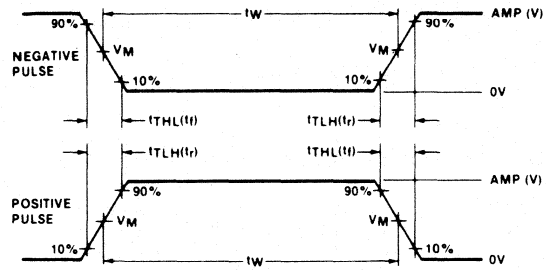
SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
OC	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

LATCH/FLIP-FLOP

FAST 54/74F533, 54/74F534

'F533 Octal Transparent Latch (3-State)
'F534 Octal D Flip-Flop (3-State)

- **8-bit transparent latch — 'F533**
- **8-bit positive edge-triggered register — 'F534**
- **3-State inverting output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F533	6.0ns	41mA
74F534	6.6ns	55mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74F533N • F74F534N	
Plastic SO	N74F533D • N74F534D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
D_0-D_7 ('F533 & 'F534)	Data Inputs	1.0/1.0	20μA/0.6mA
E ('F533)	Latch Enable Input (Active HIGH)	1.0/1.0	20μA/0.6mA
$\overline{OE}$ ('F533 & 'F534)	Output Enable Input (Active LOW)	1.0/1.0	20μA/0.6mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
$\overline{Q}_0$-$\overline{Q}_7$ ('F533 & 'F534)	3-State Outputs	150/33	3mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

DESCRIPTION

The 'F533 is an octal transparent latch coupled to eight 3-State inverting output buffers. The two sections of the device are controlled independently by latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

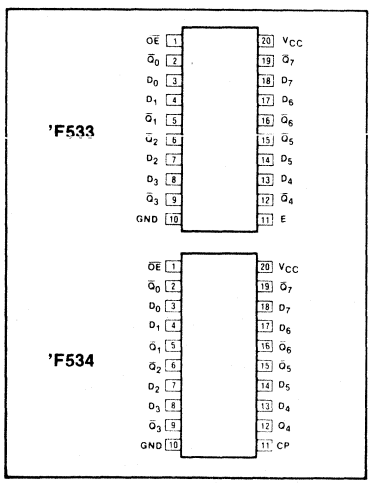
The data on the D inputs are transferred to the latch outputs when the latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition.

The 3-State inverting output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

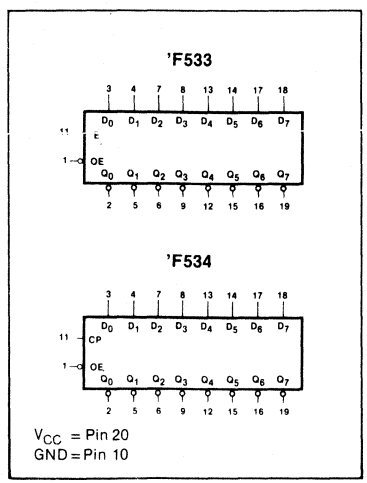
The 'F534 is an 8-bit edge-triggered register coupled to eight 3-State inverting output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition,

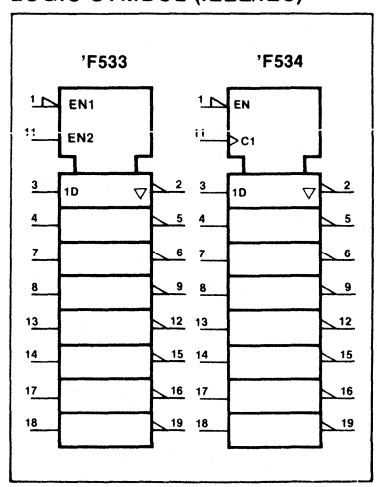
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

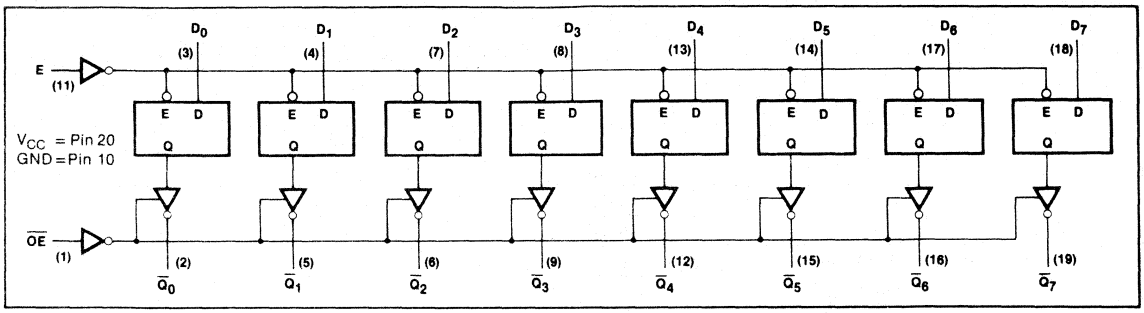


LATCH/FLIP-FLOP — FAST 54/74F533, 54/74F534

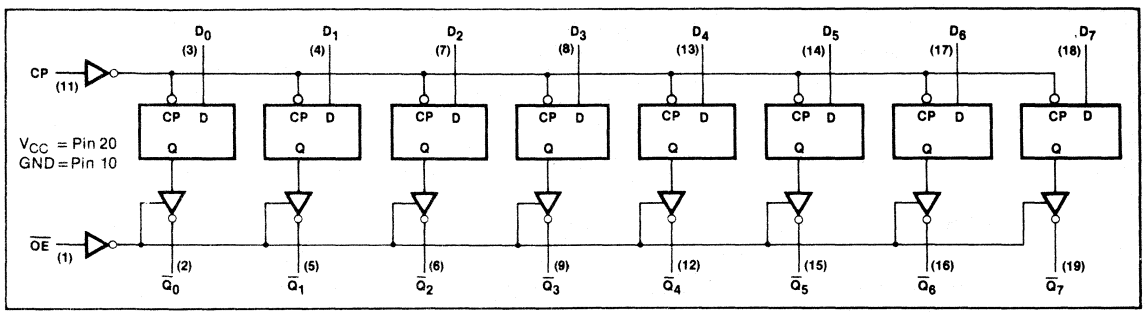
transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause the clocking operation.

The 3-State inverting output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 'F533



LOGIC DIAGRAM, 'F534



5

MODE SELECT — FUNCTION TABLE, 'F533

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		$\overline{Q}_0$-$\overline{Q}_7$
Enable and read register	L	H	X	L	H
	L	H	X	H	L
Latch and read register	L	L	L	L	H
	L	L	H	H	L
Latch register and disable outputs	H	X	X	X	(Z)
	H	X	X	X	(Z)

MODE SELECT — FUNCTION TABLE, 'F534

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		$\overline{Q}_0$-$\overline{Q}_7$
Load and read register	L	↑	l	L	H
	L	↑	h	H	L
Disable outputs	H	X	X	X	(Z)
	H	X	X	X	(Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW $\overline{OE}$ transition
L = LOW voltage level
X = Don't care
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW $\overline{OE}$ transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	48	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−3	mA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F533, 534			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = MAX	Mil	2.4	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 20mA	Mil		0.35	0.5	V
			I_{OL} = 24mA	Com'l		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_{OZH}	Off-stage output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V				2	50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				−2	−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V			−60	−90	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	'F533			41	61	mA
			'F534			55	86	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. 'F533 measure I_{CCZ} with $\overline{OE}$ input at 4.5V, D_n and E inputs at ground and all outputs open.
   'F534 measure I_{CCZ} with $\overline{OE}$ inputs at 4.5V and D_n inputs at ground and all outputs open.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic")

PARAMETER		TEST CONDITIONS		54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 3	'F534	100			60		70		MHz
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 6	'F533	4.0 3.0	6.9 5.2	9.0 7.0	4.0 3.0	12 9.0	4.0 3.0	10 8.0	ns
t_{PLH} t_{PHL}	Propagation delay Latch Enable to output	Waveform 7	'F533	5.0 3.0	8.5 5.6	11 7.0	5.0 3.0	14 9.0	5.0 3.0	13 8.0	ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 3	'F534	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.5 11	4.0 4.0	10 10	ns
t_{PZH} t_{PZL}	Enable time to HIGH level Enable time to LOW level	Waveform 1 Waveform 2	'F533	2.0 2.0	7.7 5.1	10 6.5	2.0 2.0	12.5 9.0	2.0 2.0	11 7.5	ns
t_{PHZ} t_{PLZ}	Disable time from HIGH level Disable time from LOW level	Waveform 1 Waveform 2	'F533	2.0 2.0	4.7 4.1	6.0 5.5	2.0 2.0	8.5 7.5	2.0 2.0	7.0 6.5	ns
t_{PZH} t_{PZL}	Enable time to HIGH level Enable time to LOW level	Waveform 1 Waveform 2	'F534	2.0 2.0	9.0 5.8	11.5 7.5	2.0 2.0	14 10	2.0 2.0	12.5 8.5	ns
t_{PHZ} t_{PLZ}	Disable time from HIGH level Disable time from LOW level	Waveform 1 Waveform 2	'F534	2.0 2.0	5.3 4.3	7.0 5.5	2.0 2.0	8.0 7.5	2.0 2.0	8.0 6.5	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

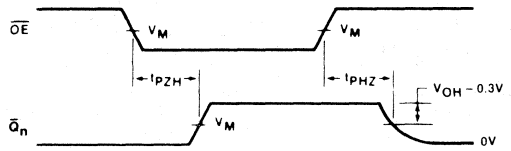
5

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS		54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, Data to Enable, HIGH or LOW	Waveform 5	'F533	2.0 2.0			2.0 2.0		2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, Data to Enable, HIGH or LOW	Waveform 5	'F533	3.0 3.0			3.0 3.0		3.0 3.0		ns
$t_W(H)$	Enable pulse width HIGH	Waveform 5	'F533	6.0			6.0		6.0		ns
$t_s(H)$ $t_s(L)$	Setup time, Data to Clock, HIGH or LOW	Waveform 4	'F534	2.0 2.0			2.5 2.0		2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, Data to Clock, HIGH or LOW	Waveform 4	'F534	2.0 2.0			2.0 2.5		2.0 2.0		ns
$t_W(H)$ $t_W(L)$	Clock pulse width, HIGH or LOW	Waveform 3	'F534	7.0 6.0			7.0 6.0		7.0 6.0		ns

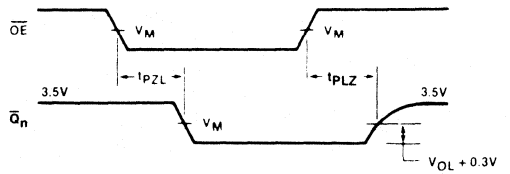
AC WAVEFORMS

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



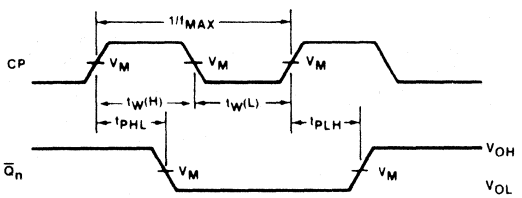
Waveform 1

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



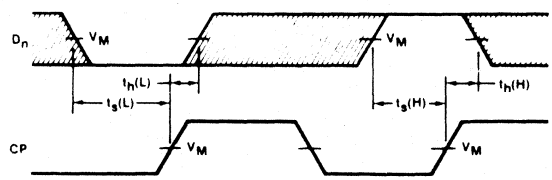
Waveform 2

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



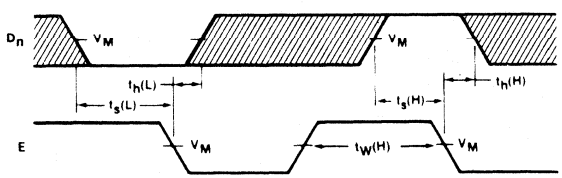
Waveform 3

DATA SETUP AND HOLD TIMES



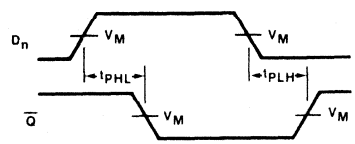
Waveform 4

DATA SETUP AND HOLD TIMES



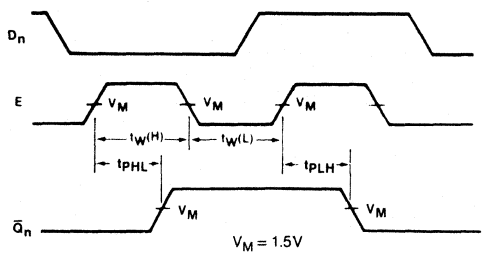
Waveform 5

DATA TO OUTPUT DELAYS



Waveform 6

LATCH ENABLE TO OUTPUT DELAYS

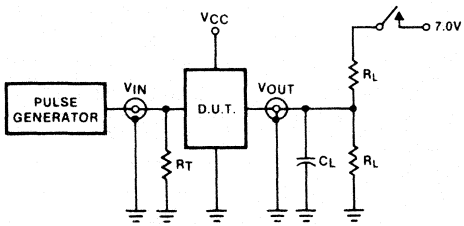


VM = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



SWITCH POSITION

TEST	SWITCH
t_{PLZ} t_{PZL} All other	closed closed open

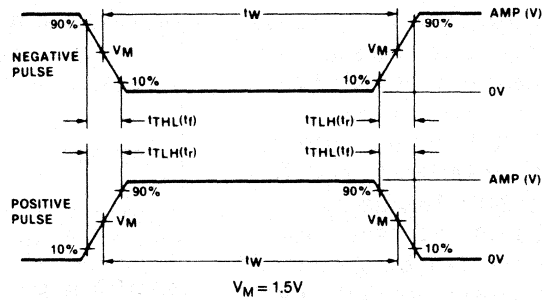
DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

TRANSCEIVERS

FAST 54/74F545

Preview

Octal Bidirectional Transceiver (With 3-State Inputs/Outputs)

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Higher drive than 8304**
- **8-bit bidirectional data flow reduces system package count**
- **3-State inputs/outputs for interfacing with bus-oriented systems**
- **20mA and 64mA bus drive capability on A and B ports, respectively**
- **Transmit/Receive and Output Enable simplify control logic**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F545		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F545N	
Plastic SO	N74F545D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FANOUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/0.033	20μA/20μA
T/$\overline{R}$	Transmit/Receive Input	1.0/0.033	20μA/20μA
A_0-A_7	Side A 3-State Data Inputs or 3-State Outputs	3.50/0.033 150/33	70μA/20μA 3mA/20mA
B_0-B_7	Side B 3-State Data Inputs or 3-State Outputs (Commercial) 3-State Outputs (Military)	3.50/0.033 750/107 600/80	70μA/20μA 15mA/64mA 12mA/48mA

NOTE:
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

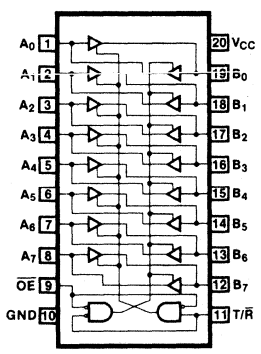
DESCRIPTION

The 'F545 is an 8-bit, 3-state, high-speed transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 20mA bus drive capability on the A ports and 64mA bus drive capability on the B ports.

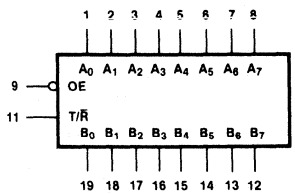
One input, Transmit/Receive (T/$\overline{R}$) determines the direction of logic signals through the bidirectional transceiver. Transmit enables data from A ports to B ports; Receive enables data from B ports to A ports. The Output Enable input disables both A and B ports by placing them in a 3-state condition.

The 'F545 performs the same function as the 'F245 the only difference being package pin assignments.

PIN CONFIGURATION

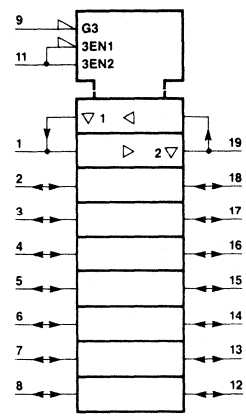


LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

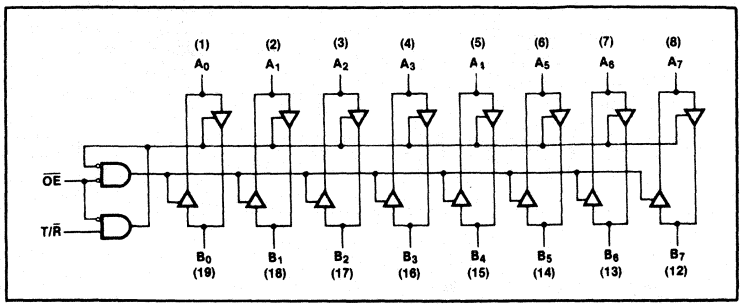
LOGIC SYMBOL (IEEE/IEC)



TRANSCEIVERS — FAST 54/74F545

Preview

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z

H = HIGH voltage level
L = LOW voltage level
X = Immaterial
Z = High impedance

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER			54F	74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	A_0-A_7	40	48	mA
		B_0-B_7	96	128	mA
T_A	Operating free-air temperature range		−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current, A_0-A_7	Mil			−3	mA
		Com'l			−3	mA
I_{OH}	HIGH-level output current, B_0-B_7	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current, A_0-A_7	Mil			20	mA
		Com'l			24	mA
I_{OL}	LOW-level output current, B_0-B_7	Mil			48	mA
		Com'l			64	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

TRANSCEIVERS FAST 54/74F545

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F545 Min	54/74F545 Typ[2]	54/74F545 Max	UNIT
V_{OH}	HIGH-level output voltage, A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3.0mA	Mil	2.4	3.4		V
				Com'l	2.7	3.4		V
V_{OH}	HIGH-level output voltage, B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −12mA	Mil	2.0			V
			I_{OH} = −15mA	Com'l	2.0			V
			I_{OH} = −3.0mA	Mil	2.4	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage, A_0-A_7	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = 24mA				0.35	0.5	V
V_{OL}	LOW-level output voltage, B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MAX	I_{OL} = 48mA	Mil		0.35	0.50	V
			I_{OL} = 64mA	Com'l		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = +7.0V					100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	$\overline{OE}$, T/$\overline{R}$				−20	μA
			A_0-A_7, B_0-B_7				−70	μA
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{OUT} = 2.4V					50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{OUT} = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH				mA
			I_{CCL}	Outputs LOW			192	mA
			I_{CCZ}	Outputs OFF				mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with outputs open.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

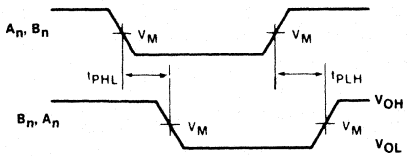
PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	Waveform 1 Waveform 1							6.5 7.0	ns
t_{PZH} t_{PZL}	Output Enable Time	Waveform 2 Waveform 3							8.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time	Waveform 2 Waveform 3							7.5 6.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

Preview

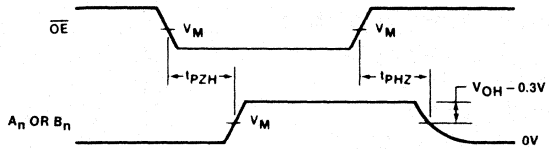
AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 1

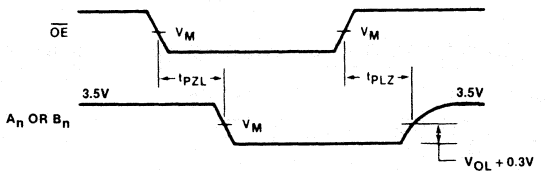
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

$V_M = 1.5V$

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL

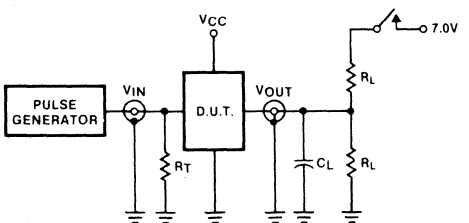


Waveform 3

5

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



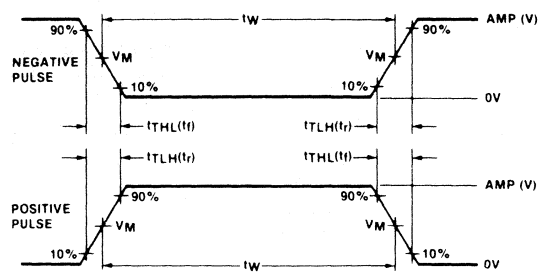
SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DECODER/DEMULTIPLEXER FAST 54/74F547

Preview

Octal Decoder/Demultiplexer with Address Latches and Acknowledge

- **3-to-8 line address decoder**
- **Address storage latches**
- **Multiple enables for address extension**
- **Open-Collector Acknowledge output**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F547		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to + 70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = − 55°C to + 125°C
Plastic DIP	N74F547N	
Plastic SO	N74F547D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

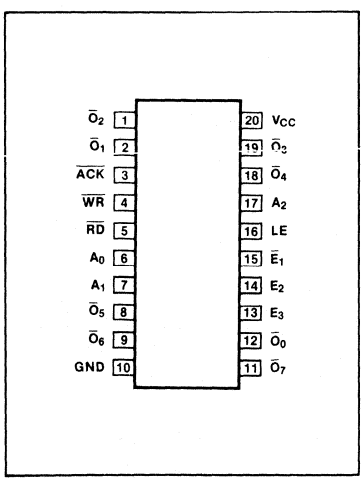
The 'F547 is a 3-to-8 line address decoder with latches for address storage. Designed primarily to simplify multiple-chip selection in a microprocessor system, it contains one active-LOW and two active-HIGH Enables to conserve address space. Also included is an active-LOW Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

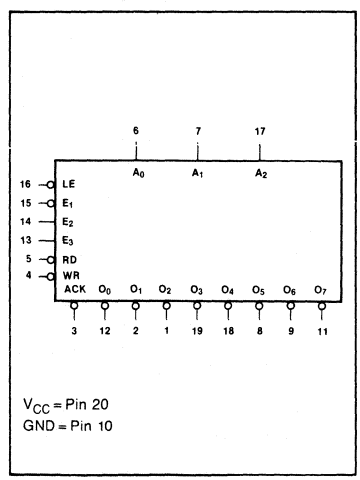
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A_0-A_2	Output Select Address Input	1.0/1.0	20μA/0.6mA
$\overline{E}_1$	Chip Enable Input (Active LOW)	1.0/1.0	20μA/0.6mA
E_2, E_3	Chip Enable Inputs	1.0/1.0	20μA/0.6mA
LE	Latch Enable Input	1.0/1.0	20μA/0.6mA
$\overline{RD}$	Read Acknowledge Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{WR}$	Write Acknowledge Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{O}_0$-$\overline{O}_7$	Decoder Outputs (Active LOW)	50/33.3	1mA/20mA
$\overline{ACK}$	Open-Collector Acknowledge Output (Active LOW)	OC*/33.3	OC*/20mA

One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.
*OC = Open-Collector.

PIN CONFIGURATION



LOGIC SYMBOL



DECODER/DEMULTIPLEXER FAST 54/74F548

Preview

Octal Decoder/Demultiplexer with Acknowledge

- 3-to-8 line address decoder
- Multiple enables for address extension
- Open-Collector Acknowledge output
- Active-LOW Decoder outputs

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F548		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F548N	
Plastic SO	N74F548D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F548 is a 3-to-8 line address decoder with four Enable inputs. Two of the Enables are active-LOW and two are active-HIGH for maximum addressing versatility. Also provided is an active-LOW Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

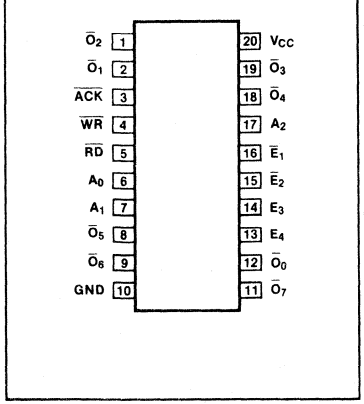
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A_0-A_2	Output Select Address Inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_1$, $\overline{E}_2$	Chip Enable Inputs (Active LOW)	1.0/1.0	20μA/0.6mA
E_3, E_4	Chip Enable Inputs	1.0/1.0	20μA/0.6mA
$\overline{RD}$	Read Acknowledge Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{WR}$	Write Acknowledge Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{O}_0$-$\overline{O}_7$	Decoder Outputs (Active LOW)	50/33	1mA/20mA
ACK	Open-Collector Acknowledge Output (Active LOW)	OC*/33	OC*/20mA

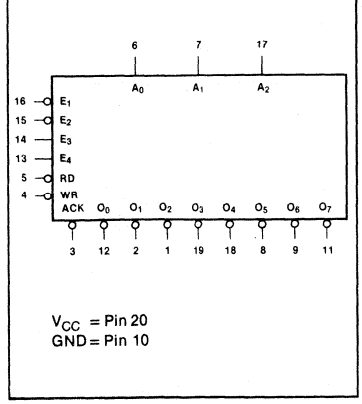
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.
*OC = Open-Collector.

5

PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

COUNTER — FAST 54/74F579

Preview

8-Bit Bidirectional Binary Counter (3-State)

- **Multiplexed 3-state I/O ports**
- **Built-in lookahead carry capability**
- **Count frequency 100MHz typ**
- **Supply current 75mA typ**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F579	100MHz	70mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to + 70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = − 55°C to + 125°C
Plastic DIP	N74F579N	
Plastic SO	N74F579D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

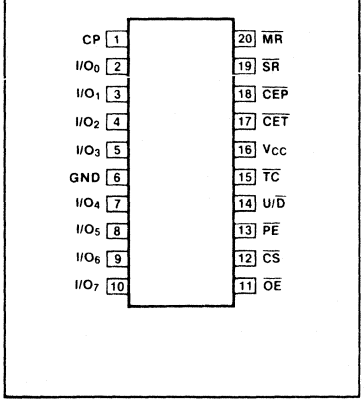
The 'F579 is a fully synchronous 8-stage up/down counter with multiplexed 3-state I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

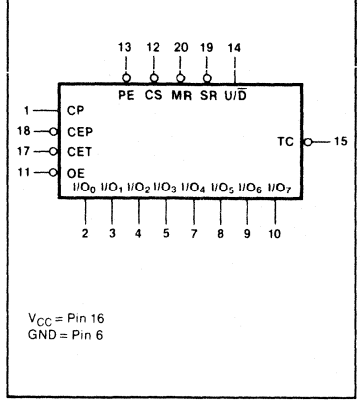
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
I/O_0–I/O_7	Data Inputs	1.0/1.0	20μA/0.6mA
	Data Outputs	150/33	3mA/20mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0	20μA/0.6mA
U/$\overline{D}$	Up-Down Count Control Input	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{SR}$	Synchronous Reset Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CS}$	Chip Select Input Active (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/1.0	20μA/0.6mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal Count Output (Active LOW)	150/33	3mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

COUNTER FAST 54/74F579

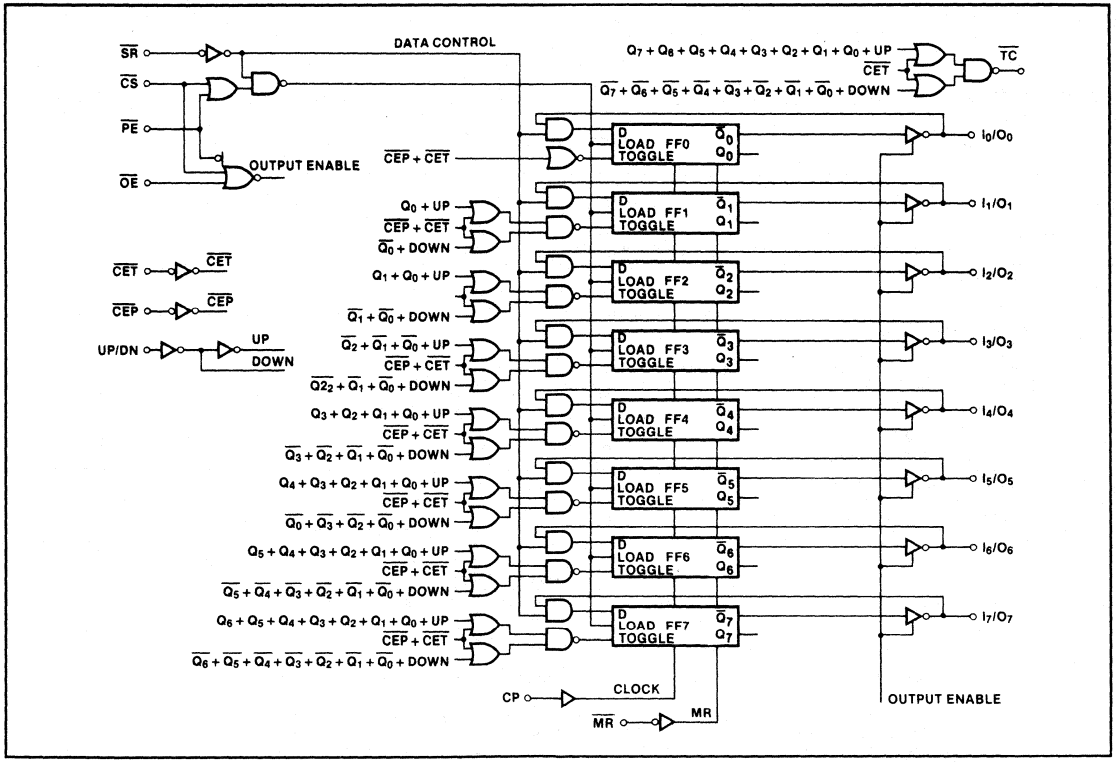
Preview

FUNCTION TABLE

$\overline{MR}$	$\overline{SR}$	$\overline{CS}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	$\overline{OE}$	CP	FUNCTION
X	X	H	X	X	X	X	X	X	I/Oa to I/Oh in High-Z ($\overline{PE}$ disabled)
X	X	L	H	X	X	X	H	X	I/Oa to I/Oh in High-Z
X	X	L	H	X	X	X	L	X	Flip-flop outputs appear on I/O lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)	H	X	X	X	X	↑	Hold
H	H	(not LL)	X	H	X	X	X	↑	Hold ($\overline{TC}$ held high)
H	H	(not LL)	L	L	H	X	X	↑	Count up
H	H	(not LL)	L	L	L	X	X	↑	Count down

H = HIGH voltage level
L = LOW voltage level
X = Don't Care
↑ = LOW-to-HIGH clock transition
not LL means $\overline{CS}$ and $\overline{PE}$ should never both be LOW voltage level at the same time.

LOGIC DIAGRAM



5

Preview

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−3	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F579			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.4			V
			Com'l	2.7			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage (negative)	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V			2	50	μA
I_{OZL}	Off-state output current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−50	μA
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			0.75	1.0	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			10	20	μA
i_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.1	−20	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		50	70	mA
			I_{CCL} Outputs LOW		80	100	mA
			I_{CCZ} Outputs Disabled		80	100	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

COUNTER — FAST 54/74F579

Preview

AC ELECTRICAL CHARACTERISTICS

(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Waveform 1	80	100		60		70		MHz
t_{PLH} / t_{PHL} CP to I/O_n	Waveform 1	3.0 4.5		10.0 10.0	2.5 4.0	12.0 12.0	2.5 4.0	11.0 11.0	ns
t_{PLH} / t_{PHL} U/$\overline{D}$ to $\overline{TC}$, $\overline{CET}$ to $\overline{TC}$, CP to $\overline{TC}$	Waveform 1	6.0 5.0		15.0 15.0	5.0 4.0	17.0 17.0	5.0 4.0	16.0 16.0	ns
t_{PLH} / t_{PHL} U/$\overline{D}$ to $\overline{TC}$, $\overline{CET}$ to $\overline{TC}$, CP to $\overline{TC}$	Waveform 1	6.0 5.0		15.0 15.0	5.0 4.0	17.0 17.0	5.0 4.0	16.0 16.0	ns
t_{PZH} / t_{PZL} Output disable time	Waveform 3 Waveform 4	12 12		20 20	10 10	24 24	10 10	22 22	ns
t_{PHZ} / t_{PLZ} Output enable time	Waveform 3 Waveform 4	12 12		20 20	10 10	24 24	10 10	22 22	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

5

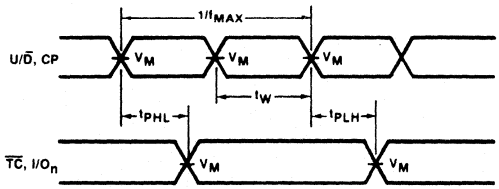
AC SETUP REQUIREMENTS

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_s (H) / t_s (L) Data to CP	Waveform 2	5.0 5.0					5.0 5.0		ns
t_h (H) / t_h (L) Data to CP	Waveform 2	0 0					0 0		ns
t_s (H) / t_s (L) $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	Waveform 2	12 12					12 12		ns
t_h (H) / t_h (L) $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	Waveform 2	0 0					0 0		ns
t_s (H) / t_s (L) $\overline{CET}$ or $\overline{CEP}$ TO CP	Waveform 2	10 10					10 10		ns
t_h (H) / t_h (L) $\overline{CET}$ or $\overline{CEP}$ to CP	Waveform 2	0 0					0 0		ns
t_w Clock pulse width	Waveform 1	5					6		ns

Preview

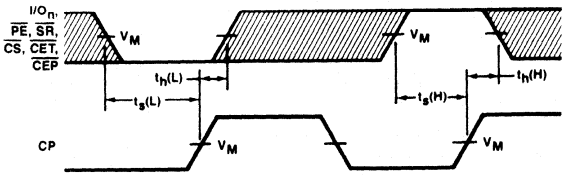
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



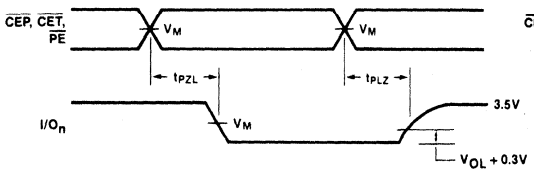
Waveform 1

DATA SETUP AND HOLD TIMES



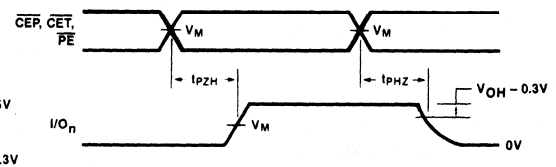
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL

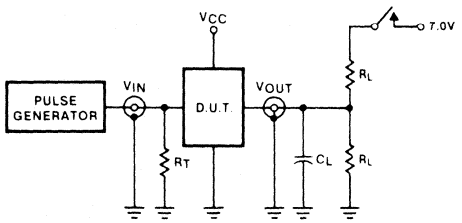


Waveform 4

$V_M = 1.5V$

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



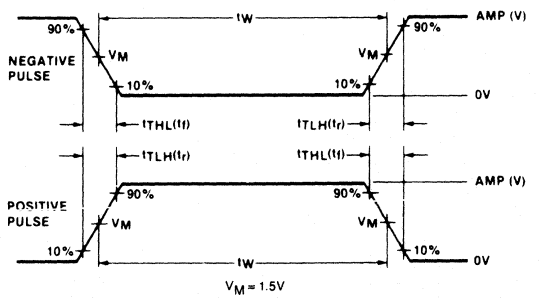
SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Preview

Octal Bidirectional Transceiver With IEEE-488 Termination Resistors (3-State Inputs and Outputs)

- **High impedance NPN base input for reduced loading (20μA in HIGH and LOW states)**
- **Non-inverting buffers**
- **Bidirectional data path**
- **B outputs sink 48mA, source 15mA**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F588		128mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F588N	
Plastic SO	N74F588D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F588 contains eight non-inverting bidirectional buffers with 3-State outputs and is intended for bus-oriented applications. The B ports have termination resistors as specified in the IEEE-488 specifications. Current sinking capability is 20mA at the A ports and 48mA at the B ports. The Transmit/Receive (T/$\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a high-impedance condition.

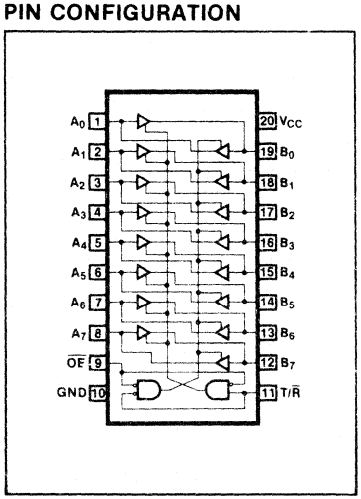
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{OE}$	Output Enable Input (Active LOW)	2.0/0.033	40μA/20μA
T/$\overline{R}$	Transmit/Receive Control Input	1.0/0.033	20μA/20μA
A_0–A_7	A Port Inputs or 3-State Outputs	3.5/0.033 150/33	70μA/20μA 3mA/20mA
B_0–B_7	B Port Inputs or 3-State Outputs	*T/0.033 260/80	*T/20μA 5.2mA/48mA

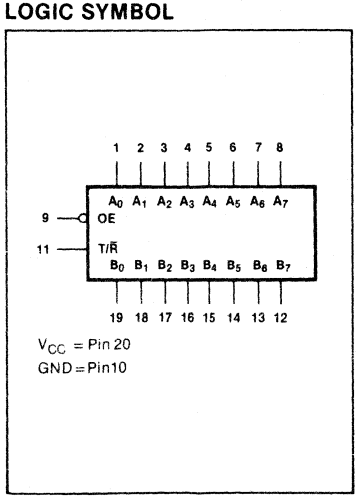
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.
*T = Resistance Termination per IEEE-488 Standard.

5

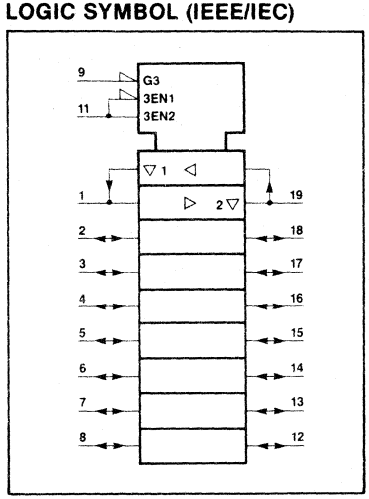
PIN CONFIGURATION



LOGIC SYMBOL

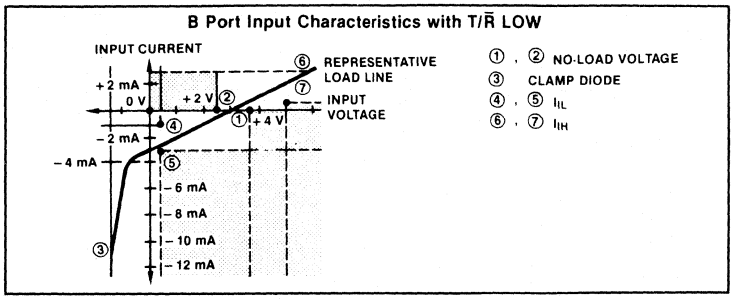


LOGIC SYMBOL (IEEE/IEC)



TRANSCEIVER FAST 54/74F588

Preview

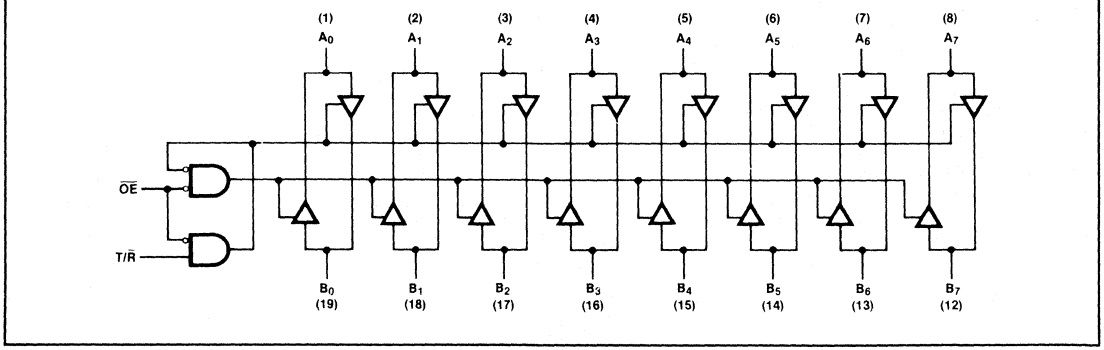


TRUTH TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Impedance

H = HIGH voltage level
L = LOW voltage level
X = Don't care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage		− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage		− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current		− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state		− 0.5 to + 5.5	− 0.5 to + 5.5	V
I_{OUT}	Current applied to output in LOW output state	A_0–A_7	48	48	mA
		B_0–B_7	128	128	mA
T_A	Operating free-air temperature range		− 55 to + 125	0 to 70	°C

TRANSCEIVER FAST 54/74F588

Preview

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current, A_0-A_7	Mil			– 3	mA
		Com'l			– 3	mA
I_{OH}	HIGH-level output current, B_0-B_7	Mil			– 12	mA
		Com'l			– 15	mA
I_{OL}	LOW-level output current, A_0-A_7	Mil			20	mA
		Com'l			24	mA
I_{OL}	LOW-level output current, B_0-B_7	Mil			48	mA
		Com'l			64	mA
T_A	Operating free-air temperature	Mil	– 55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

5

PARAMETER		TEST CONDITIONS[1]			54/74F588			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage, A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = – 3.0mA	Mil	2.4			V
				Com'l	2.7			V
V_{OH}	HIGH-level output voltage, B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = – 12mA	Mil	2.0			V
			I_{OH} = – 15mA	Com'l	2.0			V
			I_{OH} = – 3.0mA	Mil	2.4			V
				Com'l	2.7			V
V_{OL}	LOW-level output voltage, A_0-A_7	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = 24mA				0.35	0.5	V
V_{OL}	LOW-level output voltage, B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MAX	I_{OL} = 48mA	Mil		0.35	0.5	V
			I_{OL} = 64mA	Com'l		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 0.73	– 1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = + 7.0V					100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	A_0-A_7				– 70	μA
			$\overline{OE}$				– 40	μA
			T/$\overline{R}$				– 20	μA
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{OUT} = 2.4V					50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{OUT} = 0.5V					– 50	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 100		– 225	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH				mA
			I_{CCL}	Outputs LOW			192	mA
			I_{CCZ}	Outputs OFF				mA

TRANSCEIVER FAST 54/74F588

Preview

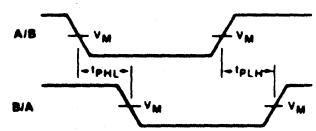
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A	Waveform 1 Waveform 1							6.5 7.0	ns
t_{PZH} t_{PZL}	Output Enable Time T/$\overline{R}$ or $\overline{OE}$ to A or B	Waveform 2 Waveform 3							8.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time T/$\overline{R}$ or $\overline{OE}$ to A or B	Waveform 2 Waveform 3							7.5 6.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

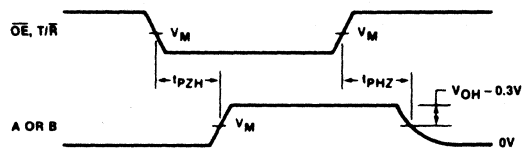
AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 1

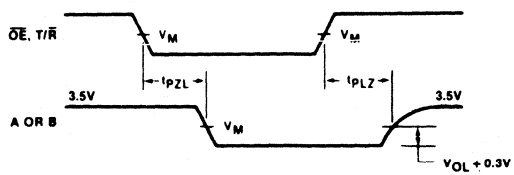
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

$V_M = 1.5V$

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL

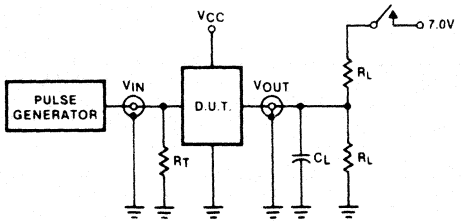


Waveform 3

Preview

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

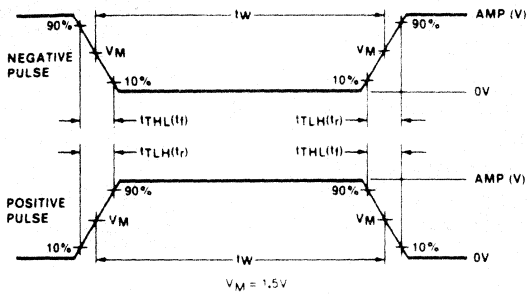
DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

8-BIT SHIFT REGISTER

FAST 54/74F595

Preview

8-Bit Shift Register with Output Latches (3-State)

- High impedance NPN base input for reduced loading (20μA in HIGH and LOW states)
- 8-bit serial-in, parallel-out shift register with storage
- 3-State outputs
- Shift register has direct clear
- Guaranteed shift frequency — DC to 100MHz

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F595		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F595N	
Plastic SO	N74F595D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-State outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct overriding clear, Serial input and Serial output pins for cascading.

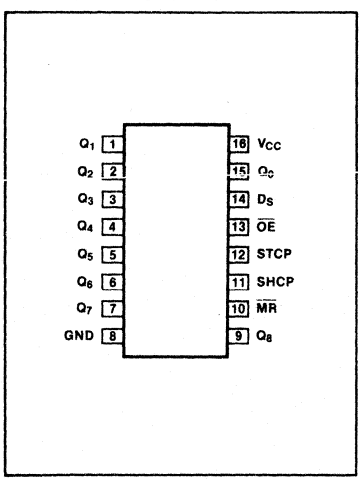
Both the shift register and storage register clocks are positive edge-triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

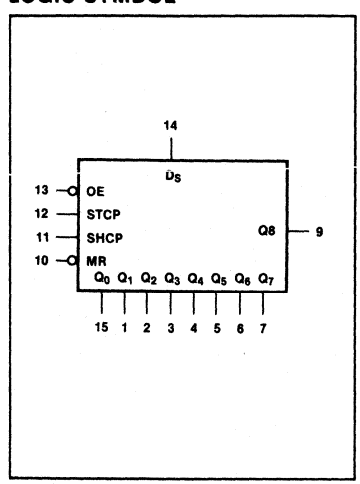
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
SHCP	Shift Register Clock Pulse Input	1/0.033	20μA/20μA
STCP	Storage Register Clock Pulse Input	1/0.033	20μA/20μA
$\overline{MR}$	Master Reset Input	1/0.033	20μA/20μA
D_S	Serial Data Input	1/0.033	20μA/20μA
$\overline{OE}$	Output Enable Input	1/0.033	20μA/20μA
Q_0–Q_7	Parallel Data Output	150/33	3.0mA/20mA
Q_8	Serial Data Output	50/33	1.0mA/20mA

One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

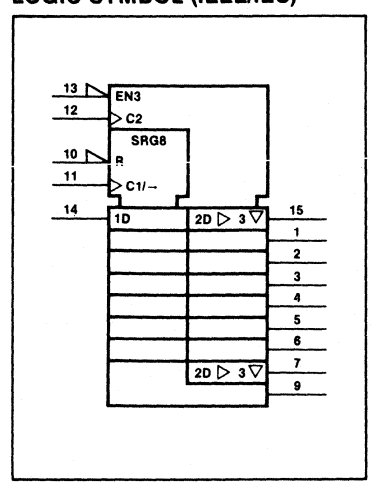
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



8-BIT SHIFT REGISTER FAST 54/74F597, 54/74F598

Preview

8-Bit Shift Registers with Input Latches (3-State)

- 8-bit Parallel Storage Register inputs ('F597)
- Parallel 3-State I/O, Storage Register inputs, Shift Register outputs ('F598)
- Shift register has direct overriding load and clear
- Guaranteed shift frequency — DC to 100MHz

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F597		
74F598		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F597N • N74F598N	
Plastic SO	N74F597D • N74F598D	

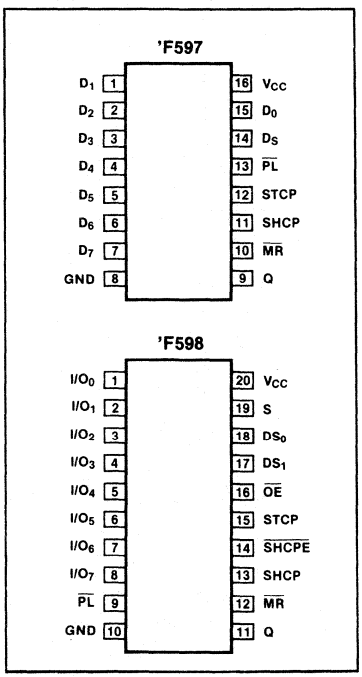
DESCRIPTION

The 'F597 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive edge-triggered clocks. The shift register also has direct load (from storage) and clear inputs.

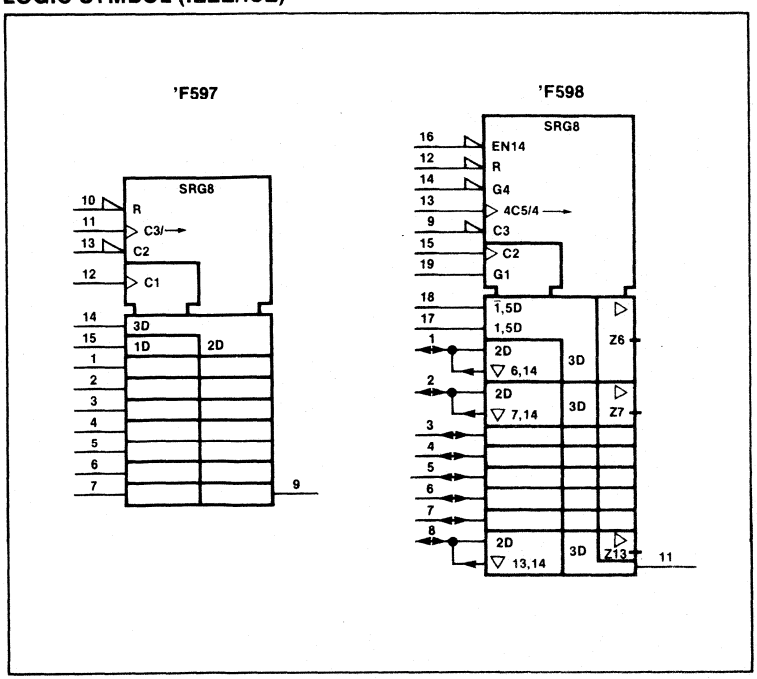
The 'F598 comes in a 20-pin package and has all the features of the 'F597, plus 3-State I/O ports that provide Parallel Shift Register outputs and also has Multiplexed Serial Data inputs.

5

PIN CONFIGURATION



LOGIC SYMBOL (IEEE/ICE)



Preliminary

'F604 — Dual Octal Register (3-State)
'F605 — Dual Octal Register (Open Collector)

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Stores 16-bit-wide Data inputs, multiplexed 8-bit outputs**
- **3-State outputs ('F604)**
- **Open-Collector Outputs ('F605)**
- **Propagation delay 10ns typical**
- **Power supply current 85mA typical**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F604	10ns	85mA
74F605	10ns	85mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74F604N • N74F605N	
Plastic SO	N74F604D • N74F605D	
Ceramic DIP		
Ceramic LLCC		

NOTE SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

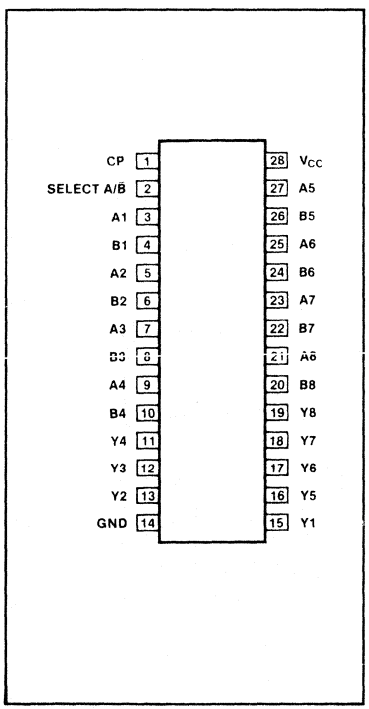
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A_1-A_8	Inputs A	1.0/0.033	20μA/20μA
B_1-B_8	Inputs B	1.0/0.033	20μA/20μA
Select A/$\overline{B}$	Select Inputs	1.0/0.033	20μA/20μA
CP	Clock Pulse Input (Active Rising Edge)	1.0/0.033	20μA/20μA
Y_1-Y_8	Outputs	150/40	3.0mA/24mA

NOTE One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

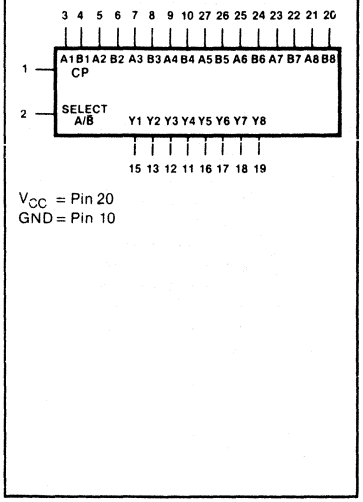
DESCRIPTION

The 'F604 contains 16 D-type edge-triggered data inputs. Organized as 8-bit A and B registers, the flip-flop outputs are connected by pairs to eight 2-input multiplexers. A Select (SA/$\overline{B}$) input determines whether the A or B register contents are multiplexed to the eight

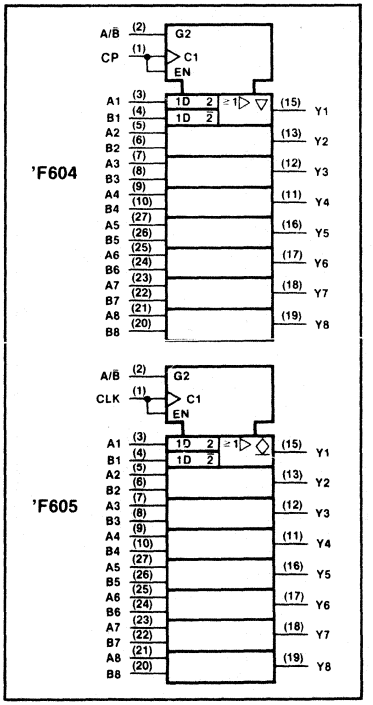
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



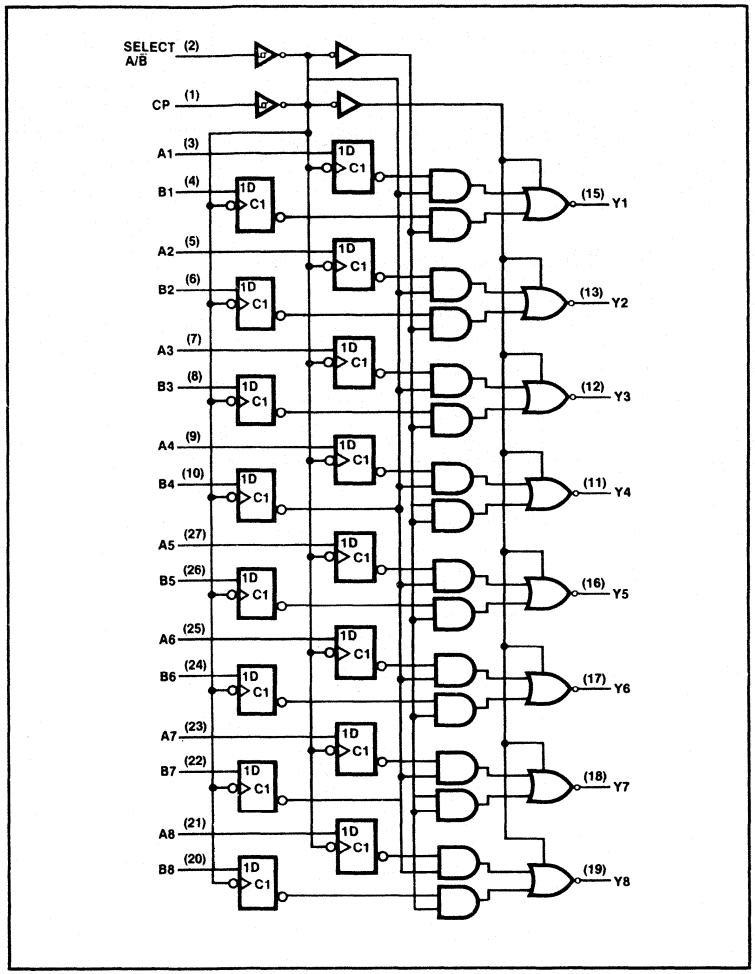
Preliminary

3-state outputs. Data entered from the I_0 inputs are selected when SA/$\overline{B}$ is LOW: data from the I_1 inputs are selected when SA/$\overline{B}$ is HIGH. Data enters the flip-flops on the rising edge of the Clock (CP) input, which also controls the 3-state outputs. The outputs are enabled when CP is HIGH and disabled when CP is LOW.

The 'F605 contains 16 D-type edge-triggered flip-flops with common clock and individual data inputs. Organized as 8-bit A and B registers, the flip-flop outputs are connected by pairs to eight 2-input multiplexers. A Select (SA/$\overline{B}$) inputs determines whether the A or B register contents are multiplexed to the eight open-collector outputs. Data entered from the I_0 inputs are selected when SA/$\overline{B}$ is LOW; data from the I_1 inputs are selected when SA/$\overline{B}$ is HIGH. Data enters the flip-flops on the rising edge of the Clock (CP) input, which also controls the open-collector outputs. The outputs are enabled when CP is HIGH and disabled when CP is LOW.

These functions are well suited for receiving 16-bit simultaneous data and transmitting it as two sequential 8-bit words.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS
A1-A8	B1-B8	SELECT A/$\overline{B}$	CP	Y1-Y8
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	Z or Off
X	X	L	H	B register stored data
X	X	H	H	A register stored data

H = HIGH level (steady state)
L = LOW level (steady state)
Off = H if pull-up resistor is connected to Open-Collector output
X = Don't care
Z = High-impedance state
↑ = Transition from LOW-to-HIGH level

5

Preliminary

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	'F605			−1	mA
		'F604			−3	mA
I_{OL}	LOW-level output current				24	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F604			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = −3mA	Mil	2.4	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 20mA	Mil		0.3	0.5	V
			I_{OL} = 24mA	Com'l		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_{OZH}	Off-stage output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V				2	50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				−2	−50	μA
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V					−20	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}					mA
			I_{CCL}					mA
			I_{CCZ}					mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Preliminary

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F605 Min	54/74F605 Typ[2]	54/74F605 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			– 0.73	– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				– 20	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		– 60	– 80	– 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		75	100	mA
			I_{CCL} Outputs LOW		85	100	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH}: V_{IN} = GND; I_{CCL}: V_{IN} = Open.

AC CHARACTERISTICS (When measured in accordance with the procedures outlines in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F604 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	54F604 T_A, V_{CC} = Mil, C_L = 50pF, R_L = 500Ω Min	Max	74F604 T_A, V_{CC} = Com'l, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	100			70		80		MHz
t_{PLH} t_{PHL}	Select A/B (Data: A = H, B = L)	Waveform 2							11 10	ns
t_{PLH} t_{PHL}	Select A/B (Data: A = L, B = H)	Waveform 3							11 10	ns
t_{PZH} t_{PZL}	Enable time to HIGH Enable time to LOW	Waveforms 4 & 5							8 12.5	ns
t_{PHZ} t_{PLZ}	Disable time from HIGH Disable time from LOW	Waveforms 4 & 5							8 12.5	ns

NOTE Subtract 0.2ns from minimum values for SO package.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifing FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F605 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	54F605 T_A, V_{CC} = Mil, C_L = 50pF, R_L = 500Ω Min	Max	74F605 T_A, V_{CC} = Com'l, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	100							MHz
t_{PLH} t_{PHL}	Select A/$\overline{B}$ (Data: A = H, B = L)	Waveform 2							15 10	ns
t_{PLH} t_{PHL}	Select A/$\overline{B}$ (Data: A = L, B = H)	Waveform 3							15 10	ns
t_{PLH} t_{PHL}	CP	Waveform 1							15 12.5	ns

NOTE Subtract 0.2ns from minimum values for SO package.

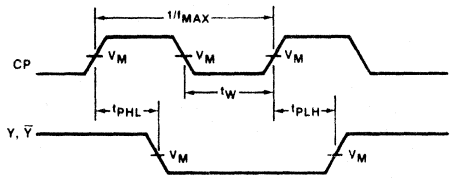
Preliminary

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F604/605 $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F604/605 T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F604/605 T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_w	Width of Clock Pulse	Waveform 1	5			5		5		ns
t_s	Set-Up Time	Waveform 6	3			3		3		ns
t_h	Hold Time	Waveform 6	0			0		0		ns

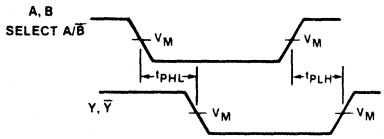
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



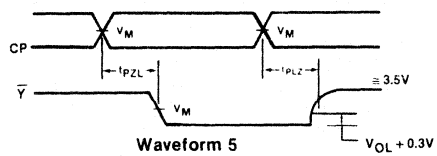
Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



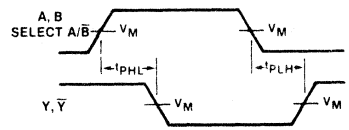
Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



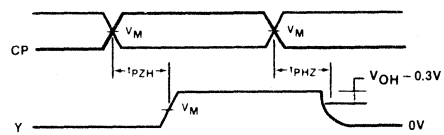
Waveform 5

WAVEFORM FOR INVERTING OUTPUTS



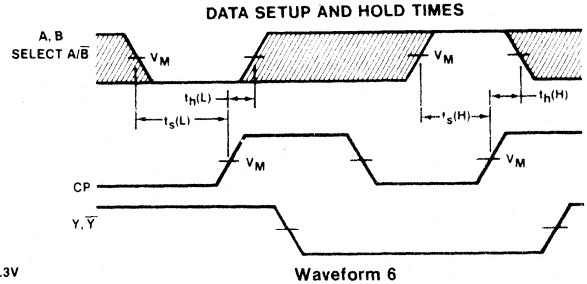
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 4

DATA SETUP AND HOLD TIMES



Waveform 6

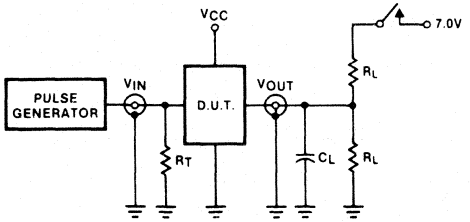
$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

Preliminary

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS 'F604



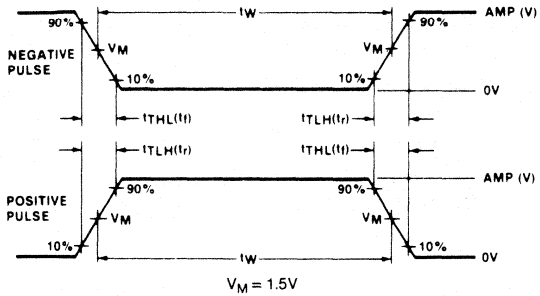
SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



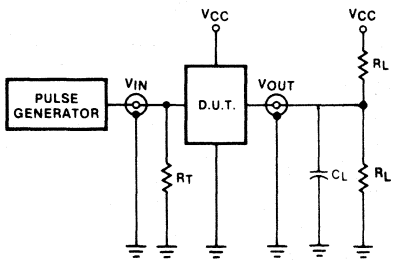
V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

TEST CIRCUITS AND WAVEFORMS

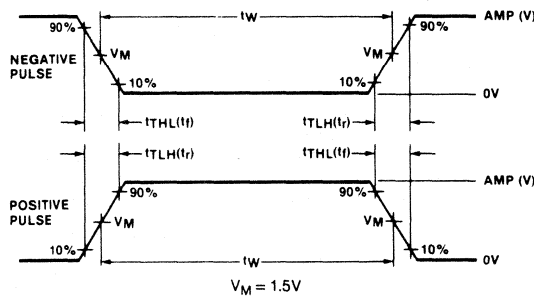
TEST CIRCUIT FOR OPEN COLLECTOR OUTPUTS, 'F605



DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

TRANSCEIVERS 54/74F620, F623

Preliminary

'F620 Octal Bus Transceiver, Inverting (3-State)
'F623 Octal Bus Transceiver, Non-Inverting (3-State)

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Octal bidirectional bus interface**
- **3-State buffer outputs sink 64mA**
  - **— 'F620, inverting**
  - **— 'F623, non-inverting**
- **15mA source current**

Type	Typical Propagation Delay	Typical Supply Current (Total)
74F620		mA
74F623	ns	mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F620N • N74F623N	
Plastic SO	N74F620D • N74F623D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F623 is an octal transceiver featuring non-inverting 3-State bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics. The 'F620 is an inverting version of the 'F623.

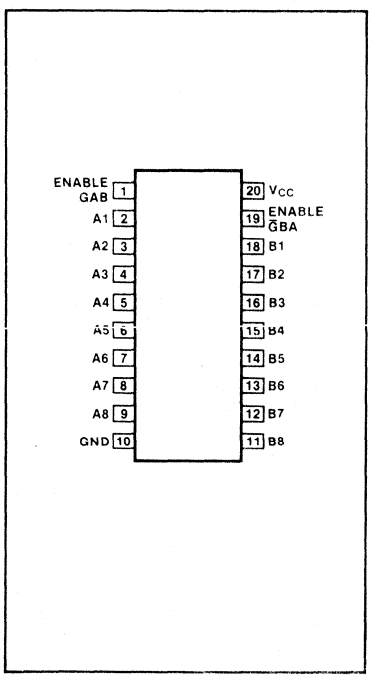
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

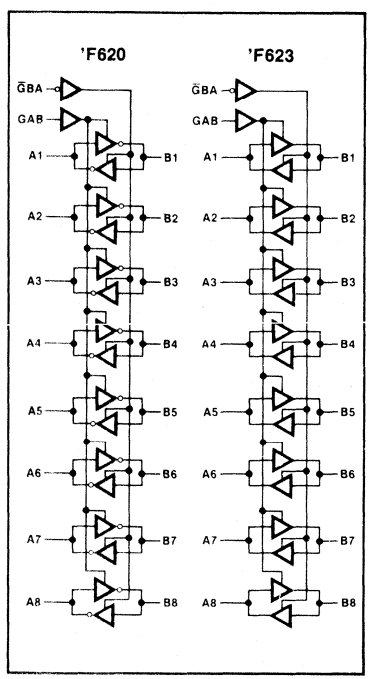
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{G}BA$, GAB	Enable Inputs	1.0/.033	20μA/20μA
A_1-A_8, B_1-B_8	3-State Inputs or 3-State Outputs	1.0/.033 50/1000	20μA/20μA 1.0mA/20mA

NOTE: One (1.0) FAST unit load (U.L.) is defined as 20μA in the HIGH state and 0.6mA in the LOW state.

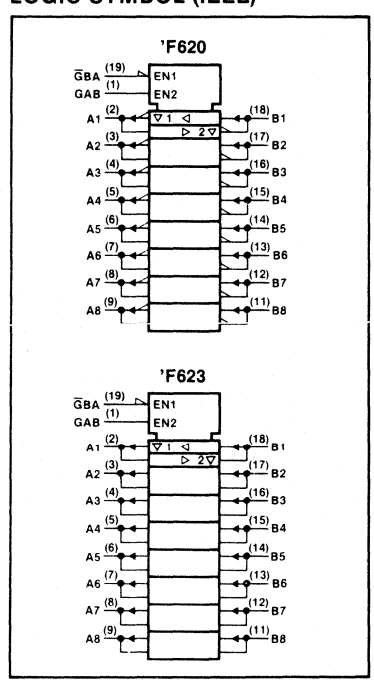
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE)



TRANSCEIVERS 54/74F620, F623

Preliminary

FUNCTION TABLE

ENABLE	INPUTS	OPERATION	
$\overline{G}BA$	GAB	'F620	'F623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	(Z)	(Z)
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

H = HIGH voltage level
L = LOW voltage level
(Z) = HIGH impedance (off) state

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{G}$BA and GAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'F620 and 'F623 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER			54F	74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	A_1–A_8	48	48	mA
		B_1–B_8	128	128	mA
T_A	Operating free-air temperature range		−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current, A_1–A_8	Mil			−3	mA
		Com'l			−3	mA
I_{OH}	HIGH-level output current, B_1–B_8	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current, A_1–A_8	Mil			20	mA
		Com'l			24	mA
I_{OL}	LOW-level output current, B_1–B_8	Mil			48	mA
		Com'l			64	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

5

TRANSCEIVERS 54/74F620, F623

Preliminary

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F620, 622			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage, A_1-A_8	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3.0mA	Mil	2.4			V
				Com'l	2.7			V
V_{OH}	HIGH-level output voltage, B_1-B_8	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -12mA	Mil	2.0			V
			I_{OH} = -15mA	Com'l	2.0			V
			I_{OH} = -3.0mA	Mil	2.4			V
				Com'l	2.7			V
V_{OL}	LOW-level output voltage, A_1-A_8	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = 24mA					0.5	V
V_{OL}	LOW-level output voltage, B_1-B_8	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MAX	I_{OL} = 48mA	Mil			0.5	V
			I_{OL} = 64mA	Com'l			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = +7.0V					100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V					20	μA
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{OUT} = 2.4V					50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{OUT} = 0.5V					-50	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH				mA
			I_{CCL}	Outputs LOW			143	mA
			I_{CCZ}	Outputs OFF				

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with outputs open.

Preliminary

AC CHARACTERISTICS

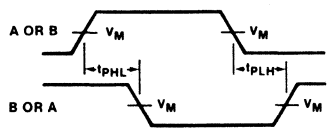
PARAMETER		TEST CONDITIONS	54F/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			54F T_A, V_{CC} = Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} = Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A input to B output	Waveform 1, '620 Waveform 2, '623							6.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay B input to A output	Waveform 1, '620 Waveform 2, '623							6.5 7.0	ns
t_{PZH}	Enable to HIGH $\overline{G}$BA input to A output	Waveform 3							8.0	ns
t_{PZH}	Enable to HIGH GAB input to B output	Waveform 3							8.0	ns
t_{PZL}	Enable to LOW $\overline{G}$BA input to A output	Waveform 4							11.0	ns
t_{PZL}	Enable to LOW GAB input to B output	Waveform 4							11.0	ns
t_{PHZ}	Disable from HIGH $\overline{G}$BA input to A output	Waveform 3							7.5	ns
t_{PHZ}	Disable from HIGH GAB input to B output	Waveform 3							7.5	ns
t_{PLZ}	Disable from LOW $\overline{G}$BA input to A output	Waveform 4							6.0	ns
t_{PLZ}	Disable from LOW GAB input to B output	Waveform 4							6.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

5

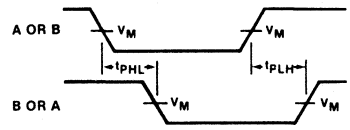
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



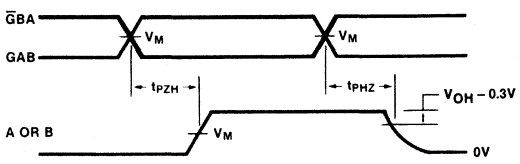
Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



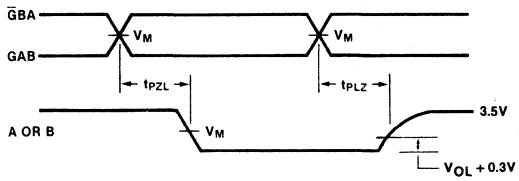
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



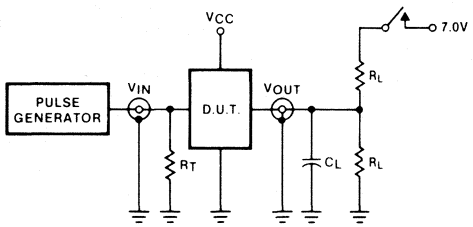
Waveform 4

$V_M = 1.5V$

Preliminary

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



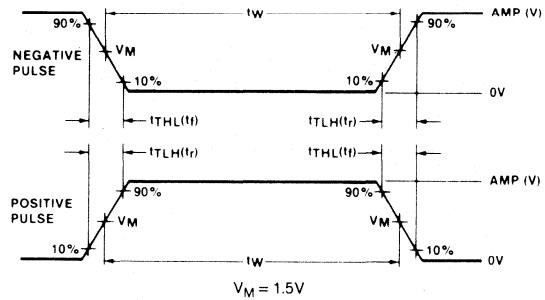
SWITCH POSITION

TEST	SWITCH
t_{PLZ} t_{PZL} All other	closed closed open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Preliminary

'F621 — Octal Bus Transceiver, Non-Inverting (Open Collector)
'F622 — Octal Bus Transceiver, Inverting (Open Collector)

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Octal bidirectional bus interface**
- **Open-Collector outputs sink 64mA**
  - **— 'F621, non-inverting**
  - **— 'F622, inverting**
- **15mA source current**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F621		
74F622		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F621N • N74F622N	
Plastic SO	N74F621D • N74F622D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F621 is an octal transceiver featuring non-inverting Open-Collector bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics. The 'F622 is an inverting version of the 'F621.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

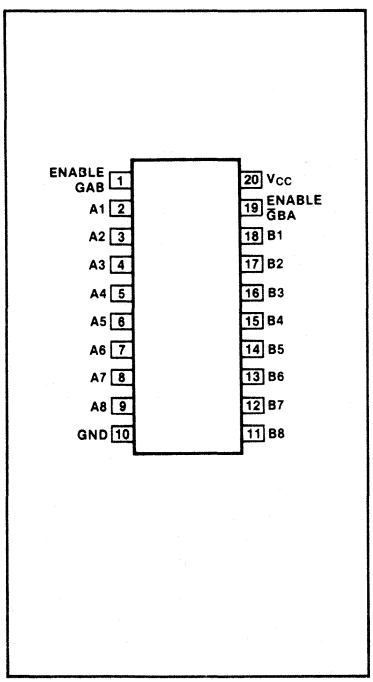
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{G}$BA, GAB	Enable Inputs	1.0/0.033	20μA/20μA
A_1-A_8, B_1-B_8	3-State Inputs	1.0/0.033	20μA/20μA
A_1-A_8	3-State Outputs	150/40	3.0mA/24mA
B_1-B_8	3-State Outputs	150/106.7	3.0mA/64mA

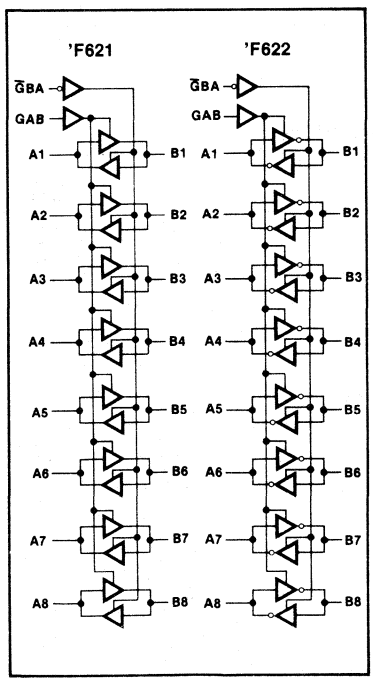
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

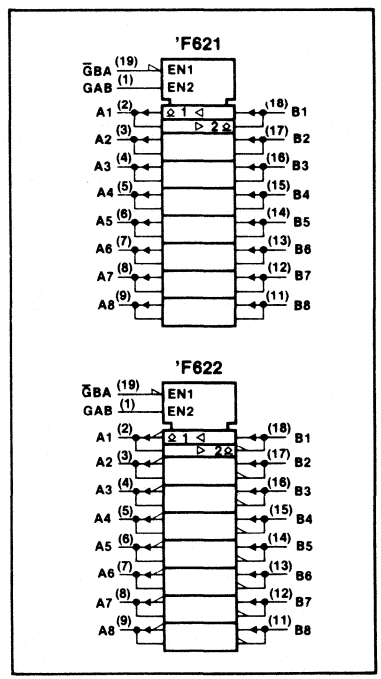
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE)



TRANSCEIVERS 54/74F621, F622

Preliminary

FUNCTION TABLE

ENABLE	INPUTS	OPERATION	
$\overline{G}BA$	GAB	'F621	'F622
L	L	B data to A bus	$\overline{B}$ data to A bus
H	H	A data to B bus	$\overline{A}$ data to B bus
H	L	(Z)	(Z)
L	H	B data to A bus, A data to B bus	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus

H = HIGH voltage level
L = LOW voltage level
(Z) = HIGH impedance (off) state

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{G}$BA and GAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'F621 and 'F622 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER			54F	74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	A_1–A_8	40	48	mA
		B_1–B_8	96	128	mA
T_A	Operating free-air temperature range		−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current, A_1–A_8	Mil			−3	mA
		Com'l			−3	mA
I_{OH}	HIGH-level output current, B_1–B_8	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current, A_1–A_8	Mil			20	mA
		Com'l			24	mA
I_{OL}	LOW-level output current, B_1–B_8	Mil			48	mA
		Com'l			64	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

Preliminary

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F621, 622			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage, A_1-A_8	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3.0mA	Mil	2.4	3.4		V
				Com'l	2.7	3.4		V
V_{OH}	HIGH-level output voltage, B_1-B_8	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −12mA	Mil	2.0			V
			I_{OH} = −15mA	Com'l	2.0			V
			I_{OH} = −3.0mA	Mil	2.4	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage, A_1-A_8	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = 24mA				0.35	0.5	V
V_{OL}	LOW-level output voltage B_1-B_8	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MAX	I_{OL} = 48mA	Mil		0.35	0.5	V
			I_{OL} = 64mA	Com'l		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = +7.0V					100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V					−20	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH					mA
			I_{CCL} Outputs LOW				143	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

5

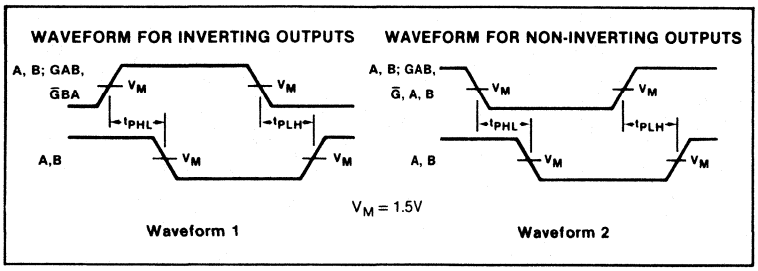
AC CHARACTERISTICS

PARAMETER		TEST CONDITIONS	54/74F			54F		74F		UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A, V_{CC} = Mil, C_L = 50pF, R_L = 500Ω		T_A, V_{CC} = Com'l, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to B, B to A	Waveform 2, 'F621			6.5 7.0					ns
t_{PLH} t_{PHL}	Propagation delay A to B, B to A	Waveform 1, 'F622			8.0 9.0					ns
t_{PLH}	Propagation delay $\overline{G}$BA input to A output GAB input to B output	 Waveform 1 Waveform 2			11.0					ns
t_{PHL}	Propagation delay $\overline{G}$BA input to A output GAB input to B output	 Waveform 2 Waveform 1			8.0					ns

NOTE
Subtract 0.2ns from minimum values for SO package.

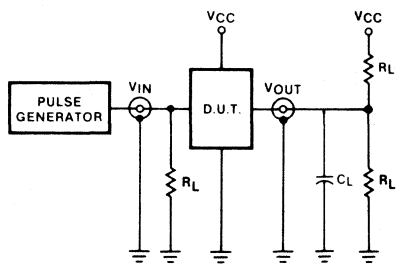
Preliminary

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS

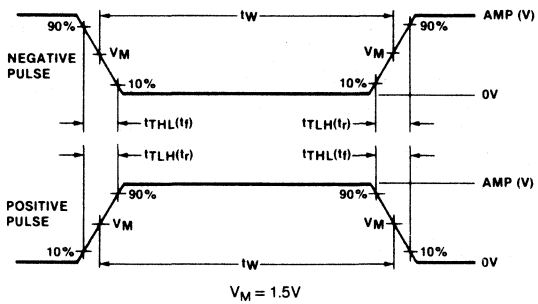
TEST CIRCUIT FOR OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Preliminary

'F630 — 16-Bit Parallel Error Detection and Correction Circuit (3-State)
'F631 — 16-Bit Parallel Error Detection and Correction Circuit (Open-Collector)

- High impedance NPN base input for reduced loading (20μA in HIGH and LOW states)
- Detects and corrects single-bit errors
- Detects and flags dual-bit errors
- Fast processing times:
  - Write cycle: Generates check word in 20ns typical
  - Read cycle: Flags errors in 25ns typical
- Power dissipation 600mW (typical)
- Choice of output configurations
  - 'F630: 3-State
  - 'F631: Open-Collector

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F630	17ns	120mA
74F631	17ns	120mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F630N • N74F631N	
Plastic SO	N74F630D • N74F631D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
S_0, S_1	Control	1.0/0.033	20μA/20μA
CB_0-CB_{15}	Check Bits, Input	1.0/0.033	20μA/20μA
DB_0-DB_{15}	Data Bits, Input	1.0/0.033	20μA/20μA
CB_0-CB_{15}	Check Bits, Output for 'F630	150/33.3	3mA/20mA
CB_0-CB_{15}	Check Bits, Output for 'F631	OC/33.3	OC/20mA
DB_0-DB_{15}	Data Bits, Output for 'F630	150/33.3	3mA/20mA
DB_0-DB_{15}	Data Bits, Output for 'F631	OC/33.3	OC/20mA
SEF, DEF	Error Flags for 'F630	150/33.3	3mA/20mA
SEF, DEF	Error Flags for 'F631	OC/33.3	OC/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state. OC = Open Collector.

DESCRIPTION

The 'F630 and 'F631 devices are 16-bit parallel error detection and correction circuits (EDACs) in 28-pin, 600-mil packages. They use a modified Hamming code to generate a 6-bit check word from a 16-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 22-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

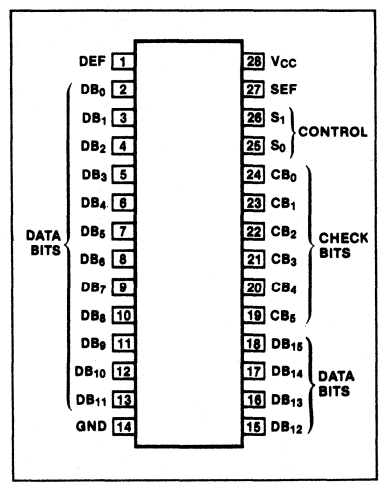
Single-bit errors in the 16-bit data word are flagged and corrected.

Single-bit errors in the 6-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 16-bit word is not in error. The correction cycle will simply pass along the original 16-bit word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These dual errors may occur in any 2 bits of the 22-bit word from memory (two errors in the 16-bit data word, two errors in the 6-bit check word, or one error in each word).

The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 22-bit word are beyond the capabilities of these devices to detect.

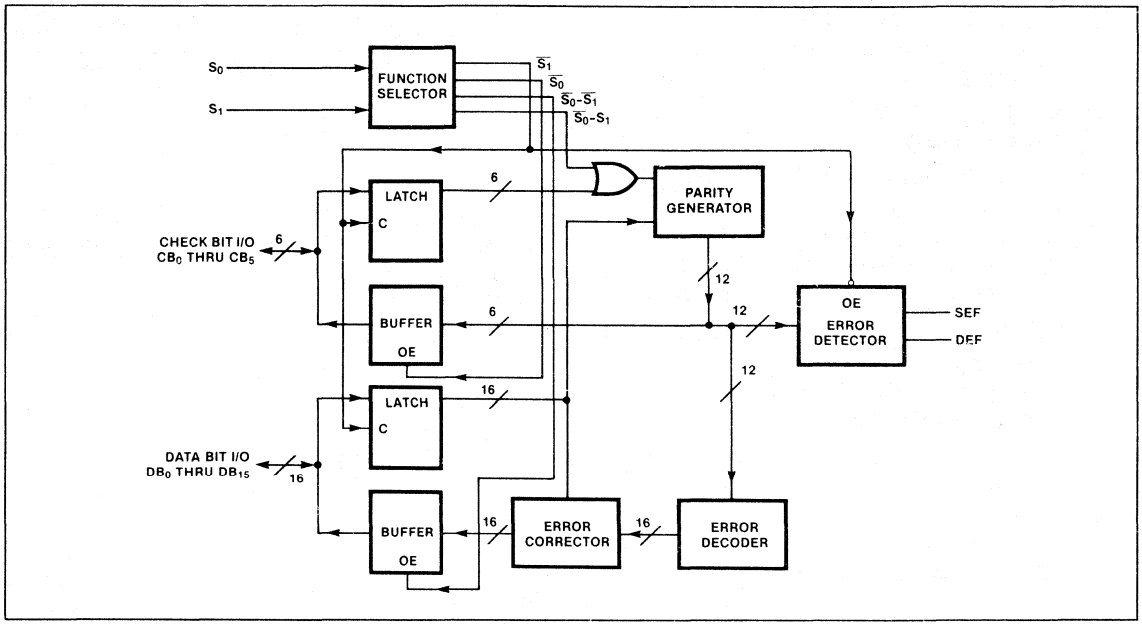
PIN CONFIGURATION



ERROR DETECTION/CORRECTION FAST 54/74F630, 54/74F631

Preliminary

LOGIC DIAGRAM



In order to be able to determine whether the data from the memory is acceptable to use as presented to the bus, the EDAC must be strobed to enable the error flags and the flags will have to be tested for the zero condition.

The first case in the error function table represents the normal, no-error condition. The CPU sees lows on both flags. The next two cases of single-bit errors require data correction. Although the EDAC can discern the single check bit error and ignore it, the error flags are identical to the single error in the 16-bit data word. The CPU will ask for data correction in both cases. An interrupt condition to the CPU results in each of the last three cases, where dual errors occur.

FUNCTION TABLE

TOTAL NUMBER OF ERRORS		ERROR FLAGS		DATA CORRECTION
16-Bit Data	6-Bit Checkword	SEF	DEF	
0	0	L	L	Not Applicable
1	0	H	L	Correction
0	1	H	L	Correction
1	1	H	H	Interrupt
2	0	H	H	Interrupt
0	2	H	H	Interrupt

H = HIGH voltage level, L = LOW voltage level

CHECK WORD BIT	16-BIT DATA WORD															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB_0	X	X		X	X				X	X	X			X		
CB_1	X		X	X		X	X		X			X			X	
CB_2		X	X		X	X		X		X			X			X
CB_3	X	X	X				X	X			X	X	X			
CB_4				X	X	X	X	X						X	X	X
CB_5									X	X	X	X	X	X	X	X

NOTE
The six check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

ERROR DETECTION AND CORRECTION DETAILS

During a memory write cycle, six check bits (CB_0-CB_5) are generated by eight-input parity generators using the data bits as defined below. During a memory read cycle, the 6-bit check word is retrieved along with the actual data.

Error detection is accomplished as the 6-bit check word and the 16-bit data word from memory are applied to internal parity generators/checkers. If the parity of all six groupings of data and check bits is correct, it is assumed that no error has occurred and both error flags will be low. (It should be noted that the sense of two of the check bits, CB_0 and CB_1, is inverted to ensure that the gross-error condition of all lows and all highs is detected).

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set high. Any single error in the 16-bit data word will change the sense of exactly 3 bits of the 6-bit check word. Any single error in the 6-bit check word changes the

ERROR DETECTION/CORRECTION — FAST 54/74F630, 54/74F631

Preliminary

sense of only that one bit. In either case, the single-error flag will be set high while the dual-error flag will remain low.

Any 2-bit error will change the sense of an even number of check bits. The 2-bit error is not correctable, since the parity tree can only identify single-bit errors. Both error flags are set high when any 2-bit error is detected.

Three or more simultaneous bit errors can fool the EDAC into believing that no error, a correctable error, or an uncorrectable error has occurred and produce erroneous results in all three cases.

Error correction is accomplished by identifying the bad bit and inverting it. Identification of the erroneous bit is achieved by comparing the 16-bit data word and 6-bit check word from memory with the new check word with one (check word error) or three (data word error) inverted bits.

As the corrected word is made available on the data word I/O port, the check word I/O port presents a 6-bit syndrome error code. This syndrome code can be used to identify the bad memory chip.

ERROR SYNDROME TABLE

ERROR LOCATION	SYNDROME ERROR CODE					
	CB_0	CB_1	CB_2	CB_3	CB_4	CB_5
DB_0	L	L	H	L	H	H
DB_1	L	H	L	L	H	H
DB_2	H	L	L	L	H	H
DB_3	L	L	H	H	L	H
DB_4	L	H	L	H	L	H
DB_5	H	L	L	H	L	H
DB_6	H	L	H	L	L	H
DB_7	H	H	L	L	L	H
DB_8	L	L	H	H	H	L
DB_9	L	H	L	H	H	L
DB_{10}	L	H	H	L	H	L
DB_{11}	H	L	H	L	H	L
DB_{12}	H	H	L	L	H	L
DB_{13}	L	H	H	H	L	L
DB_{14}	H	L	H	H	L	L
DB_{15}	H	H	L	H	L	L
CB_0	L	H	H	H	H	H
CB_1	H	L	H	H	H	H
CB_2	H	H	L	H	H	H
CB_3	H	H	H	L	H	H
CB_4	H	H	H	H	L	H
CB_5	H	H	H	H	H	L
No Error	H	H	H	H	H	H

H = HIGH voltage level
L = LOW voltage level

5

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	'F631			−1	mA
		'F630			−3	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

ERROR DETECTION/CORRECTION FAST 54/74F630, 54/74F631

Preliminary

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F630			54/74F631			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	Mil	2.4	3.4					V
				Com'l	2.7	3.4					V
			I_{OH} = −1mA	Mil				2.5	3.4		V
				Com'l				2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2		−0.73	−1.2	V
I_{OZH}	Off-State output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V				2	50				μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				−2	−50				μA
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100		5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20		1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−1	−20		−1	−20	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−60	−80	−150	−60	−80	−150	mA
I_{CC}	Total supply current	'F630	V_{CC} = MAX, Outputs open	Outputs HIGH							mA
				Outputs LOW							mA
				Outputs at Hi-Z							mA
		'F631	V_{CC} = MAX, Outputs open	Outputs HIGH							mA
				Outputs LOW							mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

ERROR DETECTION/CORRECTION FAST 54/74F630, 54/74F631

Preliminary

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F630 $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F630 T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F630 T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay time, LOW-to-HIGH level output, DB to CB	Waveform 1			22					ns
t_{PHL}	Propagation delay time, HIGH-to-LOW level output, DB to CB	Waveform 1			20					ns
t_{PLH} t_{PHL}	Propagation delay time, SI to DEF, SEF	Waveform 1			13 12					ns
t_{PZH}	Output enable time to HIGH level, SO to CB, DB	Waveform 4			12					ns
t_{PZL}	Output enable time to LOW level, SO to CB, DB	Waveform 3			12					ns
t_{PHZ}	Output disable time from HIGH level, SO to CB, DB	Waveform 4			15					ns
t_{PLZ}	Output disable time from LOW level, SO to CB, DB	Waveform 3			15					ns

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

5

PARAMETER		TEST CONDITIONS	54/74F631 $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F631 T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F631 T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay time, LOW-to-HIGH level output, DB to CB	Waveform 1			25					ns
t_{PHL}	Propagation delay time, HIGH-to-LOW level output, DB to CB	Waveform 1			18					ns
t_{PLH} t_{PHL}	Propagation delay time, SI to DEF, SEF	Waveform 1			16 11					ns
t_{PHL}	Propagation delay time, HIGH-to-LOW level output, SO to CB, DB	Waveform 1			12					ns
t_{PLH}	Propagation delay time, LOW-to-HIGH level output, SO to CB, DB	Waveform 1			16					ns

NOTE
Subtract 0.2ns from minimum values for SO package.

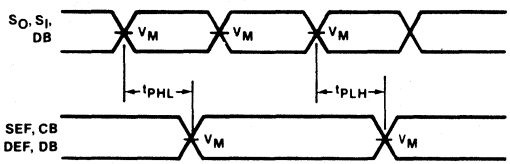
AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_s	Setup time, CB or DB to SI	Waveform 2	4							ns
t_h	Hold time, CB or DB to SI	Waveform 2	4							ns

Preliminary

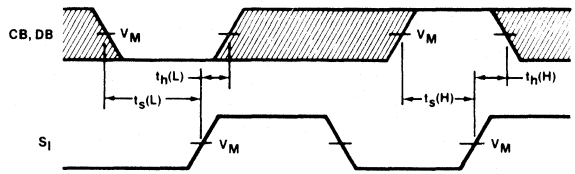
AC WAVEFORMS

DB TO CB
S_I TO DEF, SEF } DELAYS
S_O TO CB, DB



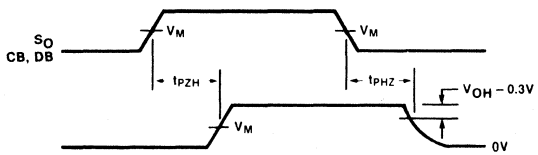
Waveform 1

DATA SETUP AND HOLD TIMES



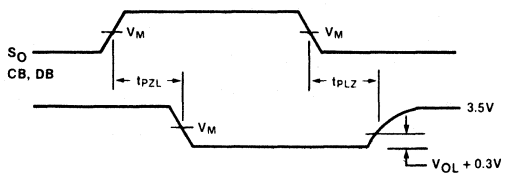
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

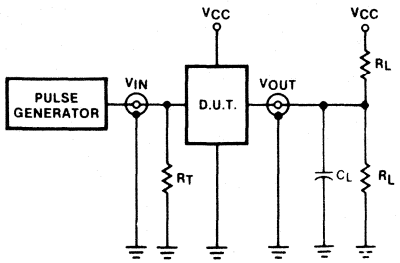
$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

Preliminary

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 OPEN-COLLECTOR OUTPUTS ('F631)



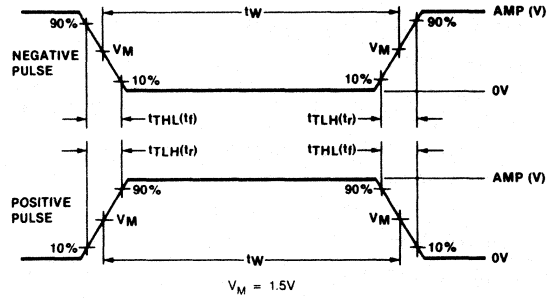
DEFINITIONS

R_L = Load resistor. See AC CHARACTERISTICS for value.

C_L = Load, capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

INPUT PULSE DEFINITIONS



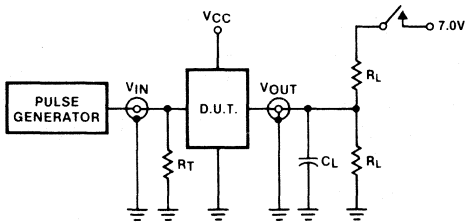
V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

TEST CIRCUITS AND WAVEFORMS

5

TEST CIRCUIT FOR 3-STATE OUTPUTS ('F630)



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

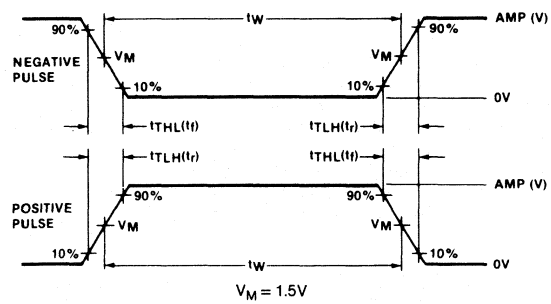
DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

TRANSCEIVERS/REGISTERS FAST 54/74F646, 647, 648, 649

Preliminary

'F646 — Octal Transceiver/Register, Non-Inverting (3-State)
'F647 — Octal Transceiver/Register, Non-Inverting (Open Collector)
'F648 — Octal Transceiver/Register, Inverting (3-State)
'F649 — Octal Transceiver/Register, Inverting (Open Collector)

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of true and inverting data paths**
- **Choice of 3-State or Open-Collector outputs**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F646		
74F647		
74F648		
74F649		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74F646N • N74F647N N74F648N • N74F649N	
Plastic SO	N74F646D • N74F647D N74F648D • N74F649D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

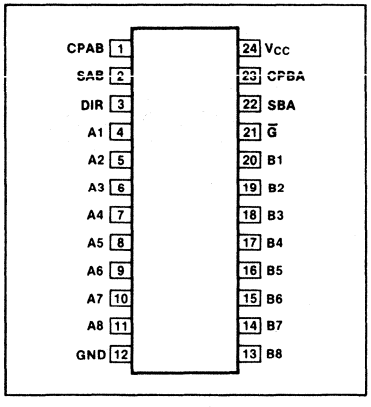
These devices consist of bus transceiver circuits with 3-State or Open-Collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a HIGH logic level. Enable $\overline{G}$ and Direction DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register, or in both. The Select (S) controls can multiplex stored and real-time (transparent mode) data. The Direction DIR determines which bus will receive data when the Enable $\overline{G}$ is active (LOW). In the isolation mode (Enable $\overline{G}$, HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

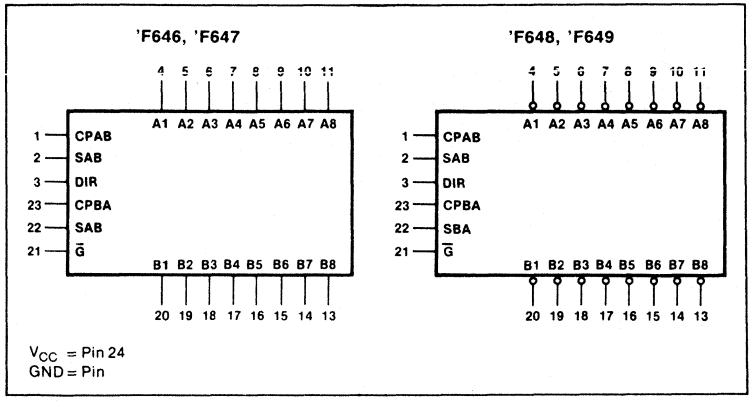
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A_1-A_8, B_1-B_8	Data Register A, B Inputs	1.0/1.0	20μA/20μA
A_1-A_8, B_1-B_8	Data Register A, B Outputs	150/33.3	3mA/20mA
CPAB, CPBA	Clock Pulse Inputs	1.0/1.0	20μA/20μA
SAB, SBA	Transmit/Receive Inputs	1.0/1.0	20μA/20μA
DIR, $\overline{G}$	Output Enable Inputs	1.0/1.0	20μA/20μA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION

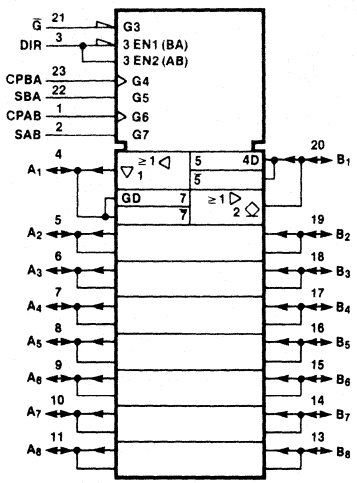


LOGIC SYMBOL

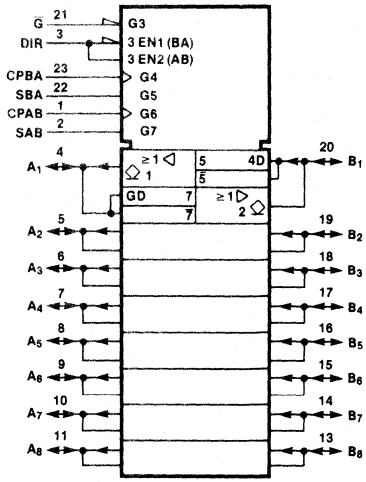


LOGIC SYMBOL (IEEE/IEC)

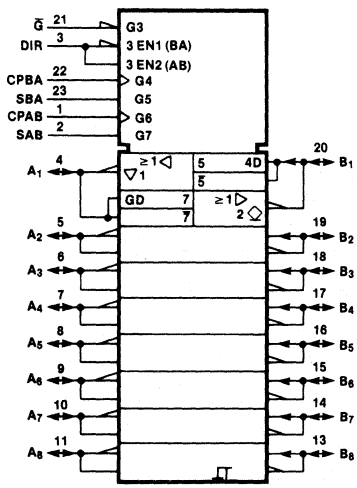
'F646



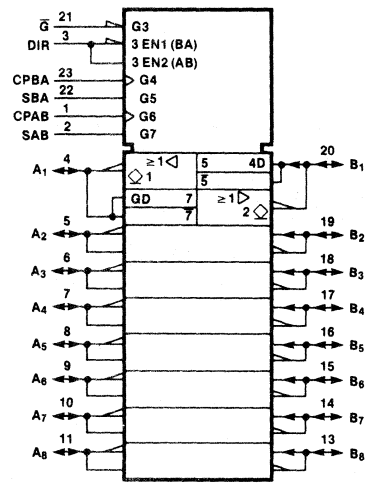
'F647



'F648

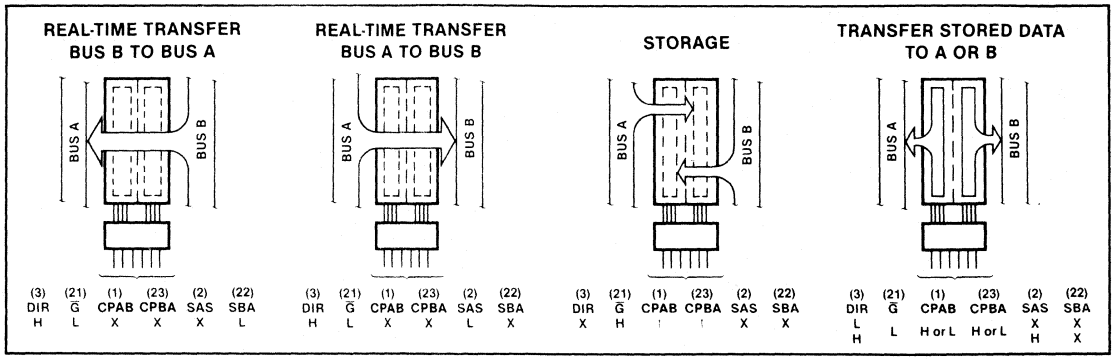


'F649



5

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'F646, 'F647, 'F648, or 'F649.



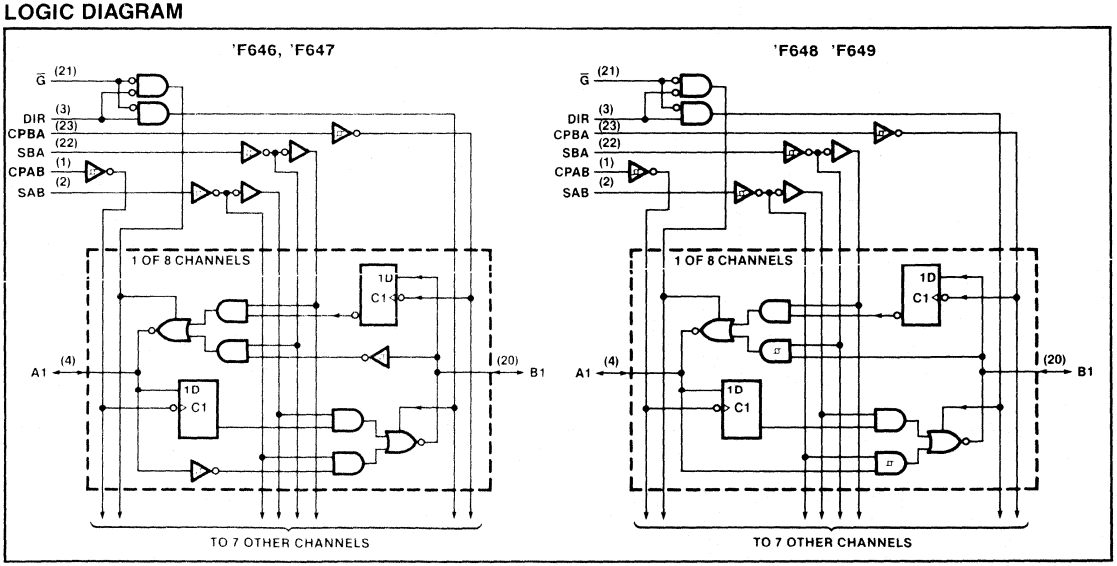
FUNCTION TABLE

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A1-A8	B1-B8	'F646, 'F647	'F648, 'F649
H H	X X	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data
L L	L L	X X	X X	X X	L H	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus	Real Time $\overline{B}$ Data to A Bus Stored $\overline{B}$ Data to A Bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real Time A Data to B Bus Stored A Data to B Bus	Real Time $\overline{A}$ Data to B Bus Stored $\overline{A}$ Data to B Bus

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

H = high level X = irrelevant
L = low level ↑ = low-to-high level transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	'F647, 'F649			−1	mA
		'F646, 'F648			−3	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F646, 'F648			54/74F647, 'F649			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	Mil	2.4	3.4					V
				Com'l	2.7	3.4					V
			I_{OH} = −1mA	Mil				2.5	3.4		V
				Com'l				2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2		−0.73	−1.2	V
I_{OZH}	Off-State output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V				2	50				μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				−2	−50				μA
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				5	100		5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20		1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−1	−20		−1	−20	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−60	−80	−150	−60	−80	−150	mA
I_{CC}	Total supply current	'F646, 'F648	V_{CC} = MAX, Outputs open	Outputs HIGH							mA
				Outputs LOW							mA
				Outputs at Hi-Z							mA
		'F647, 'F649	V_{CC} = MAX, Outputs open	Outputs HIGH							mA
				Outputs LOW							mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F646,'F648 $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F646,'F648 T_A, V_{CC} = Mil $C_L = 50pF$ $R_L = 500\Omega$		74F646,'F648 T_A, V_{CC} = Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} Clock to bus t_{PHL} CPBA or CPAB to A or B	Waveform 1							13 13	ns
t_{PLH} Bus to bus t_{PHL} A or B to B or A	Waveforms 2 and 3							11 11	ns
t_{PLH} Select with Bus input HIGH to bus t_{PHL} SBA or SAB to A or B	Waveforms 2 and 3							13 13	ns
t_{PLH} Select with Bus input LOW to bus t_{PHL} SBA or SAB to A or B								13 13	ns
t_{PZH} Enable to bus t_{PZL} $\overline{G}$ to A or B	Waveforms 4 and 5							13.5 12.5	ns
t_{PZH} Direction to bus t_{PZL} DIR to A or B								12.5 12.5	ns
t_{PHZ} Enable to bus t_{PLZ} $\overline{G}$ to A or B	Waveforms 4 and 5							10.5 10.5	ns
t_{PHZ} Direction to bus t_{PLZ} DIR to A or B								10.5 10.5	ns

5

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F647,'F649 $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F647,'F649 T_A, V_{CC} = Mil $C_L = 50pF$ $R_L = 500\Omega$		74F647,'F649 T_A, V_{CC} = Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} Clock to bus t_{PHL} CPBA or CPAB to A or B	Waveform 1							13 13	ns
t_{PLH} Bus to bus t_{PHL} A or B to B or A	Waveforms 2 and 3							11 11	ns
t_{PLH} Select with Bus input HIGH to bus t_{PHL} SBA or SAB to A or B	Waveforms 4 and 5							13 13	ns
t_{PLH} Select with Bus input LOW to bus t_{PHL} SBA or SAB to A or B								13 13	ns

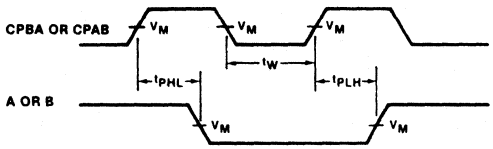
NOTE
Subtract 0.2ns from minimum values for SO package.

AC SETUP REQUIREMENTS

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_w Width of clock pulse	Waveform 1						4		ns
t_s Setup time (bus to clock)	Waveform 6						3		ns
t_h Hold time (bus to clock)	Waveform 6						1		ns

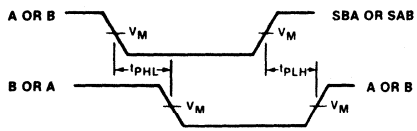
AC WAVEFORMS

CLOCK TO BUS DELAYS AND CLOCK PULSE WIDTH



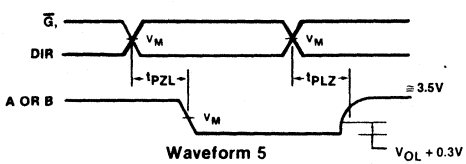
Waveform 1

BUS TO BUS AND SELECT WITH BUS INPUT HIGH AND LOW TO BUS DELAYS



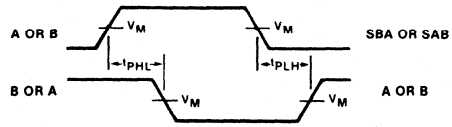
Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



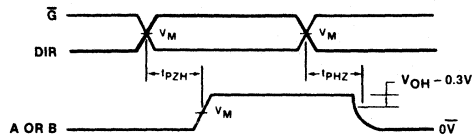
Waveform 5

BUS TO BUS AND SELECT WITH BUS INPUT HIGH AND LOW TO BUS DELAYS



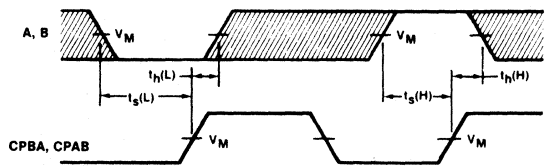
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 4

DATA SETUP AND HOLD TIMES



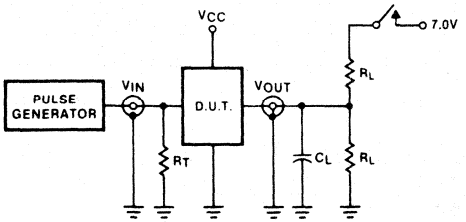
Waveform 6

$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



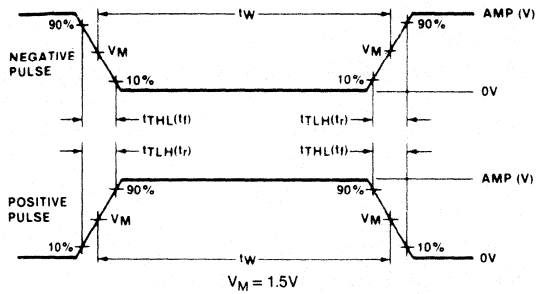
SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



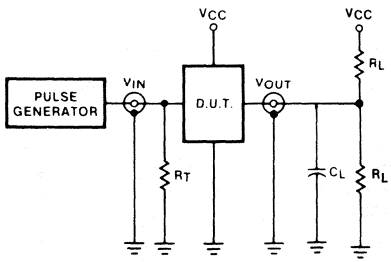
$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

TEST CIRCUITS AND WAVEFORMS

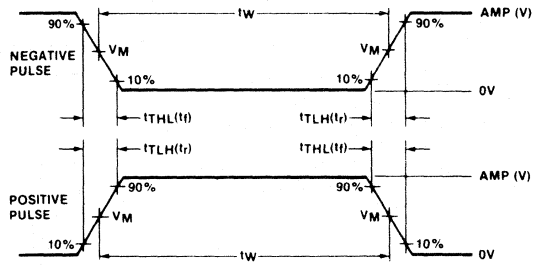
TEST CIRCUIT FOR OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

'F655 — Octal Buffer/Line Driver with Parity, Inverting (3-State)
'F656 — Octal Buffer/Line Driver with Parity, Non-Inverting (3-State)

- High impedance NPN base input for reduced loading (20μA in HIGH and LOW states)
- Inverting ('F655) or non-inverting ('F656) outputs
- 24-pin plastic slim dip (300-mil) package
- 'F655 combines 'F240 and 'F280 functions in one package
- 'F656 combines 'F241 and 'F280A functions in one package
- Inputs on one side and outputs on the other side simplify PC board layout
- 3-State outputs
- Outputs sink 64mA
- 15mA source current

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F655	8ns	83mA
74F656	8ns	83mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74F655N • N74F656N	
Plastic SO	N74F655D • N74F656D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

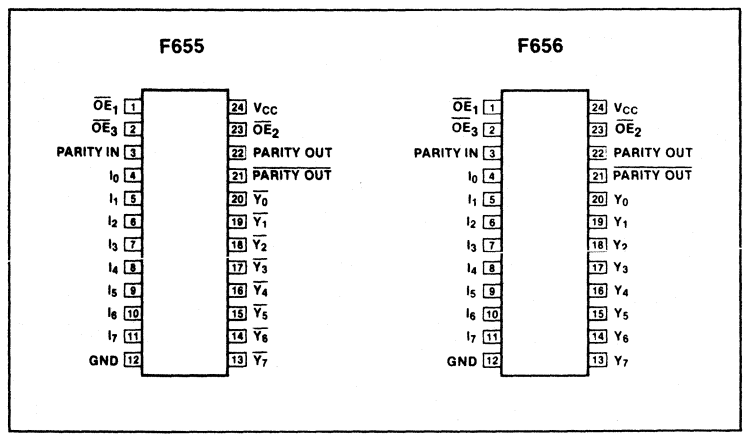
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$	3-State Output Enable (Active LOW)	1.0/0.033	20μA/20μA
PARITY IN	Input	1.0/0.033	20μA/20μA
I_n	Input	1.0/0.033	20μA/20μA
Y_n, PARITY OUT	Outputs	150/33	3mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

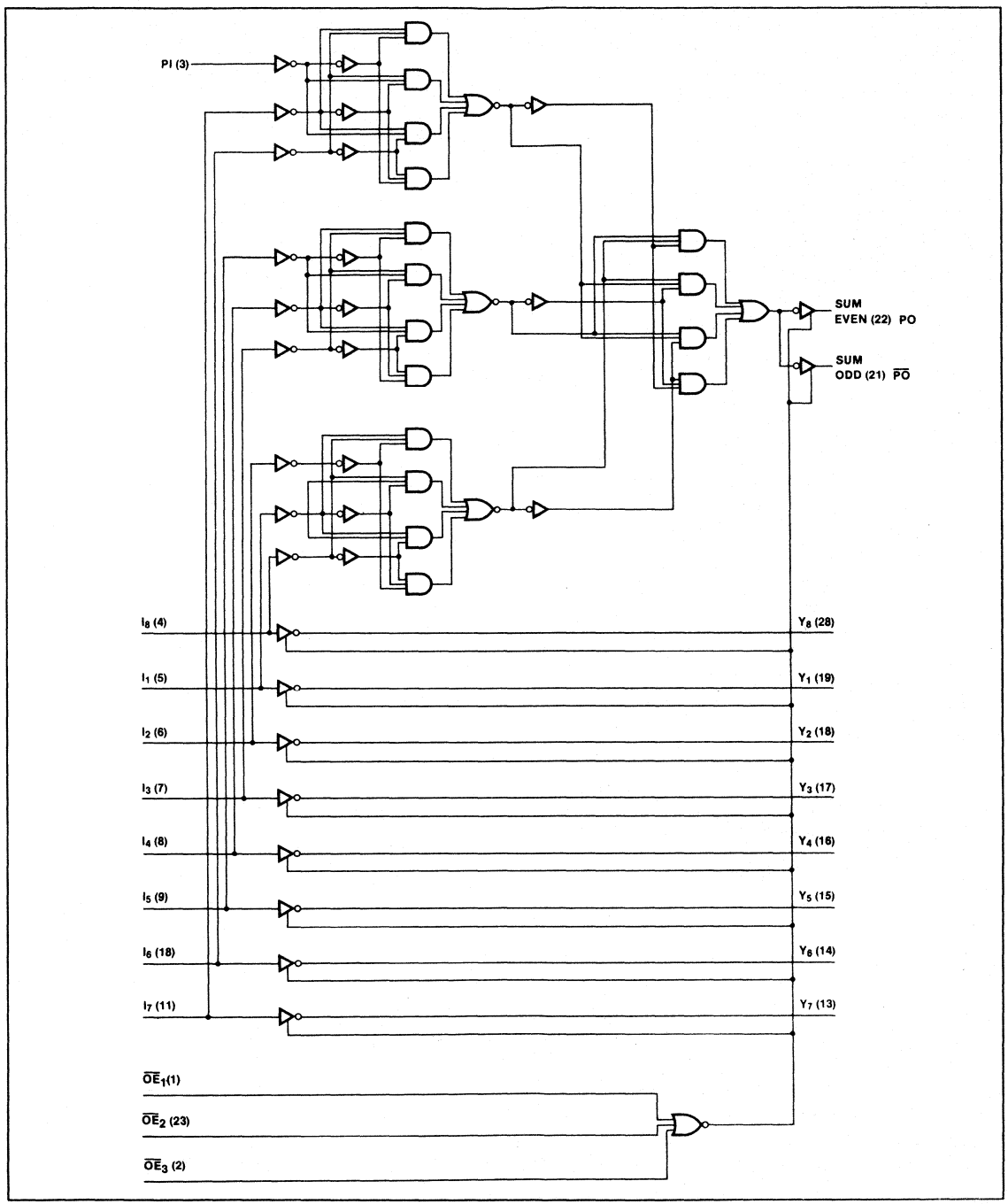
DESCRIPTION

The 'F655 and 'F656 are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE, 'F655

INPUTS				OUTPUT
OE_1	OE_2	OE_3	D	
L	L	L	L	H
L	L	L	H	L
H	H	H	X	Z

FUNCTION TABLE, 'F656

INPUTS				OUTPUT
OE_1	OE_2	OE_3	D	
L	L	L	L	L
L	L	L	H	H
H	H	H	X	Z

H = HIGH voltage level
L = LOW voltage level
Z = High impedance (OFF) level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	96	128	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current	Mil			48	mA
		Com'l			64	mA
T_A	Operating free-air temperature	Mil	−55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F655, 'F656			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = −12mA	Mil	2.0			V
			I_{OH} = −15mA	Com'l	2.0			V
		V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = −3mA	Mil	2.4	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 48mA	Mil		0.35	0.5	V
			I_{OL} = 64mA	Com'l		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V					50	μA
I_{OZL}	Off-state output current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					−50	μA
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−1	−20	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V			−100		−225	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		45	70	mA
			I_{CCL}	Outputs LOW		65	105	mA
			I_{CCZ}	Outputs OFF		55	95	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

5

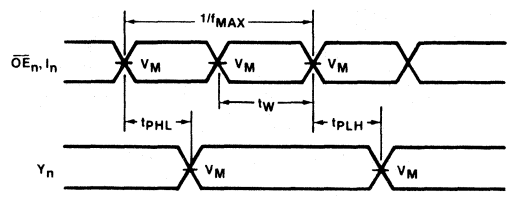
AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F			54F		74F		UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A, V_{CC} = Mil, C_L = 50pF, R_L = 500Ω		T_A, V_{CC} = Com'l, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 'F655	4.0 2.0	7.5 3.5	11.5 5.0	3.5 1.5	15.0 6.0	4.0 2.0	13.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 'F656	3.0 4.0	4.0 6.0	6.5 9.5	2.5 3.0	8.0 12.0	3.0 4.0	7.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay Data to Parity Output	Waveform 'F655	6.5 8.0	10.0 11.0	13.0 14.5	6.0 7.0	15.0 18.0	6.5 8.0	14.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay Data to Parity Output	Waveform 'F656	6.5 8.0	9.0 11.0	13.0 15.0	6.0 7.0	16.0 20.0	6.5 8.0	14.0 16.5	ns
t_{PZH} t_{PZL}	Enable time to HIGH level Enable time to LOW level	Waveform 2 Waveform 3 'F655	7.0 8.0	13.0 13.0	16.5 19.5	6.0 7.5	19.5 24.0	7.0 8.0	18.0 23.0	ns
t_{PHZ} t_{PLZ}	Disable time from HIGH level Disable time from LOW level	Waveform 2 Waveform 3 'F655	3.0 3.5	6.5 7.0	9.0 8.5	2.5 3.0	11.5 11.0	3.0 3.5	10.0 9.0	ns
t_{PZH} t_{PZL}	Enable time to HIGH level Enable time to LOW level	Waveform 2 Waveform 3 'F656	7.0 8.0	12.0 12.0	17.5 18.5	6.5 7.5	19.5 23.0	7.0 8.0	18.0 21.5	ns
t_{PHZ} t_{PLZ}	Disable time from HIGH level Disable time from LOW level	Waveform 2 Waveform 3 'F656	2.0 2.5	4.0 4.0	6.5 7.5	1.5 2.0	8.5 9.0	2.0 2.5	6.5 7.5	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

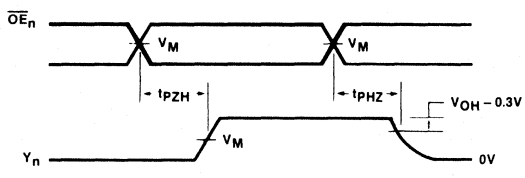
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



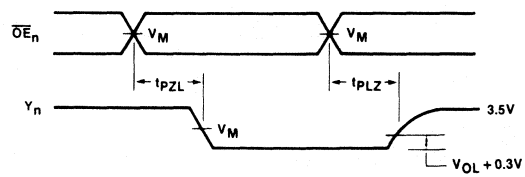
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL

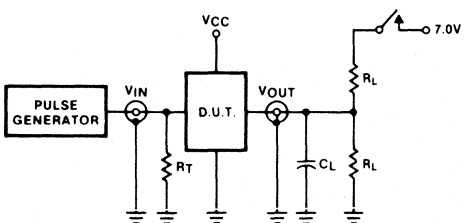


Waveform 3

$V_M = 1.5V$

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



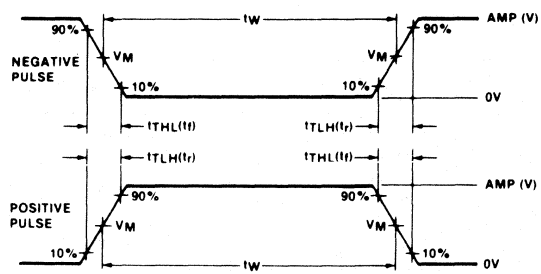
SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

TRANSCEIVER FAST 54/74F657

Preview

Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker (3-State Outputs)

- **High-impedance NPN base input for reduced loading (20μA with HIGH and LOW states)**
- **24-pin plastic slim dip (300-mil) package**
- **Combines 'F245 and 'F280A functions in one package**
- **3-State outputs**
- **Outputs sink 64mA**
- **15mA source current**
- **Input diodes for termination effects**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F657		120mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F657N	
Plastic SO	N74F657D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/0.033	20μA/20μA
T/$\overline{R}$	Transmit/Receive Input	1.0/0.033	20μA/20μA
A_0-A_7	Side A, 3-State Inputs	1.0/0.033	20μA/20μA
B_0-B_7	Side B, 3-State Inputs	1.0/0.033	20μA/20μA
A_0-A_7	Side A, 3-State Outputs	150/40	3mA/24mA
B_0-B_7	Side B, 3-State Outputs (Commercial)	750/107	15mA/64mA
	Side B, 3-State Outputs (Military)	600/80	12mA/48mA
PARITY	Parity Output/Error Output	150/40	3mA/24mA

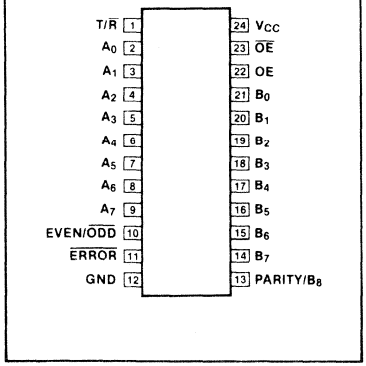
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

DESCRIPTION

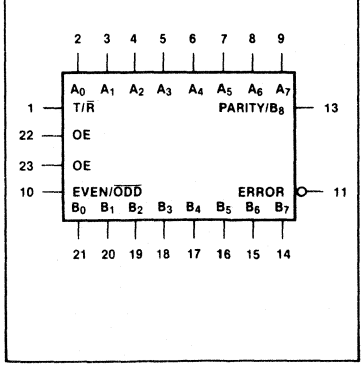
The 'F657 contains eight non-inverting buffers with 3-State outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 20mA at the A ports and 64mA at the B ports. The Transmit/Receive (T/$\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports. The Output Enable inputs disable both the A and B ports by placing them in a High-Z condition when either the $\overline{OE}$ input is HIGH or the $\overline{OE}$ input is LOW.

The parity generator detects whether an even or odd number of bits on the A ports are HIGH, depending on the condition of the Even/$\overline{Odd}$ input. If the Even input is active HIGH and an even number of A inputs are HIGH, the Parity output is HIGH. The parity of the data received on the B ports is compared with the Even/$\overline{Odd}$ input and the Error output is LOW if not equal.

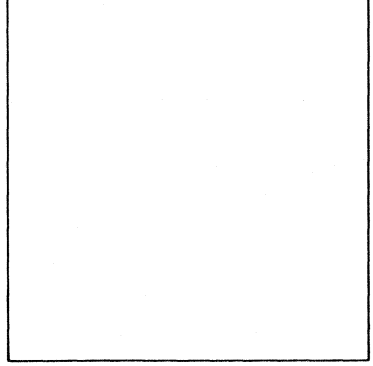
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

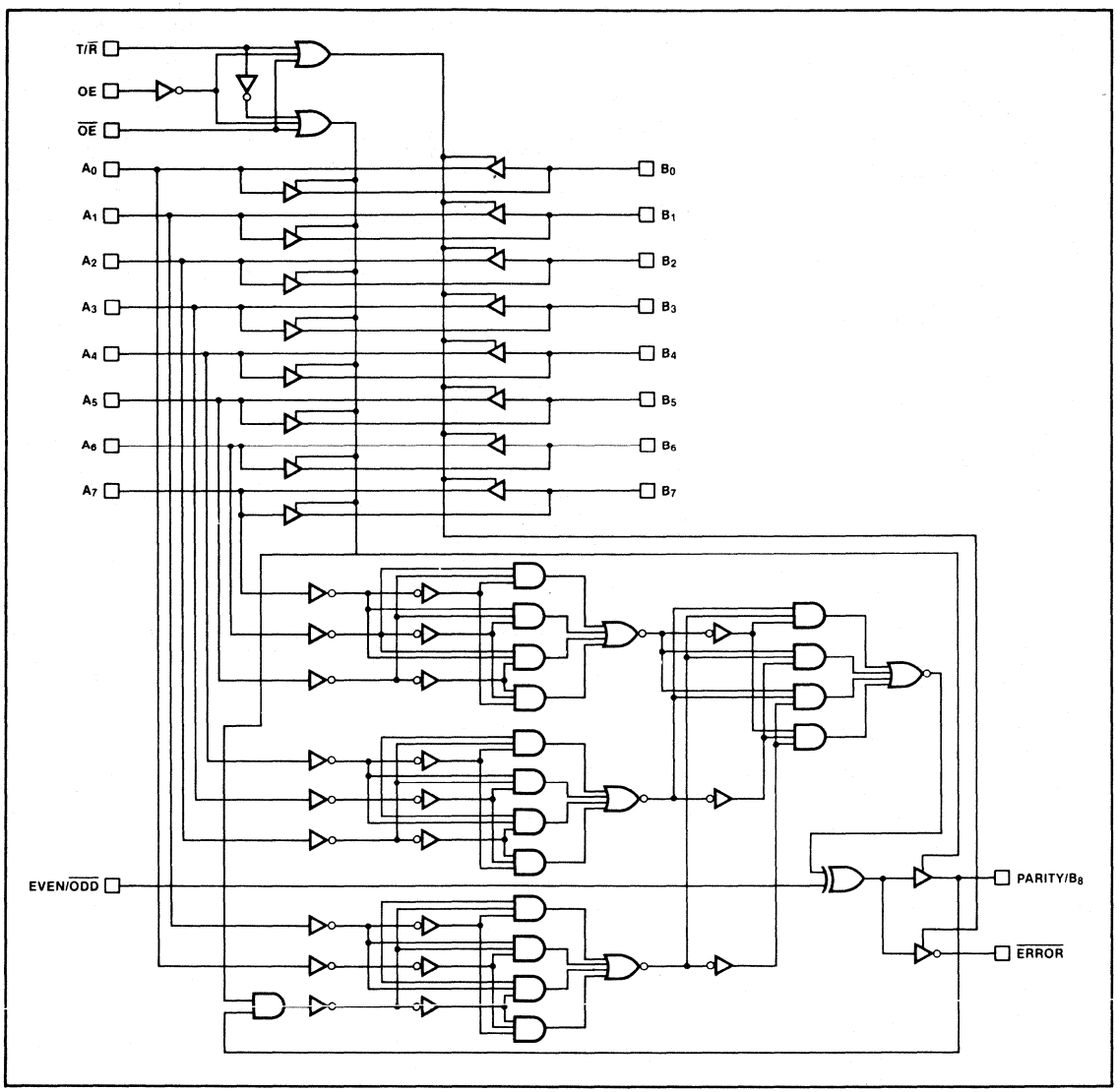


5

TRANSCEIVER FAST 54/74F657

Preview

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High-Z State

NUMBER OF INPUTS I_0-I_8 THAT ARE HIGH	PARITY	
	Even	Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TRANSCEIVER FAST 54/74F657

Preview

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER			54F	74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	A_0–A_7	40	40	mA
		B_0–B_7	128	128	mA
T_A	Operating free-air temperature range		−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current, A_0–A_7 parity error	Mil			−3	mA
		Com'l			−3	mA
I_{OH}	HIGH-level output current, B_0–B_7	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current, A_0–A_7 parity error	Mil			20	mA
		Com'l			20	mA
I_{OL}	LOW-level output current, B_0–B_7	Mil			48	mA
		Com'l			64	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

5

TRANSCEIVER FAST 54/74F657

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F657			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage, A_0-A_7 parity error	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3.0mA	Mil	2.4			V
				Com'l	2.7			V
V_{OH}	HIGH-level output voltage, B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −12mA	Mil	2.0			V
			I_{OH} = −15mA	Com'l	2.0			V
			I_{OH} = −3.0mA	Mil	2.4			V
				Com'l	2.7			V
V_{OL}	LOW-level output voltage, A_0-A_7 parity error	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = 20mA					0.5	V
V_{OL}	LOW-level output voltage, B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MAX	I_{OL} = 48mA	Mil			0.55	V
			I_{OL} = 64mA	Com'l			0.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = +7.0V					100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V					−20	μA
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V					50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				120	165	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with outputs open.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

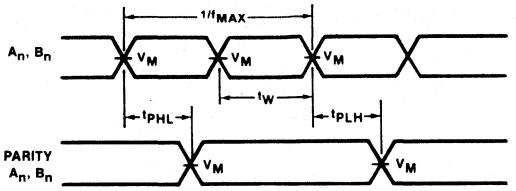
PARAMETER		TEST CONDITIONS	54/74F T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			54F T_A, V_{CC} Mil C_L = 50pF R_L = 500Ω		74F T_A, V_{CC} Com'l C_L = 50pF R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay, A_n to B_n or B_n to A_n	Waveform 1	2.5 2.5	4.2 4.6	5.5 6.0			2.5 2.5	6.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay, A_n to parity, error	Waveform 1	6.0 6.5	10 11	14 15.5			6.0 6.5	15.5 16.0	ns
t_{PZH} t_{PZL}	Output enable time	Waveform 2 Waveform 3	3.0 4.5	5.3 7.9	7.0 10			3.0 4.5	8.0 11	ns
t_{PHZ} t_{PLZ}	Output disable time	Waveform 2 Waveform 3	3.0 2.0	5.0 3.7	6.5 5.0			3.0 2.0	7.5 6.0	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

Preview

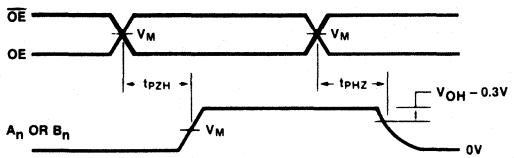
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



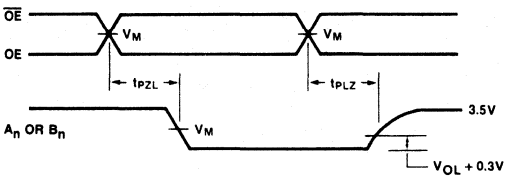
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



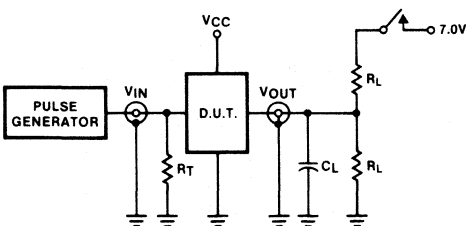
Waveform 3

VM = 1.5V

5

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



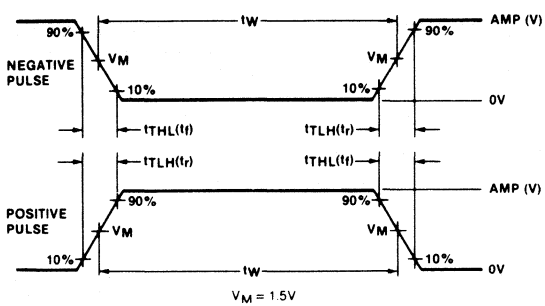
SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

INPUT PULSE DEFINITIONS



VM = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

16-BIT SHIFT REGISTER — FAST 54/74F673

Preview

16-Bit Shift Register (Serial-In/Serial-Parallel Out)

- **Serial-to-parallel converter**
- **16-bit serial I/O shift register**
- **16-bit parallel-out storage register**
- **Recirculating serial shifting**
- **Recirculating parallel transfer**
- **Common serial data I/O pin**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F673		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74F673N	
Plastic SO	N74F673D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

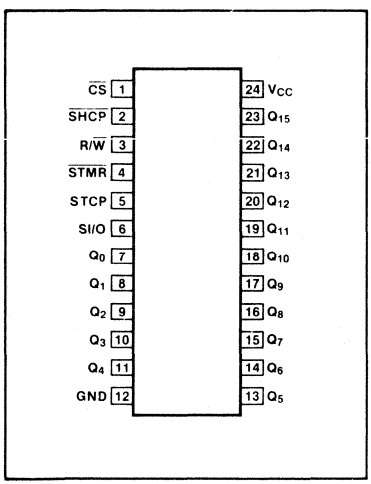
The 'F673 contains a 16-bit serial-in/serial-out shift register and a 16-bit parallel-out storage register. A single pin serves either as an input for serial entry or as a 3-state serial output. In the Serial-out mode, the data recirculates in the shift register. By means of a separate clock, the contents of the shift register are transferred to the storage register for parallel outputting. The contents of the storage register can also be parallel loaded back into the shift register. A HIGH-signal on the Chip Select input prevents both shifting and parallel transfer. The storage register may be cleared via STMR.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

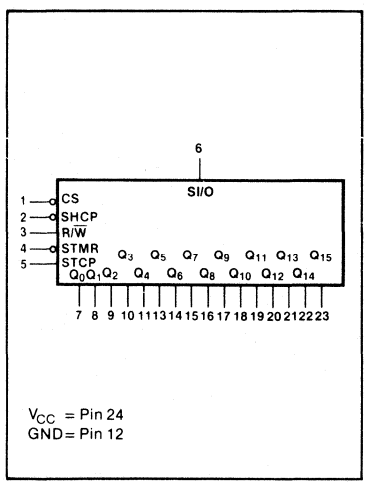
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{SHCP}$	Shift Clock Pulse Input (Active Falling Edge)	1.0/1.0	20μA/0.6mA
STMR	Store Master Reset Input (Active LOW)	1.0/1.0	20μA/0.6mA
STCP	Store Clock Pulse Input	1.0/1.0	20μA/0.6mA
R/$\overline{W}$	Read/Write Input	1.0/1.0	20μA/0.6mA
SI/O	Serial Data Input or	3.5/1.0	70μA/0.6mA
	3-State Serial Output	50/33	1.0mA/20mA
Q_0-Q_{15}	Parallel Data Outputs	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

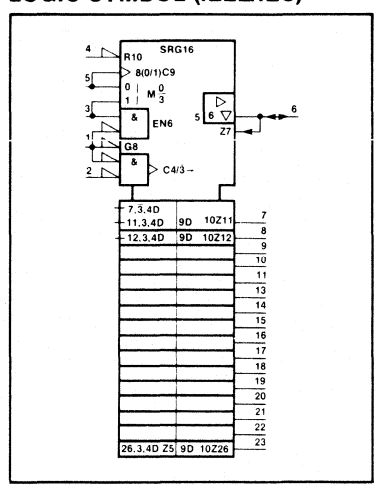
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



16-BIT SHIFT REGISTER — FAST 54/74F673

Preview

FUNCTIONAL DESCRIPTION

The 16-bit shift register operates in one of four modes, as indicated in the Shift Register Operations Table. A HIGH signal on the Chip Select ($\overline{CS}$) input prevents clocking and forces the Serial Input/Output (SI/O) 3-state buffer into the high-impedance state. During serial shift-out operations, the SI/O buffer is active (i.e., enabled) and the output data is also recirculated back into the shift register. When parallel loading the shift register from the storage register, serial shifting is inhibited.

The storage register has an asynchronous MASTER RESET ($\overline{STMR}$) input that overrides all other inputs and forces the Q_0-Q_{15} outputs LOW. The storage register is in the Hold mode whether $\overline{CS}$ or the Read/Write (R/$\overline{W}$) input is HIGH. With $\overline{CS}$ and R/$\overline{W}$ both LOW, the storage register is parallel loaded from the shift register.

To prevent false clocking of the shift register, $\overline{SHCP}$ should be in the LOW state during a LOW-to-HIGH transition of $\overline{CS}$. To prevent false clocking of the storage register, STCP should be LOW during a HIGH-to-LOW transition of $\overline{CS}$ if R/$\overline{W}$ is LOW, and should also be LOW during a HIGH-to-LOW transition of R/$\overline{W}$ if $\overline{CS}$ is LOW.

SHIFT REGISTER OPERATIONS TABLE

CONTROL INPUTS				SI/O STATUS	OPERATING MODE
$\overline{CS}$	R/$\overline{W}$	$\overline{SHCP}$	STCP		
H	X	X	X	High Z	Hold
L	L	↓	X	Data in	Serial load
L	H	↓	L	Data out	Serial output with recirculation
L	H	↓	H	Active	Parallel load; no shifting

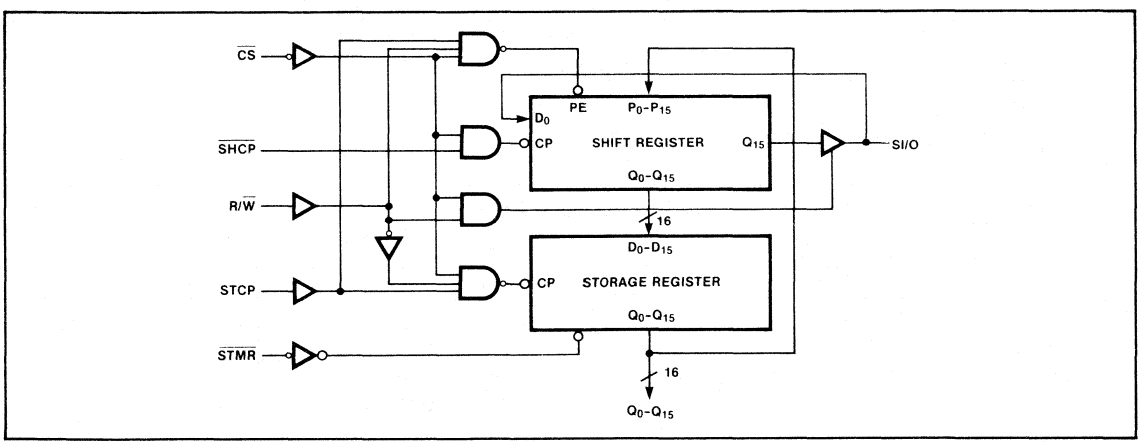
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↓ = HIGH-to-LOW clock transition

STORAGE REGISTER OPERATIONS TABLE

CONTROL INPUTS				OPERATING MODE
$\overline{STMR}$	$\overline{CS}$	R/$\overline{W}$	$\overline{STCP}$	
L	X	X	X	Reset; Outputs LOW
H	H	X	X	Hold
H	X	H	X	Hold
H	L	L	↑	Parallel Load

↑ = LOW-to-HIGH clock transition

FUNCTIONAL BLOCK DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

16-BIT SHIFT REGISTER — FAST 54/74F673

Preview

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	– 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F673			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	Mil	2.4	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			– 0.73	– 1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V			2	70	μA
I_{OZL}	Off-state output current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			– 2	– 650	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			– 0.4	– 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		– 60	– 80	– 150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH				mA
			I_{CCL} Outputs LOW			160	mA
			I_{CCZ} Outputs OFF				mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/ or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

16-BIT SHIFT REGISTER — FAST 54/74F673

Preview

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	140						MHz
t_{PLH} t_{PHL}	Propagation delay STCP to Q_n	Waveform 1	7.5 9.5	13 16	18 22					ns
t_{PHL}	Propagation delay $\overline{STMR}$ to Q_n	Waveform 2	6.0	10	14					ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHCP}$ to SI/O	Waveform 1	4.5 5.0	8.0 9.0	11 12.5					ns
t_{PZH} t_{PZL}	Output enable time $\overline{CS}$ or R/$\overline{W}$ to SI/O	Waveform 3 Waveform 4	3.0 3.0	5.0 5.0	7.0 7.0					ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{CS}$ or R/$\overline{W}$ to SI/O	Waveform 3 Waveform 4	3.0 3.0	5.0 5.0	7.0 7.0					ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC SETUP REQUIREMENTS

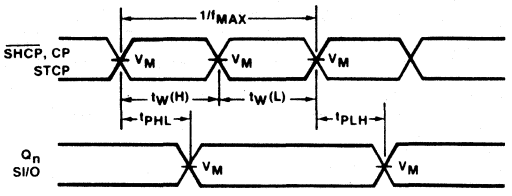
PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW $\overline{CS}$ or R/$\overline{W}$ to STCP	Waveform 5	7.0 7.0							ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{CS}$ or R/$\overline{W}$ to STCP		0 0							ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW SI/O to $\overline{SHCP}$	Waveform 5	3.0 3.0							ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW SI/O to $\overline{SHCP}$		0 0							ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW $\overline{CS}$ or R/$\overline{W}$ to $\overline{SHCP}$	Waveform 5	5.0 5.0							ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{CS}$ or R/$\overline{W}$ to $\overline{SHCP}$		0 0							ns
$t_w(H)$ $t_w(L)$	$\overline{SHCP}$ pulse width, HIGH or LOW	Waveform 1	4.0 5.0							ns
$t_w(H)$ $t_w(L)$	STCP pulse width, HIGH or LOW	Waveform 1	5.0 10							ns
$t_w(L)$	$\overline{STMR}$ pulse width LOW	Waveform 2	7.0							ns
t_{rec}	Recovery time $\overline{STMR}$ to STCP	Waveform 2	10							ns

5

Preview

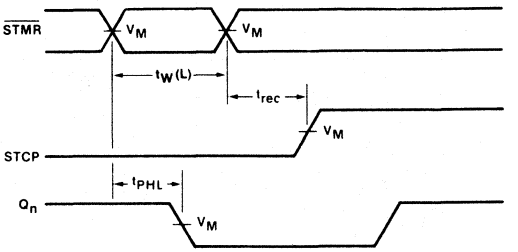
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS
AND CLOCK PULSE WIDTH



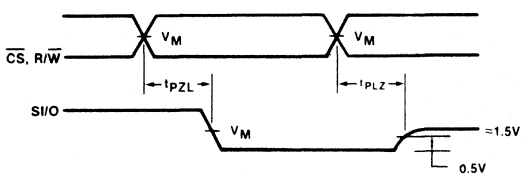
WAVEFORM 1

MASTER RESET PULSE WIDTH,
MASTER RESET TO OUTPUT DELAY AND
MASTER RESET TO CLOCK RECOVERY TIME



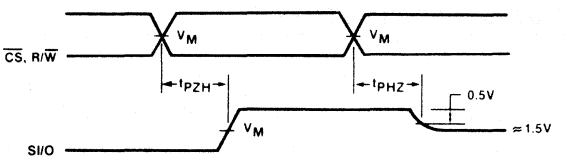
WAVEFORM 2

3-STATE ENABLE TIME TO LOW LEVEL AND
DISABLE TIME FROM LOW LEVEL



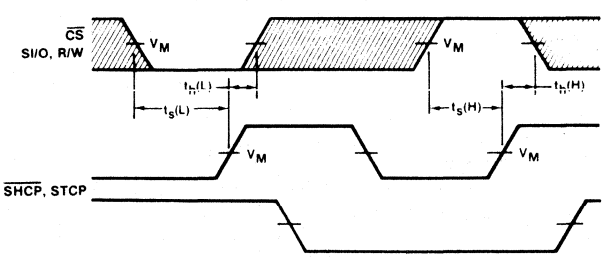
WAVEFORM 3

3-STATE ENABLE TIME TO HIGH LEVEL AND
DISABLE TIME FROM HIGH LEVEL



WAVEFORM 4

DATA SETUP AND HOLD TIMES



WAVEFORM 5

$V_M = 1.5V$

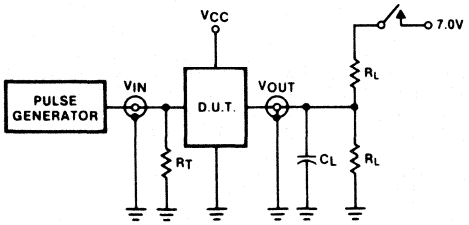
The shaded areas indicate when the input is permitted to change for predictable output performance.

16-BIT SHIFT REGISTER FAST 54/74F673

Preview

TEST CIRCUITS AND WAVEFORMS

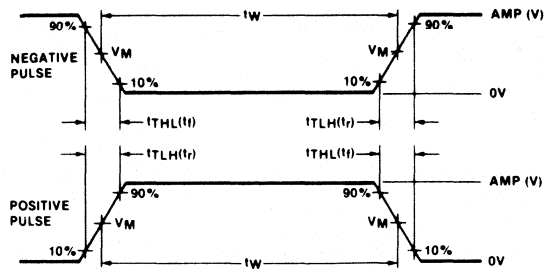
TEST CIRCUIT FOR 3-STATE OUTPUTS



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

16-BIT SHIFT REGISTER — FAST 54/74F674

Preview

16-Bit Shift Register, Serial-Parallel-In/Serial-Out (3-State)

- **16-bit serial I/O shift register**
- **16-bit parallel-in/serial-out converter**
- **Recirculating serial shifting**
- **Common serial data I/O pin**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F674		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F674N	
Plastic SO	N74F674D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F674 is a 16-bit shift register with serial and parallel load capability and serial output. A single pin serves alternately as an input for serial entry or as a 3-state serial output. In the Serial-out mode the data recirculates in the register. Chip Select, Read/Write and Mode inputs provide control flexibility.

FUNCTIONAL DESCRIPTION

The 16-bit shift register operates in one of four modes, as indicated in the Shift Register Operations Table.

Hold—a HIGH signal on the Chip Select ($\overline{CS}$) input prevents clocking and forces the Serial Input/Output (SI/O) 3-state buffer into the high-impedance state.

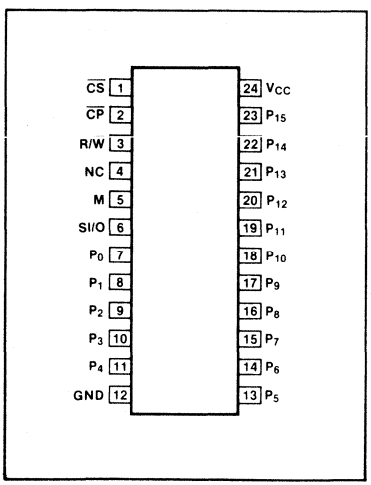
Serial Load—data present on the SI/O pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

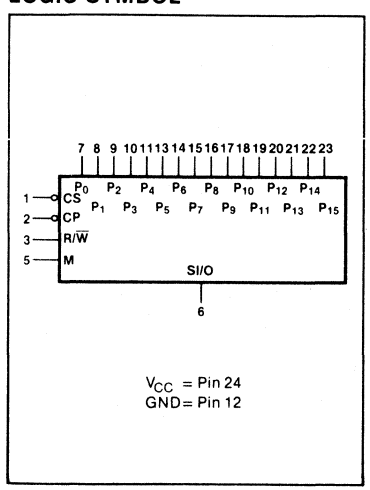
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
P_0-P_{15}	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{CS}$	Chip Select input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CP}$	Clock Pulse input (active (LOW)	1.0/1.0	20μA/0.6mA
M	Mode Select input	1.0/1.0	20μA/0.6mA
R/$\overline{W}$	Read/Write input	1.0/1.0	20μA/0.6mA
SI/O	3-State Serial data input or	3.75/1.0	70μA/0.6mA
	3-State Serial output	150/33	3.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

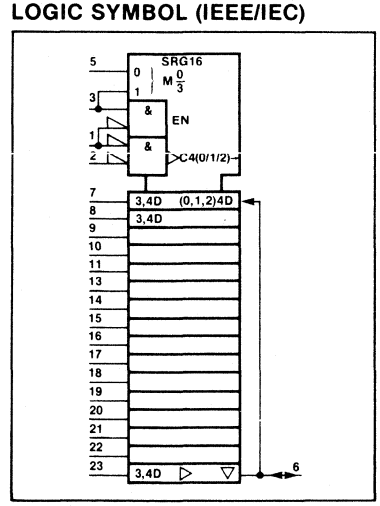
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



16-BIT SHIFT REGISTER — FAST 54/74F674

Preview

Serial Output—the SI/O 3-state buffer is active and the register contents are shifted out from Q_{15} and simultaneously shifted back into Q_0.

Parallel Load—data present on P_0-P_{15} are entered into the register on the falling edge of CP. The SI/O 3-state buffer is active and represents the Q_{15} output.

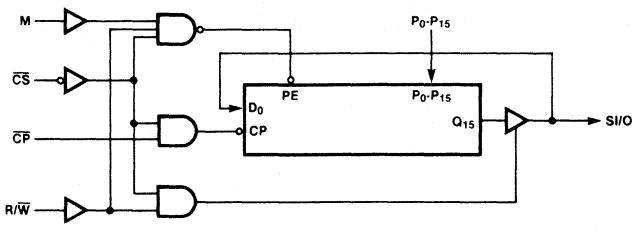
To prevent false clocking, CP must be LOW during a LOW-to-HIGH transition of CS.

Shift Register Operations Table

CONTROL INPUTS				SI/O STATUS	OPERATING MODE
$\overline{CS}$	R/$\overline{W}$	M	$\overline{CP}$		
H	X	X	X	High Z	Hold
L	L	X		Data in	Serial load
L	H	L	↓	Data out	Serial output with recirculation
L	H	H	↓	Active	Parallel load; no shifting

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↓ = HIGH-to-LOW clock transition

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

16-BIT SHIFT REGISTER — FAST 54/74F674

Preview

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 3	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	– 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F674			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	Mil	2.4	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			– 0.73	– 1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V			2	70	μA
I_{OZL}	Off-state output current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			– 2	– 650	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			– 0.4	– 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		– 60	– 80	– 150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH				mA
			I_{CCL} Outputs LOW			80	mA
			I_{CCZ} Outputs OFF				mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Preview

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	140						MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to SI/O	Waveform 1	4.5 5.0	8.0 9.0	11 12.5					ns
t_{PZH} t_{PZL}	Output enable time $\overline{CS}$ or R/$\overline{W}$ to SI/O	Waveform 3 Waveform 4	3.0 3.0	5.0 5.0	7.0 7.0					ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{CS}$ or R/$\overline{W}$ to SI/O	Waveform 3 Waveform 4	3.0 3.0	5.0 5.0	7.0 7.0					ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC SETUP REQUIREMENTS

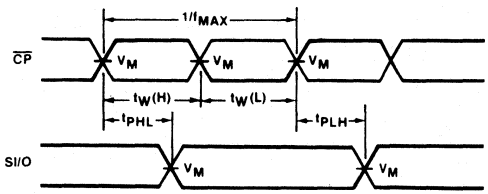
PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW SIO to $\overline{CP}$	Waveform 2	7.0 7.0							ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW SI/O to $\overline{CP}$		0 0							ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW P_n to $\overline{CP}$	Waveform 2	3.0 3.0							ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW P_N to $\overline{CP}$		0 0							ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW R/$\overline{W}$ or $\overline{CS}$ to $\overline{CP}$	Waveform 2	5.0 5.0							ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW R/$\overline{W}$ or $\overline{CS}$ to $\overline{CP}$		0 0							ns
$t_w(H)$ $t_w(L)$	$\overline{CP}$ pulse width, HIGH or LOW	Waveform 1	4.0 5.0							ns

5

Preview

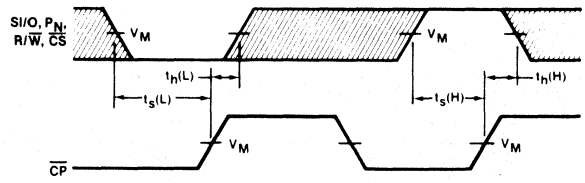
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS
AND CLOCK PULSE WIDTH



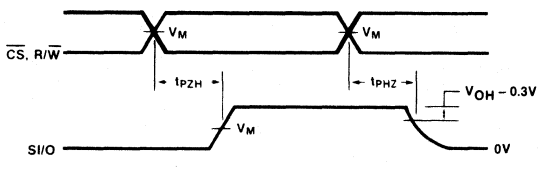
Waveform 1

DATA SETUP AND HOLD TIMES



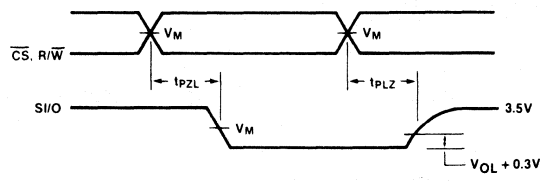
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND
DISABLE TIME FROM LOW LEVEL



Waveform 3

3-STATE ENABLE TIME TO HIGH LEVEL AND
DISABLE TIME FROM HIGH LEVEL



Waveform 4

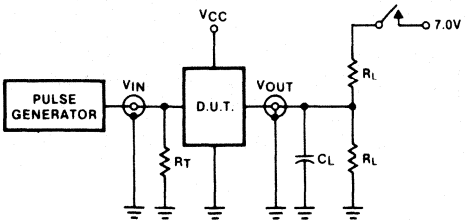
$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

Preview

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



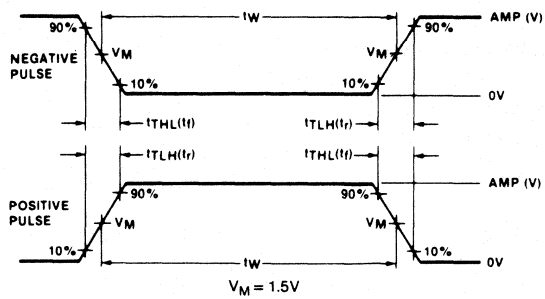
SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

Preview

- Serial-to-parallel converter
- 16-bit serial I/O shift register
- 16-bit parallel-out storage register
- Recirculating parallel transfer
- Expandable for longer words

16-Bit Shift Register (Serial-In/Serial-Parallel Out)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F675		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F675N	
Plastic SO	N74F675D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F675 contains a 16-bit serial-in/serial-out shift register and a 16-bit parallel-out storage register. Separate serial input and output pins are provided for expansion to longer words. By means of a separate clock, the contents of the shift register are transferred to the storage register. The contents of the storage register can also be loaded back into the shift register. A HIGH signal on the Chip Select input prevents both shifting and parallel loading.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F/74F (U.L.) High/Low	LOAD VALUE High/Low
SI	Serial Data Input	1.0/1.0	20μA/0.6mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{SHCP}$	Shift Clock Pulse Input (Active Falling Edge)	1.0/1.0	20μA/0.6mA
STCP	Store Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
R/$\overline{W}$	Read/Write Input	1.0/1.0	20μA/0.6mA
SO	Serial Data Output	50/33	1.0mA/20mA
Q_0–Q_{15}	Parallel Data Outputs	50/33	1.0mA/20mA

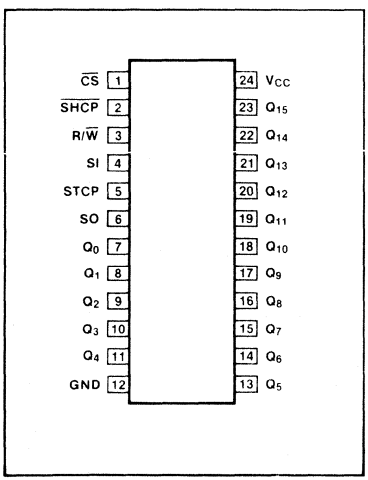
NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

FUNCTIONAL DESCRIPTION

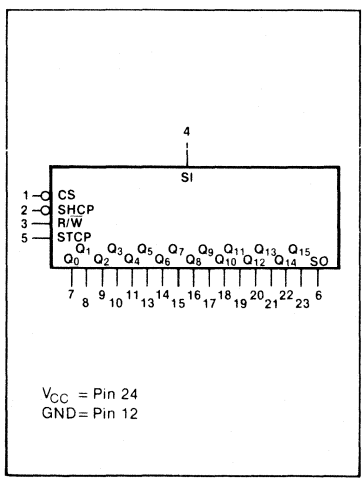
The 16-bit shift register operates in one of four modes, as determined by the signals applied to the Chip Select ($\overline{CS}$), Read/Write (R/$\overline{W}$) and Store Clock Pulse (STCP) inputs. State changes are indicated by the falling edge of the Shift Clock Pulse ($\overline{SHCP}$). In the Shift-right mode, data enters D_0 from the Serial Input (SI) pin and exits from Q_{15} via the Serial Data Output (SO) pin. In the Parallel Load mode, data from the storage register outputs enter the shift register and serial shifting is inhibited.

The storage register is in the Hold mode when either $\overline{CS}$ or R/$\overline{W}$ is HIGH. With $\overline{CS}$ and R/$\overline{W}$ both LOW, the storage register is parallel loaded from the shift register on the rising edge of STCP.

PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

16-BIT SHIFT REGISTER — FAST 54/74F675

Preview

To prevent false clocking of the shift register, $\overline{SHCP}$ should be in the LOW state during a LOW-to-HIGH transition of $\overline{CS}$. To prevent false clocking of the storage register, STCP should be LOW during a HIGH-to-LOW transition of $\overline{CS}$ if R/$\overline{W}$ is LOW, and should also be LOW during a HIGH-to-LOW transition of R/$\overline{W}$ if $\overline{CS}$ is LOW.

SHIFT REGISTER OPERATIONS TABLE

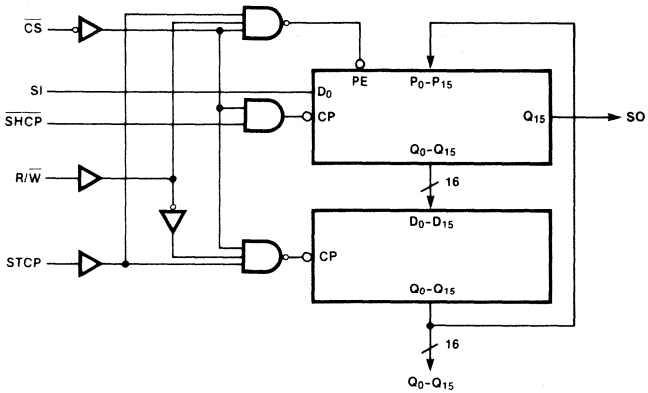
CONTROL INPUTS				OPERATING MODE
$\overline{CS}$	R/$\overline{W}$	$\overline{SHCP}$	STCP	
H	X	X	X	Hold
L	L	↓	X	Sihft Right
L	H	↓	L	Shift Right
L	H	↓	H	Parallel Load; No Shifting

STORAGE REGISTER OPERATIONS TABLE

INPUTS			OPERATING MODE
$\overline{CS}$	R/$\overline{W}$	STCP	
H	X	X	Hold
L	H	X	Hold
L	L	↑	Parallel Load

H = HIGH voltage level
L = LOW voltage level
XX = Don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

FUNCTIONAL BLOCK DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

16-BIT SHIFT REGISTER — FAST 54/74F675

Preview

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	– 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F675			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-60	-80	-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX				160	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F			54F		74F		UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	140						MHz
t_{PLH} t_{PHL}	Propagation delay STCP to Q_n	Waveform 1	7.5 9.5	13 16	18 22					ns
t_{PLH} t_{PHL}	Propagation delay SHCP to SO	Waveform 1	4.5 5.0	8.0 9.0	11 12.5					ns

NOTE
Subtract 0.2ns from minimum values for SO package.

16-BIT SHIFT REGISTER — FAST 54/74F675

Preview

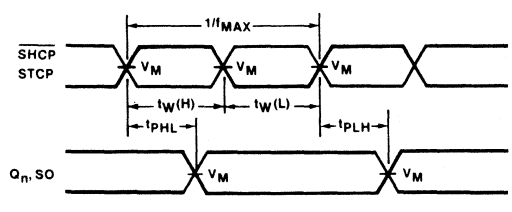
AC SETUP REQUIREMENTS

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ Setup time, HIGH or LOW $t_s(L)$ $\overline{CS}$ or R/$\overline{W}$ to STCP	Waveform 2	7.0 7.0							ns
$t_h(H)$ Hold time, HIGH or LOW $t_h(L)$ $\overline{CS}$ or R/$\overline{W}$ to STCP	Waveform 2	0 0							ns
$t_s(H)$ Setup time, HIGH or LOW $t_s(L)$ SI to $\overline{SHCP}$	Waveform 2	3.0 3.0							ns
$t_h(H)$ Hold time, HIGH or LOW $t_h(L)$ SI to $\overline{SHCP}$	Waveform 2	0 0							ns
$t_s(H)$ Setup time, HIGH or LOW $t_s(L)$ R/$\overline{W}$ or $\overline{CS}$ to $\overline{SHCP}$	Waveform 2	5.0 5.0							ns
$t_h(H)$ Hold time, HIGH or LOW $t_h(L)$ R/$\overline{W}$ or $\overline{CS}$ to $\overline{SHCP}$	Waveform 2	0 0							ns
$t_w(H)$ $t_w(L)$ $\overline{SHCP}$ pulse width, HIGH or LOW	Waveform 1	4.0 5.0							ns
$t_w(H)$ $t_w(L)$ STCP pulse width, HIGH or LOW	Waveform 1	5.0 10							ns

5

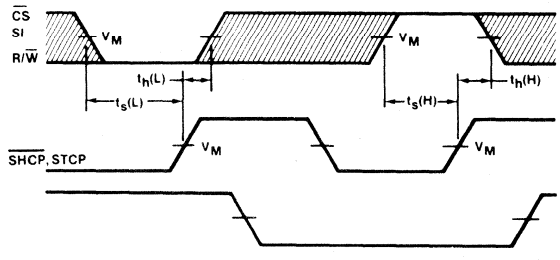
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

DATA SETUP AND HOLD TIMES



Waveform 2

$V_M = 1.5V$

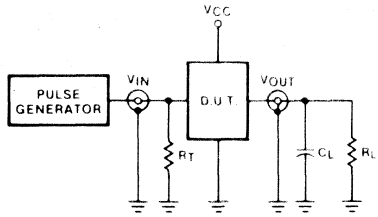
The shaded areas indicate when the input is permitted to change for predictable output performance.

16-BIT SHIFT REGISTER — FAST 54/74F675

Preview

TEST CIRCUITS AND WAVEFORMS

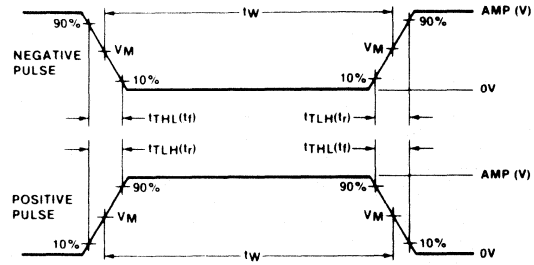
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Preview

'F676 — 16-Bit Shift Register

- **16-bit parallel-to-serial conversion**
- **16-bit serial-in, serial-out**
- **Chip Select control**
- **Power supply current 48mA typical**
- **Shift frequency 110MHz typical**

TYPE	TYPICAL, f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F676	110MHz	48mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F676N	
Plastic SO	N74F676D	
Ceramic DIP		
Ceramic LLCC		

NOTE:
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20μA/0.6mA
SI	Serial Data Input	1.0/1.0	20μA/0.6mA
M	Mode Select Input	1.0/1.0	20μA/0.6mA
D_0-D_{15}	Parallel Data Inputs	1.0/1.0	20μA/0.6mA
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	1.0/1.0	20μA/0.6mA
SO	Serial Data Output	50/33	1mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

DESCRIPTION

The 'F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the Mode (M) input is HIGH, information present on the parallel data (P_0-P_{15}) inputs is entered on the falling edge of the Clock Pulse ($\overline{CP}$) input signal. When M is LOW, data is shifted out of the most significant bit position while information present on the Serial (SI) input shifts into the least significant bit position. A HIGH signal on the Chip Select ($\overline{CS}$) input prevents both parallel and serial operations.

The 16-bit shift register operates in one of three modes, as indicated in the Shift Register Operations Table.

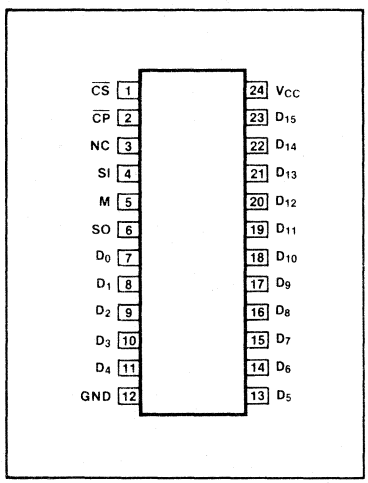
HOLD — a HIGH signal on the Chip Select ($\overline{CS}$) input prevents clocking, and data is stored in the 16 registers.

Shift/Serial Load — data present on the SI pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks, finally appearing on the SO pin.

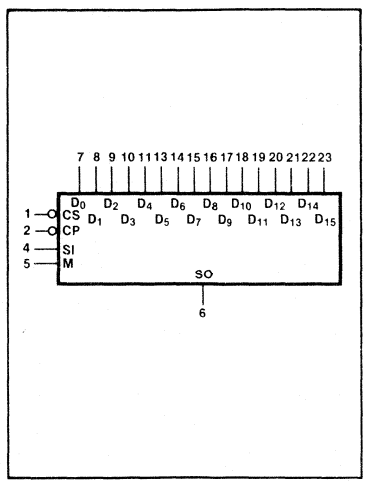
Parallel Load — data present on P_0-P_{15} are entered into the register on the falling edge of $\overline{CP}$. The SO output represents the Q_{15} register output.

To prevent false clocking, $\overline{CP}$ must be LOW during a LOW-to-HIGH transition of $\overline{CS}$.

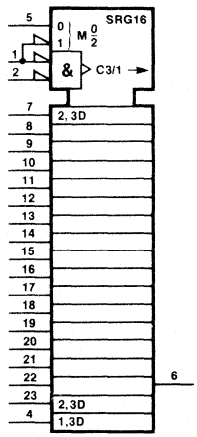
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTER — FAST 54/74F676

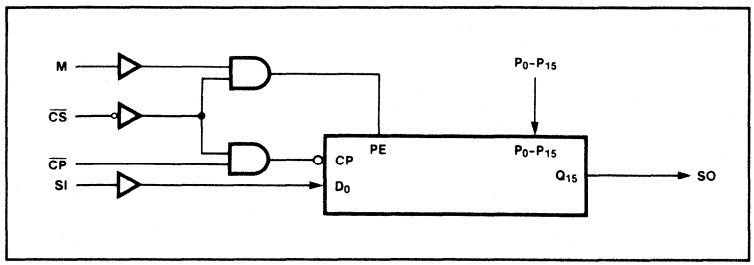
Preview

FUNCTION TABLE

CONTROL INPUT			OPERATING MODE
$\overline{CS}$	M	$\overline{CP}$	
H	X	X	Hold
L	L	↓	Shift/Serial Load
L	H	↓	Parallel Load

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↓ = HIGH-to-LOW clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

SHIFT REGISTER — FAST 54/74F676

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F676 Min	54/74F676 Typ[2]	54/74F676 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			− 0.73	− 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			− 0.4	− 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		− 60	− 80	− 150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			48	72	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

5

PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	110				90		MHz
t_{PLH} t_{PHL}	Propagation delay, $\overline{CP}$ to SO	Waveform 1	4.5 5.0	9.0 9.0	11 12.5			4.5 5.0	12 13.5	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

SHIFT REGISTER — FAST 54/74F676

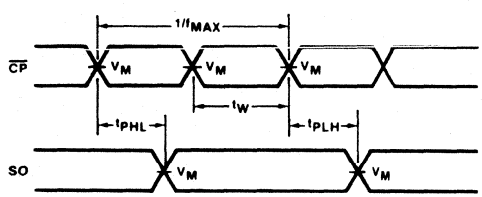
Preview

AC SETUP REQUIREMENTS

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_s (H) Setup time, HIGH or LOW t_s (L) SI to $\overline{CP}$	Waveform 2	4.0 4.0						4.0 4.0	ns
t_h (H) Hold time, HIGH or LOW t_h (L) SI to $\overline{CP}$	Waveform 2	4.0 4.0						4.0 4.0	ns
t_s (H) Setup time, HIGH or LOW t_s (L) D_n to $\overline{CP}$	Waveform 2	3.0 3.0						3.0 3.0	ns
t_h (H) Hold time, HIGH or LOW t_h (L) D_n to $\overline{CP}$	Waveform 2	4.0 4.0						4.0 4.0	ns
t_s (H) Setup time, HIGH or LOW t_s (L) M to $\overline{CP}$	Waveform 2	4.0 6.5						4.5 7.5	ns
t_h (H) Hold time, HIGH or LOW t_h (L) M to $\overline{CP}$	Waveform 2	0 2.0						0 2.0	ns
t_s (L) Setup time, LOW $\overline{CS}$ to $\overline{CP}$	Waveform 2	10.0						10.0	ns
t_h (H) Hold time, HIGH $\overline{CS}$ to $\overline{CP}$	Waveform 2	10.0						10.0	ns
t_w (H) $\overline{CP}$ pulse width t_w (L) HIGH or LOW	Waveform 2	4.0 6.0						4.0 6.0	ns

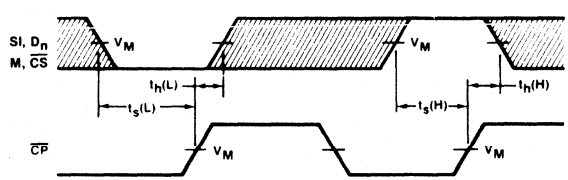
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

DATA SETUP AND HOLD TIMES



Waveform 2

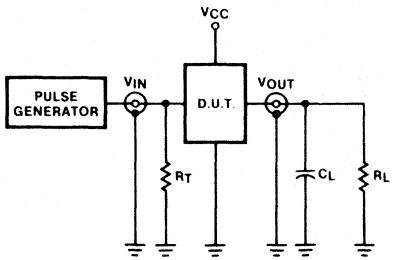
$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

Preview

TEST CIRCUITS AND WAVEFORMS

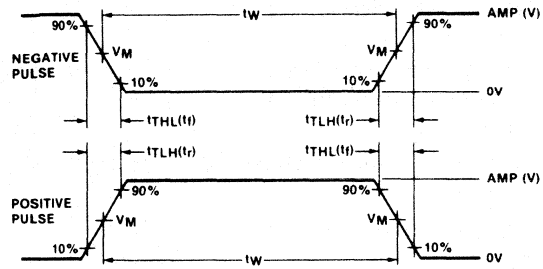
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

8-BIT COUNTER — FAST 54/74F779

Preview

8-Bit Bidirectional Binary Counter (3-State)

- **High impedance NPN base input for reduced loading (20μA with HIGH and LOW states)**
- **Multiplexed 3-state I/O ports**
- **Built-in lookahead carry capability**
- **Count frequency 100MHz typical**
- **Supply current 80mA typical**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F779	100MHz	70mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F779N	
Plastic SO	N74F779D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

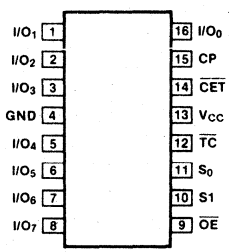
The 'F779 is a fully synchronous 8-stage up/down counter with multiplexed 3-state I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins (S_0, S_1). The device also features carry lookahead for easy cascading. All state changes are initiated by the rising edge of the clock.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

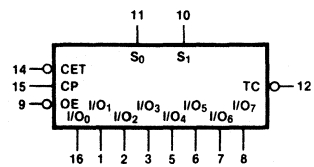
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
I/O_0–I/O_7	Data Inputs	1.0/0.033	20μA/20μA
	Data Outputs	150/33	3mA/20mA
S_0, S_1	Select Inputs	1.0/0.033	20μA/20μA
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/0.033	20μA/20μA
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	1.0/0.033	20μA/20μA
CP	Clock Pulse Input (Active Rising Edge)	1.0/0.033	20μA/20μA
$\overline{TC}$	Terminal Count Output (Active LOW)	150/33	3mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION



LOGIC SYMBOL



V_{CC} = Pin 13
GND = Pin 4

LOGIC SYMBOL (IEEE/IEC)

8-BIT COUNTER FAST 54/74F779

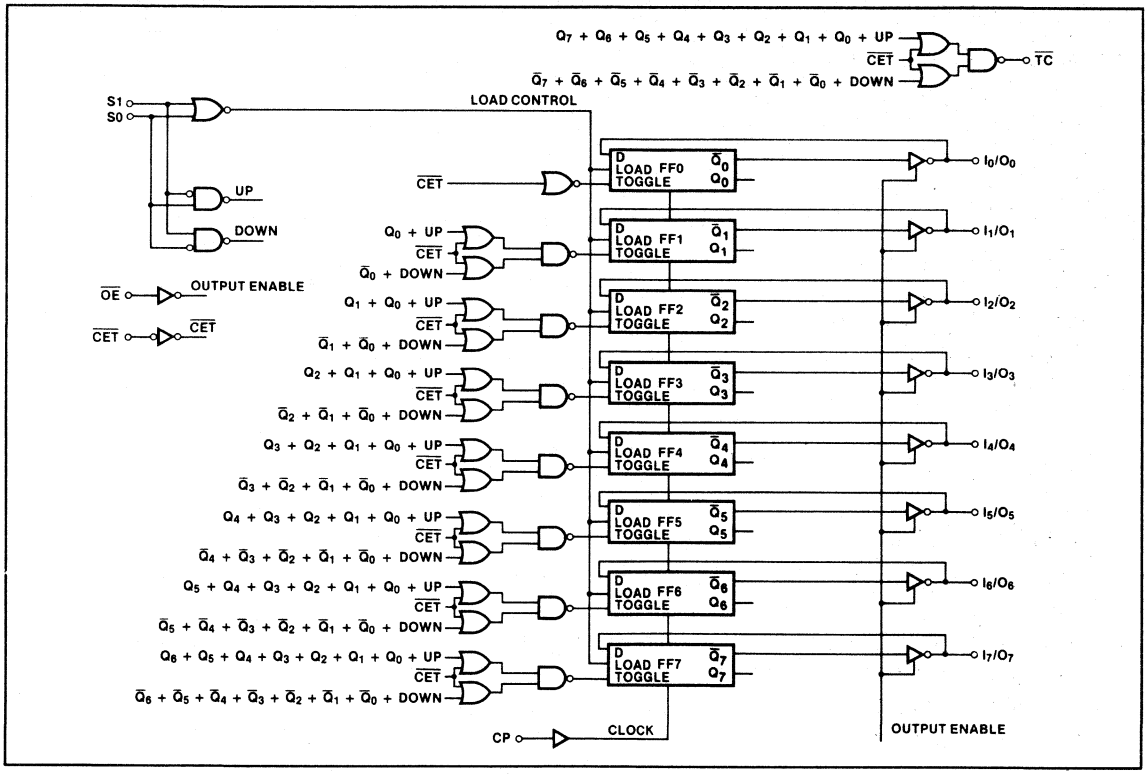
Preview

FUNCTION TABLE

S1	S0	$\overline{CET}$	$\overline{OE}$	CP	
X	X	X	H	X	I/Oa to I/Oh in HIGH Z
X	X	X	L	X	Flip-flop outputs appear on I/O lines
L	L	X	X		Parallel load all flip-flops
(not LL)		H	X		Hold ($\overline{TC}$ held HIGH)
H	H	X	X		Hold
H	L	L	X		Count up
L	H	L	X		Count down

H = HIGH voltage level
L = LOW voltage level
X = Don't Care
not LL means S0 and S1 should never both be LOW level at the same time.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

8-BIT COUNTER — FAST 54/74F779

Preview

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 3	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	– 55		125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74F779			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4			V
				Com'l	2.7			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 0.73	– 1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V				2	50	μA
I_{OZL}	Off-state output current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				– 2	– 50	μA
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				0.75	1.0	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				10	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				– 0.1	– 20	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 60	– 115	– 150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		50	70	mA
			I_{CCL}	Outputs LOW		80	100	mA
			I_{CCZ}	Outputs Disabled		80	100	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

8-BIT COUNTER FAST 54/74F779

Preview

AC ELECTRICAL CHARACTERISTICS

When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100				70		MHz
t_{PLH} t_{PHL}	CP to I/O_n CP to I/O_n	Waveform 1	3.0 4.5					2.5 4.0		ns
t_{PLH} t_{PHL}	$\overline{CET}$ to $\overline{TC}$ CP to $\overline{TC}$	Waveform 1	6.0 5.0					5.0 4.0		ns
t_{PZH} t_{PZL}	Output Enable Time	Waveform 3 Waveform 4	12 12					10 10		ns
t_{PHZ} t_{PLZ}	Output Disable Time	Waveform 3 Waveform 4	12 12					10 10		ns

NOTE
Subtract 0.2ns from minimum values for SO package.

AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_s (H) t_s (L)	Data to CP Data to CP	Waveform 2	5.0 5.0					5.0 5.0		ns
t_h (H) t_h (L)	Data to CP Data to CP	Waveform 2	0 0					0 0		ns
t_s (H) t_s (L)	$\overline{OE}$ to CP $\overline{OE}$ to CP	Waveform 2	12 12					12 12		ns
t_h(H) t_h(L)	$\overline{OE}$ to CP $\overline{OE}$ to CP	Waveform 2	0 0					0 0		ns
t_s (H) t_s (L)	CET to CP CET to CP	Waveform 2	10 10					10 10		ns
t_h(H) t_h(L)	CET to CP CET to CP	Waveform 2	0 0					0 0		ns
t_w (H)	Clock pulse width	Waveform 1	5					6		ns

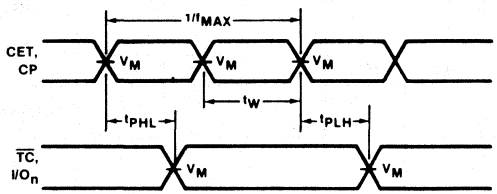
5

8-BIT COUNTER FAST 54/74F779

Preview

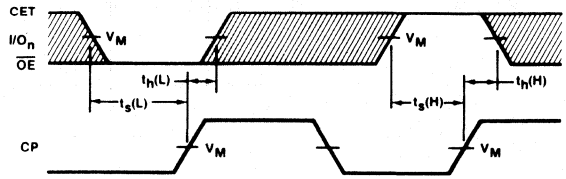
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



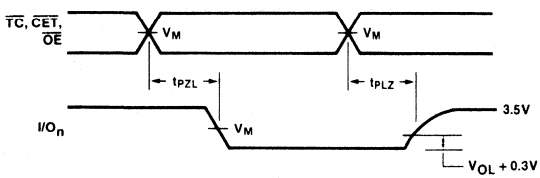
Waveform 1

DATA SETUP AND HOLD TIMES



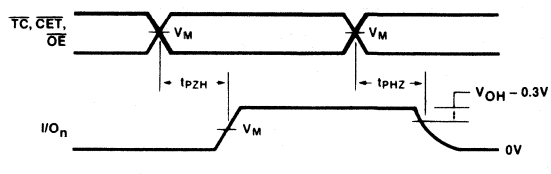
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL

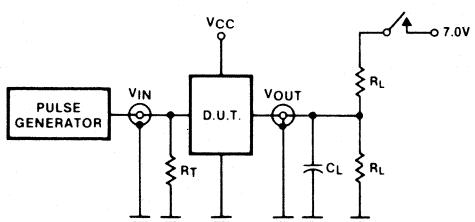


Waveform 4

$V_M = 1.5V$

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



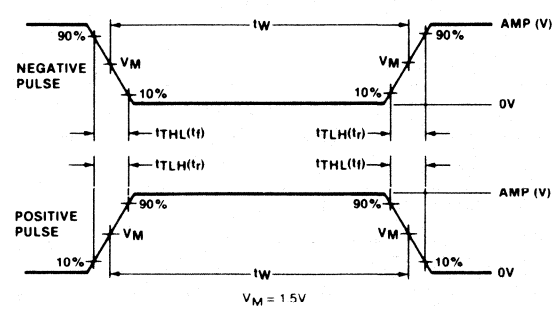
SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

MULTIPLIER FAST 54/74F784

Preview

8-Bit Serial/Parallel Multiplier (With Adder/Subtractor)

- **Two's complement multiplication**
- **Cascadable for any number of bits**
- **Full Adder and B – 1 input included for maximum flexibility**
- **Maximum clock frequency 50MHz guaranteed**
- **Supply current 100mA max**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F784		76mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F784N	
Plastic SO	N74F784D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

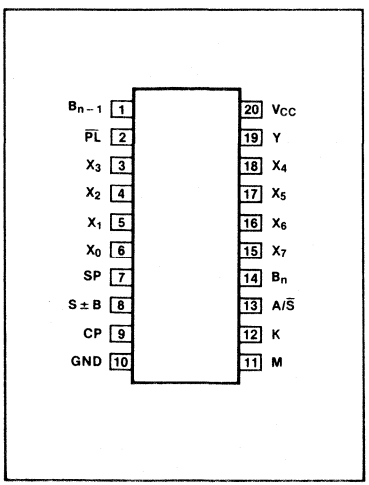
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
X_0-X_7	Multiplicand Data Inputs	1.0/1.0	20μA/0.6mA
Y	Serial Multiplier Input	1.0/1.0	20μA/0.6mA
CP	Clock Pulse Input	1.0/1.0	20μA/0.6mA
K	Serial Expansion Input	1.0/1.0	20μA/0.6mA
M	Mode Control Input	1.0/1.0	20μA/0.6mA
$\overline{PL}$	Parallel Load Input	1.0/2.0	20μA/1.2mA
A/$\overline{S}$	Add/Subtract Input	1.0/1.0	20μA/0.6mA
B_n	Serial B Input	1.0/1.0	20μA/0.6mA
B_{n-1}	Delayed Serial B Input	1.0/1.0	20μA/0.6mA
SP	Serial X•Y Product Output	50/33.3	1mA/20mA
S ± B	Serial Y•Y ± B Output	50/33.3	1mA/20mA

One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

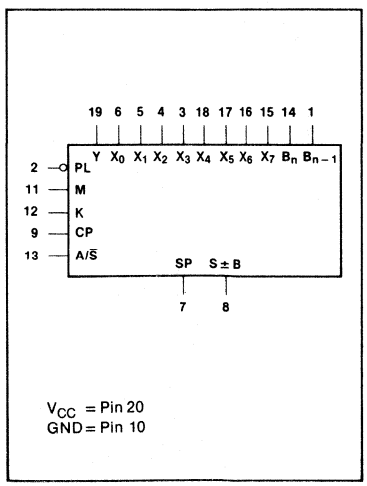
DESCRIPTION

The 'F784 is a serial n × 8-bit multiplier with a final stage adder/subtractor for optional use in adding a B bit to obtain S ± B. A 'B – 1' bit can also be added via an internal flip-flop to achieve a 1-bit delay. The X word is parallel loaded (8 bits wide) into latches and the Y word is clocked in serially from a shift register. The 'F784 is particularly useful for high-speed digital filtering or butterfly networks in fast Fourier transforms.

PIN CONFIGURATION



LOGIC SYMBOL



5

MULTIPLIER FAST 54/74F784

Preview

The 'F784 is a serial/parallel 8-bit multiplier. Also included is an adder/subtractor stage. The X word (multiplicand) is loaded into a register while simultaneously clearing the arithmetic cell flip-flops in preparation for a multiplication. The Y word (multiplier) is clocked in serially.

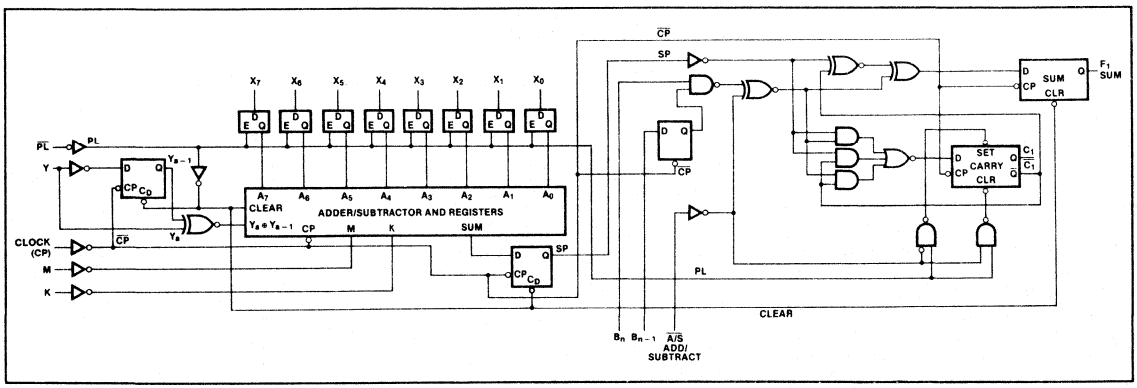
Expansion capability is provided via the M and K inputs. The K (cascade) input is connected to the SO output of the more significant chip. The M (mode) input is used to determine whether the multiplicand is to be treated as a two's complement or unsigned number.

The 'F784 has logic to enable complex arithmetic to be performed. A serial adder/subtractor enables constants to be added to the product. Typically, this feature would be used in FFT butterfly networks to reduce package count and power.

Two outputs are provided; the product X•Y and the product X•Y ± B. Because of the internal adder/subtractor, a speed advantage is gained when using the 'F784 over using a separate adder and multiplier chip.

During a multiplication operation, the first clock cycle is used to load both the X word (multiplicand) and the first bit of the Y word (operand) into the input registers. At this time there is no valid data at the SP output, so that B bits added will not give the correct sum output. In order to load the first B bit on the same clock as X and Y, a B_{n-1} input is provided which delays the B data by one clock cycle. Thus, a valid output results.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	54F	74F	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature	Mil	− 55		125	°C
		Com'l	0		70	°C

MULTIPLIER FAST 54/74F784

Preview

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F784 Min	54/74F784 Typ[2]	54/74F784 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			– 0.73	– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	PL			– 1.2	mA
			Others		– 0.4	– 0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		– 60	– 80	– 150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			76	100	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	54/74F: T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			54F: T_A, V_{CC} Mil, C_L = 50pF, R_L = 500Ω		74F: T_A, V_{CC} Com'l, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	50					50		MHz
t_{PHL}	Propagation delay $\overline{PL}$ to SP	Waveform 2	6		13			5	14.5	ns
t_{PHL}	Propagation delay $\overline{PL}$ to S ± B	Waveform 2	5.5		12			4.5	13.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to SP	Waveform 1	4 4.5		9 10.5			3.5 4	10 12	ns
t_{PLH} t_{PHL}	Propagation delay CP to S ± B	Waveform 1	4 4		9 9			3.5 3.5	10 10	ns

NOTE
Subtract 0.2ns from minimum values for SO package.

5

MULTIPLIER FAST 54/74F784

Preview

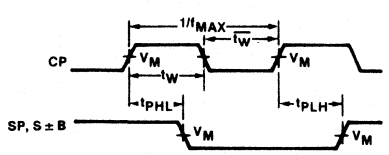
AC SETUP REQUIREMENTS

PARAMETER		TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time K to CP	Waveform 3	13 9					11.5 8		ns
$t_h(H)$ $t_h(L)$	Hold time K to CP	Waveform 3	0 1					0 0.5		ns
$t_s(H)$ $t_s(L)$	Setup time Y to CP	Waveform 3	15 15					13 13		ns
$t_h(H)$ $t_h(L)$	Hold time Y to CP	Waveform 3	1.5 1.5					1 1		ns
$t_s(H)$ $t_s(L)$	Setup time X_3 to $\overline{PL}$	Waveform 3	5 5					4 4		ns
$t_h(H)$ $t_h(L)$	Hold time X_3 to $\overline{PL}$	Waveform 3	2 2					1.5 1.5		ns
$t_s(H)$ $t_s(L)$	Setup time B_n to CP	Waveform 3	7 7					6 6		ns
$t_h(H)$ $t_h(L)$	Hold time B_n to CP	Waveform 3	0 0					0 0		ns
$t_s(H)$ $t_s(L)$	Setup time A/$\overline{S}$ to CP	Waveform 3	12 12					10.5 10.5		ns
$t_h(H)$ $t_h(L)$	Hold time A/$\overline{S}$ to CP	Waveform 3	1.5 1.5					1 1		ns
$t_s(H)$ $t_s(L)$	Setup time B_n to CP	Waveform 3	4 4					3.5 3.5		ns
$t_h(H)$ $t_h(L)$	Hold time B_n to CP	Waveform 3	0 0					0 0		ns
t_{rec}	Recovery time $\overline{PL}$ to CP	Waveform 2	6.5					5.5		ns
$t_W(L)$	Pulse width		5					4		ns
$t_W(H)$ $t_W(L)$	CP pulse width	Waveform 1	5 5					4 4		ns

Preview

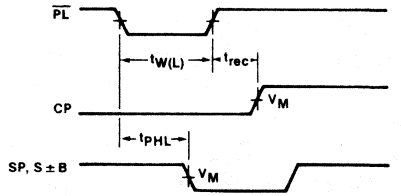
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



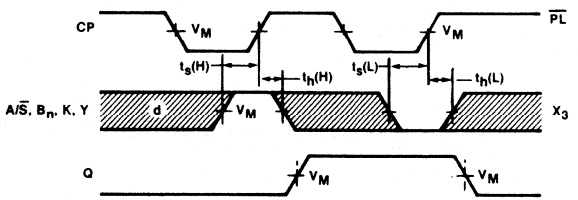
Waveform 1

PARALLEL LOAD PULSE WIDTH, PARALLEL LOAD TO OUTPUT DELAY AND PARALLEL LOAD TO CLOCK RECOVERY TIME



Waveform 2

DATA SETUP AND HOLD TIMES



$V_M = 1.5V$

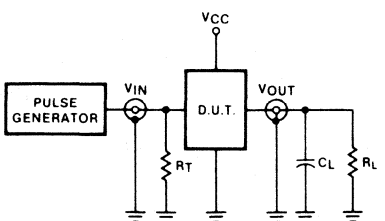
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 3

5

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



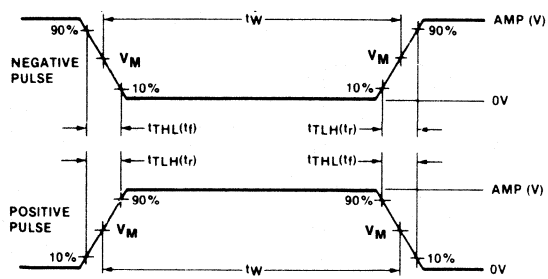
DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

TRANSMISSION LINE DRIVER FAST 54/74F3037

Preliminary

Quad 2-Input 30Ω Transmission Line Driver

- 30Ω transmission line driver
- 160mA output drive capability
- High speed
- Facilitates Incident wave switching
- 2nh lead inductance each on V_{CC} and Gnd when both side pins are used

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F3037	ns	mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F3037N	

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

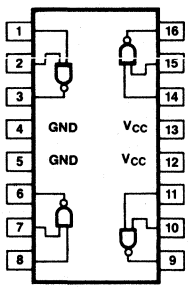
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

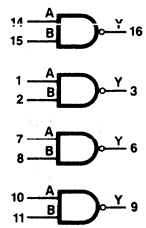
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A, B	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	2500/267	50mA/160mA

One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

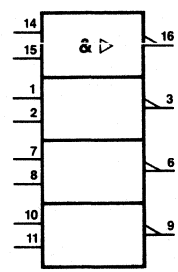
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



TRANSMISSION LINE DRIVER FAST 54/74F3037

Preliminary

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state		320	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−50	mA
I_{OL}	LOW-level output current			160	mA
T_A	Operating free-air temperature	0		70	°C

5

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F3037			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX	Mil				V
			Com'l		0.5	0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	2	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−100		−225	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		3.5	4	mA
			I_{CCL} Outputs LOW		26	34	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH}, V_{IH} = GND; I_{CCL}, V_{IN} = Open.

TRANSMISSION LINE DRIVER FAST 54/74F3037

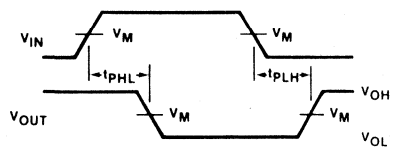
Preliminary

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F			54F		74F		UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1	2.4	3.7	5.0	2.0	7.0	2.4	6.0	ns
t_{PHL} Propagation delay	Waveform 1	1.5	3.2	4.3	1.5	6.5	2.0	6.0	ns

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS

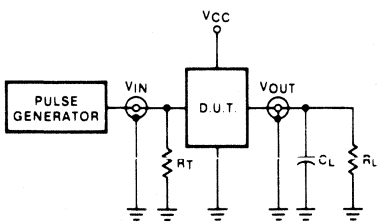


$V_M = 1.5V$

Waveform 1

TEST CIRCUITS AND WAVEFORMS

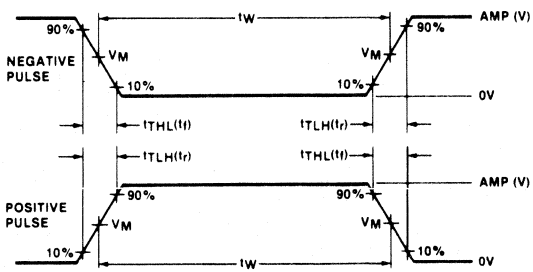
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

TRANSMISSON LINE DRIVER FAST 54/74F3040

Preliminary

Dual 4-Input 30Ω Transmission Line Driver

- **30Ω transmission line driver**
- **160mA output drive capability**
- **High speed**
- **Facilitates Incident wave switching**
- **2nh lead inductance each on V_{CC} and Gnd when both side pins are used**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F3040	ns	mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F3040N	

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

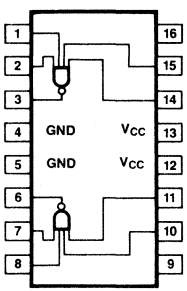
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
A, B, C, D	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	2500/267	50mA/160mA

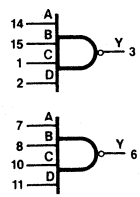
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

5

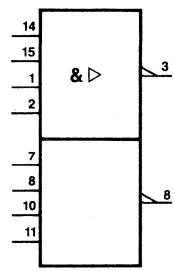
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



TRANSMISSION LINE DRIVER FAST 54/74F3040

Preliminary

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state		320	mA
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−50	mA
I_{OL}	LOW-level output current			160	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F3040			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX I_{OL} = MAX	Mil				V
			Com'l		0.5	0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	2	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−100		−225	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		1.72	2	mA
			I_{CCL} Outputs LOW		13.2	17	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH}, V_{IH} = GND; I_{CCL}, V_{IN} = Open.

TRANSMISSION LINE DRIVER FAST 54/74F3040

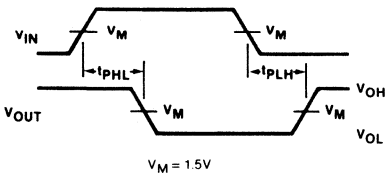
Preliminary

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	54/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			54F T_A, V_{CC} Mil $C_L = 50pF$ $R_L = 500\Omega$		74F T_A, V_{CC} Com'l $C_L = 50pF$ $R_L = 500\Omega$		UNIT
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1	2.5 2.0	4.4 3.1	6.0 4.5	2.5 2.0	8.0 6.5	2.5 2.0	7.0 5.5	ns

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS

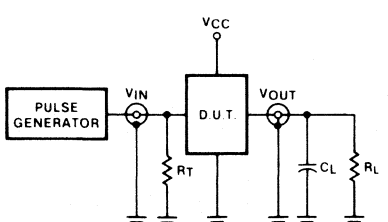


$V_M = 1.5V$

Waveform 1

TEST CIRCUITS AND WAVEFORMS

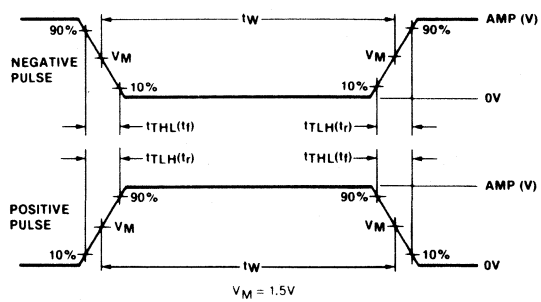
TEST CIRCUIT FOR TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE DEFINITIONS



$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74F	3.0V	1MHz	500ns	2.5ns	2.5ns

5

Section 6
FAST Application Notes

USING FAST LOGIC FUNCTIONS IN MICROPROCESSOR SYSTEMS — APP NOTE 201

ABSTRACT

The development of commercially available oxide-isolated TTL logic devices has significantly improved the traditional speed/power figures achievable in TTL families. One of these oxide-isolated families, FAST[1], has become a broad-based product line offering performance characteristics ideal for many microprocessor systems. The small geometries associated with oxide-isolation are making complex functions possible with very high-speed and low-power characteristics.

HIGH-SPEED TTL LOGIC

The basic circuitry used for TTL Logic has evolved over a period of 15 years and arrived at a set of designs that are optimized for the junction-isolated processing technology currently in use. These circuits have produced two separate families—one driven to high-speed and the other to low power. While the subject of this paper is primarily concerned with the high-speed segment of the TTL marketplace, many of the remarks apply equally to the low-power segment as well.

With today's circuitry the speed of the devices are fixed primarily by the node capacitance of the device junctions. Taking a simplistic view of the matter, the speed of the device is tied to junction capacitance by the rule of RC time constants. This allows the speed of a function to be changed by varying the resistor sizes—the smaller the resistor, the faster the device. Of course there are practical limits to how small the resistors may be made without introducing other, more serious problems. Using the smallest practical resistor size creates a family which is basically the current Schottky family of high-speed logic.

Reducing the resistor sizes to increase speed also increases the power dissipation. Any Schottky logic device consumes about nine times more power than the equivalent device in low-power Schottky. Trying to run faster than this dissipates much, much more power and introduces other, very undesirable phenomenon. Short-circuit protection, for instance, is fixed by the size of the output resistor. Input loading is also a function of resistor size—as resistors get very small, the input LOW requirements get large, which introduces other problems into the circuit. By placing the resistor sizes where they are, the family achieves the highest practical speed—even so, problems such as I_{CC} spiking become large and require extensive capacitive decoupling on the board.

Traditional Schottky TTL also suffers from low input breakdown voltages—on the order of 5.5-6.5V. This low value occurs because the input of the device is connected to the base of the input transistor and the user sees the normal base emitter breakdown voltage. This requires that the user guard against positive overshoots in excess of the supply voltage. It also requires that unused inputs be tied to V_{CC} through pull-up resistors rather than connected directly to the supply.

All of these disadvantages are not lost on the marketplace. In fact, Schottky TTL has tended to be a fairly narrow product line with only about one third of the types that exist in the Low-Power Schottky family. One of the reasons for this is that the high power dissipation limits the complexity of the available types. But the primary reason is the power itself. With a nine to one penalty paid for the high speed of Schottky (over Low-Power Schottky), users have been reluctant to use Schottky anywhere but in the most critical circuit paths.

OXIDE ISOLATION

For some time it has been clear to both manufacturers and users that a processing breakthrough was needed if the traditional speed-power curves of LS/S were ever to be changed. That breakthrough occurred with the advent of oxide isolation. In this process, transistors and other active devices are isolated from each other, not by a reverse biased junction, but by an actual channel of oxide. This dramatically reduces the size of the devices which in turn reduces their associated capacitances.

Reducing the capacitances has a direct effect on the speed/power product of the family. Because the capacitances of oxide-isolated devices are far less than corresponding Schottky capacitances, the resistors may be made larger and still produce RC time constants smaller than those of Schottky. As the resistors become larger, the power dissipation is decreased, I_{CC} spiking is reduced, input current is lowered, and a whole new family is created. In addition, the combination of smaller geometries and lower power allows much more complex devices to be fabricated with commercially-acceptable yields, and hence market prices. Thus, the resulting logic devices offer speed in excess of that from current Schottky devices, much lower power, and the promise of higher complexity due to smaller geometries and relaxed power constraints.

FAST — ADVANCED SCHOTTKY TTL

One such implementation of an oxide-isolated TTL familiy is FAST, a family optimized for high speed with moderate power consumption (see Figure 1). In this family, the resistor sizes have been increased by about a factor of four, while the speed has been increased by about 30% over Schottky. This seeming contradiction has been brought about by a tremendous decrease in junction capacitance (see Table 1) which has allowed the resistor sizes to be increased. As a result, FAST devices in general require four times less power than their Schottky equivalents. In fact, the user pays only a two-to-one power penalty for the ultra-high speed of FAST relative to low-power Schottky. The basic parameters of the family comparing FAST, S, and LS are shown in Table 2.

Table 1. Process Comparison

	FP4 ORIGINAL S & LS	HS-I NEW S & LS	HS-II FAST TTL
Size of Min. Trans	$37 \times 51\mu$	$28 \times 40\mu$	$17 \times 35\mu$
Area	$1887\mu^2$	$1120\mu^2$	$505\mu^2$
F_T	4GHz	5GHz	7GHz
Line Resolution	3 microns	3 microns	2 microns
Normalized Capacitance			
Collector — Base	x2	—	x1
Base — Emitter	x4	—	x1
Collector — Substrate	x6	—	x1
Metal — Substrate	x10	—	x1

[1]FAST is a trademark of Fairchild Camera and Instrument Corporation.

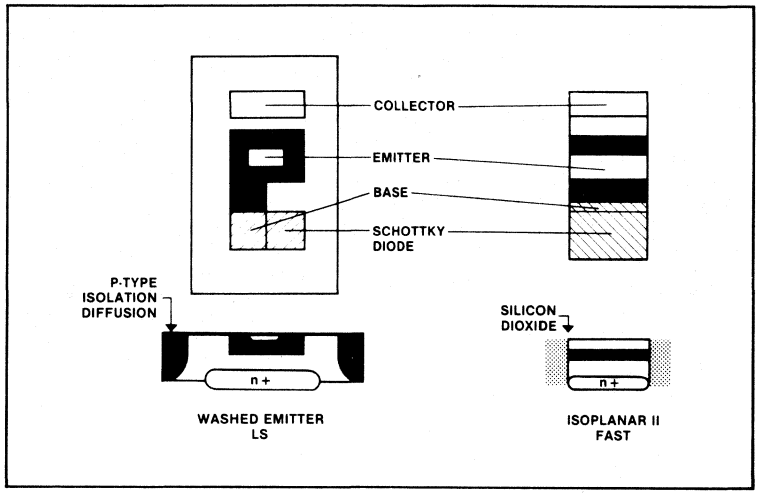


Figure 1. Oxide Isolation Brings on New, Smaller Geometrics

Table 2. Family Comparison

	FAST 74F00	74S00	74LS00
PD (mW/gate)	32.5mW	130mW	15.0mW
t_{PHL}	3.6ns	5.0ns	15ns
t_{PLH}	3.9ns	4.5ns	15ns

NOTE
Propagation delays are all shown at V_{CC} = +5.0V, T_A = 25°C and C_L = 15pF for comparison purposes. FAST is normally guaranteed from 4.75V-5.25V, 0°-70°C, and C_L = 50pF.

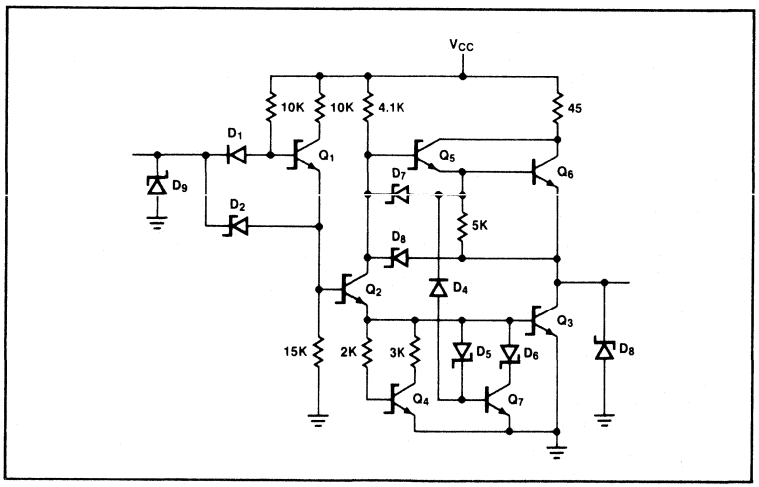


Figure 2. The Basic Fast Gate

The basic FAST gate schematic is shown in Figure 2. It will be seen that the threshold of the device is basically set by two VBEs, or about 1.6V at room temperature. This is considerably better than Schottky, with a threshold of about 1.3V, or Low Power Schottky with its even lower threshold of 0.95V. Thus the FAST circuitry presents the user with about 0.6V more noise immunity than LS. See Figure 3.

The squaring circuit made up of Q4 in the emitter circuit of the phase splitter Q2 is used to pull charge from the base of Q3 during a LOW to HIGH transition. Q4 is turned ON faster than output transistor Q3 can be turned OFF—it pulls the base of Q3 about 100mV below the turn-on point and serves to pull charge from the base of Q3 to speed the transition. A similar function, though basically an AC phenomenon is provided by the "Miller-Killer" circuitry made up of Q7 and diodes D4-D6. Again during the LOW to HIGH transition, stored charge on D4 (acting here as a capacitor) provides a sharp pull-down on the base of Q3. This occurs for a very brief period, a couple of nanoseconds, but serves to kill the I_{CC} spike that would normally appear here. For instance at 0°C, the spike with the "Miller-Killer" in place is only 1.1mA peak—without the "Miller-Killer" the peak I_{CC} reaches 3.3mA, three times larger. During the HIGH to LOW transition, a kicker diode, D3, uses charge stored in the external load capacitance to drive through Q2 into the base of Q3 and turn ON the Q3 output transistor faster. All of these circuits are aimed at increasing the speed of the transitions without unduly increasing the I_{CC} spiking phenomenon.

Both the inputs and outputs of the FAST devices are clamped to prevent negative overshoots from damaging the part. In addition, the diode input structure offers an inherently high breakdown voltage, 15V-20V, as opposed to typically 6V for normal Schottky inputs.

The larger resistors and multiple stages of gain in the FAST circuits allow much smaller input currents. In fact, the basic FAST input requires only 0.6mA max, which is about three times less than the standard Schottky input. When this is combined with the 20mA sink capability of the output stage, an effective family fanout of 33 is achieved. The low input currents also allow low-power Schottky outputs to drive over 10 FAST inputs to the commercial specs. This is a vast improvement over the LS-S fanout interface which is limited by the 2mA Schottky input currents to an effective fanout of only 4 (see

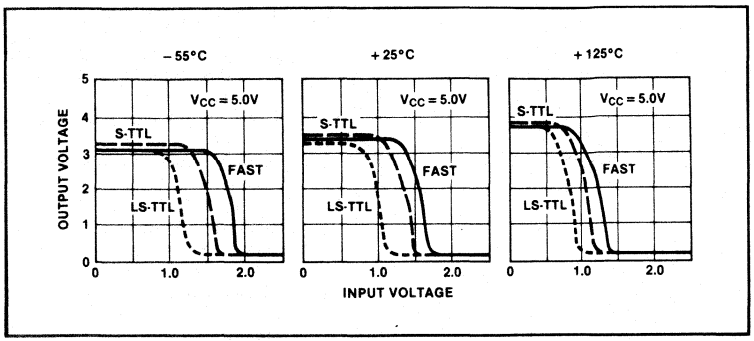


Figure 3. Higher Threshold Levels for Improved Noise Immunity

PARAMETER	FAST	S	LS
Input HIGH Current, I_{IH}	20μA	50μA	20μA
Input HIGH Current, I_I	100μA@7V	1mA@5.5V	100μA@10V
Input LOW Current, I_{IL}	0.6mA	2mA	0.4mA

Figure 4. Reduced Input Currents

PARAMETER		FAST	S	LS
OUTPUT SOURCE CURRENT, I_{OH}		1 mA	1 mA	0.4 mA
OUTPUT SINK CURRENT, I_{OL}		20 mA	20 mA	8 mA
(BUFFER) I_{OL}		(64 mA)	(64 mA)	(24 mA)
OUTPUT SHORT CIRCUIT, I_{OS}				
STANDARD	MAX	150 mA	100 mA	100 mA
	MIN	60 mA	40 mA	20 mA
BUFFERS	MAX	225 mA	225 mA	100 mA
	MIN	100 mA	50 mA	30 mA

Figure 5. Output Drive Capability

Figures 4 and 5). Certain FAST part types are now available with NPN base input structures which reduce input LOW current requirements by a factor of 30—from a 0.6mA family standard to 20μA. Thus, fanout can be increased by a factor of 30 in certain applications.

The three stages of gain provide another advantage—high isolation between outputs and inputs. In the past, some of the early LS flip-flops coupled negative spikes on the outputs back to the inputs and could latch into the wrong state. The high isolation provided by the extra stage of gain eliminates this problem.

The original TTL specifications were driven by a combination of the user's needs and the availability of test equipment. This led to a situation where DC specifications were guaranteed over the combination of worst case supply voltage and temperature, but the AC propagation delays were only guaranteed at a nominal supply voltage and at room temperature. As a result, users were forced to derate the AC performance of the parts to guarantee operation under real-life conditions. Furthermore, AC performance was normally only specified with a load of 15pF, which is unrealistic for many applications.

As test equipment has become more sophisticated, manufacturers now have the ability to guarantee devices for AC performance over the same ranges as the DC parameters—namely across the supply range and temperature range simultaneously. In addition, the load capacitance for these tests has been increased to a more realistic 50pF. This has resulted in reduced special testing by customers and manufactures alike (see Figure 6).

USING FAST WITH MICROPROCESSOR SYSTEMS

FAST has already become a wide product line consisting of over 120 circuit types.

SSI	18 TYPES
MSI	67 TYPES
OCTALS	22 TYPES
ERROR COR/DET	9TYPES
MEMORIES AND MEM-CONTROL	4 TYPES

The same features that make FAST attractive to the general marketplace are particularly interesting to designers of microprocessor based systems. Over 60% of the FAST types planned for the Signetics FAST product line are aimed at these types of systems. They are characterized by the heavy use of octals and specialized memory control and error detecting and correcting functions. We will now explore some of the devices planned for this family.

In the category of octals, all of the popular 74F240, F241, F244, and F245 buffers and transceivers are available. In addition, some of the newer types such as the 74F620 through the 'F623 offer transceiver functions with slightly different control signals that are more closely suited to the control signals present in most microprocessor systems.

Seventeen octal latches are also planned for the family. These include the popular 74F373, 'F374, 'F533, and 'F534. However additional functions with other capabilities are also being added to the family. The 'F604-'F605 are classified here as octals, although they actually contain sixteen latches—the outputs of those latches are multiplexed to eight outputs. These are ideal for applications such as storing memory addresses which are then multiplexed into separate row and column addresses for dynamic memories. Another use would be for interfacing sixteen-bit processors to eight-bit memories or peripherals. The 'F646, 'F647, 'F648, and 'F649 are dual 8-bit latches with bidirectional inputs and outputs that are ideal for transferring data from one bus to a second, asynchronous bus. Because all of the control signals for each set of latches are

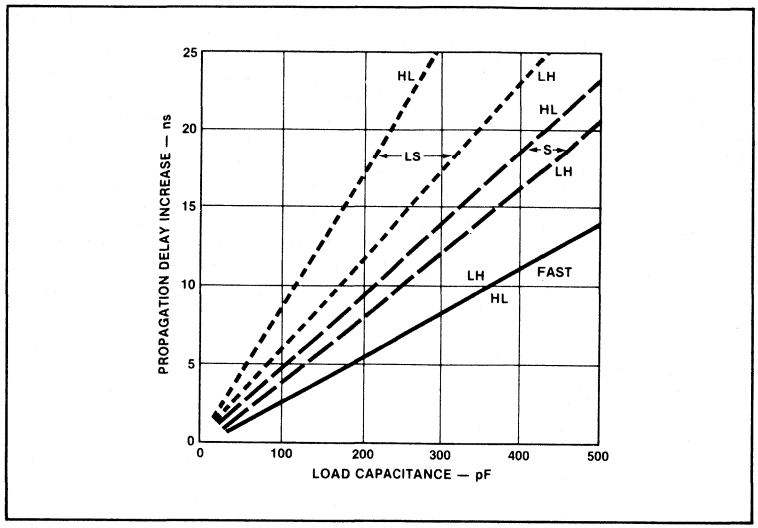


Figure 6. Prop. Delay Increase with Load Cap.

brought out, there is a great deal of versatility built into the devices. Bidirectional data transfers, such as in DMA applications, are very straightforward. In this application, the devices can actually do double duty because they can also latch data from one bus and at a later time place it back on that same bus. This means that DMA controllers used for transfers from one bus to another can also funciton as temporary latches for DMA-driven block moves within the address space on each bus independently of the other.

Table 3. Octal Buffers and Transceivers

'F240	Octal Buffer/Line Driver—Inverting, 3-State Outputs
'F241	Octal Buffer/Line Driver—Non-Inverting, 3-State Outputs
'F244	Octal Buffer/Line Driver—Non-Inverting, 3-State Outputs
'F245	Octal Transceiver—Non-Inverting, 3-State Outputs
'F545	Octal Transceiver—Non-Inverting, 3-State Outputs
'F588	Octal Transceiver—Non-Inverting, IEEE-488, 3-State Outputs
'F620	Octal Transceiver—Inverting, 3-State Outputs
'F621	Octal Transceiver—Non-Inverting, Open-Collector Outputs
'F622	Octal Transceiver—Inverting, Open-Collector Outputs
'F623	Octal Transceiver—Non-Inverting, 3-State Outputs
'F655	Octal Buffer/Line Drivers with Parity Generator/Checker—Inverting, 3-State Outputs
'F656	Octal Buffer/Line Drivers with Parity Generator/Checker—Non-Inverting, 3-State Outputs
'F657	Octal Transceiver with Parity Generator/Checker—Non-Inverting, 3-State Outputs

The growing recognition of the need for error detection and correction in microprocessor systems has resulted in both totally new circuits being added to the FAST family, as well as functions popular in LS and S being duplicated in FAST, but with added performance. For instance, the popular 'F280 also appears in FAST as the 'F280A. This part features a high-impedance NPN transistor input structure and high-speed interior, which results in typical propagation delays of 9ns, making it twice as fast as the older Schottky equivalent. Additionally, the input LOW current is only 20μA, which makes it possible to achieve improved fanout.

To carry the use of parity one step further, a set of three octals incorporating parity generator/checkers in the same package have been added to the family. These duplicate the familiar 'F540 and 'F541 buffers and the 'F245 transceiver, but the use of a 24-pin, 300-mil-wide DIP package allows the equivalent of the 'F280A to be included with the octal function. This provides the user with automatic parity checking without increasing his package count and makes parity checking at the subsystem level both practical and inexpensive.

Table 4. Octal Latches

'F273	Octal D Flip-Flops—TTL Outputs
'F373	Octal Transparent Latch—3-State Outputs
'F374	Octal D Flip-Flops—3-State Outputs
'F377	Octal D Flip-Flops w/Clock Enable—TTL Outputs
'F533	Octal Transparent Latch—Inverting 3-State Outputs
'F534	Octal D Flip-Flops—Inverting 3-State Outputs
'F604	Octal 2-Input Multiplexed Latch—High Speed, 3-State Outputs
'F605	Octal 2-Input Multiplexed Latch—High Speed, Open Collector Outputs
'F646	Octal Bus Transceivers and Registers—3-State, Non-Inverting Outputs
'F647	Octal Bus Transceivers and Registers—Open Collector, Non-Inverting Outputs
'F648	Octal Bus Transceivers and Registers—3-State, Inverting Outputs
'F649	Octal Bus Transceivers and Registers—Open Collector, Inverting Outputs

For those systems requiring error correction as well as detection, several circuits are planned. The 'F630 and 'F631 are 16-bit EDACs capable of detecting and correcting single-bit errors and detecting two-bit errors. This is an example of the importance of using high-speed bipolar support circuits in conjunciton with relatively slow MOS memories. Any delay in this circuit can introduce a WAIT state to the processor, because the entire operation should be transparent to the processor and must occur in the normal memory access. The 'F630 and 'F418 devices are 16- and 32-bit Error Detection and Correction Circuits (EDACs). They generate 6-bit ('F630) and 7-bit ('F418) check words from 16- or 32-bit words. Each check word is stored along with a corresponding data word during the memory WRITE cycle. During the memory READ cycle, the 22- or 39-bit word retrieved from the memory is analyzed and all single-bit errors are flagged and corrected, and all dual-bit errors are flagged (but not corrected). In addition, the gross-error condition (all 1's or 0's) is detected.

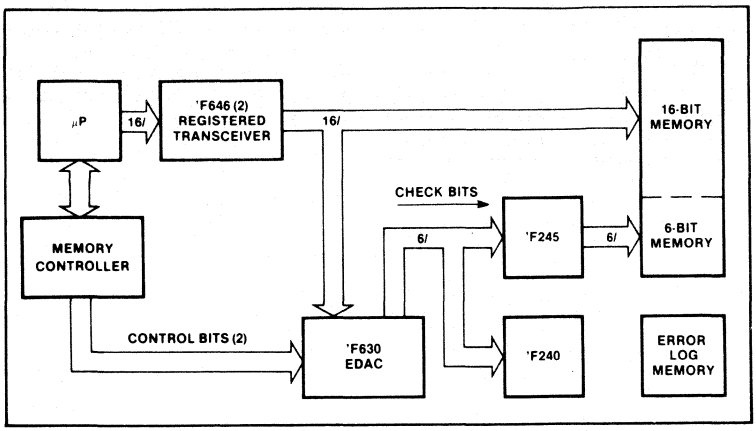


Figure 7. Error Detection and Correction (Write Cycle)

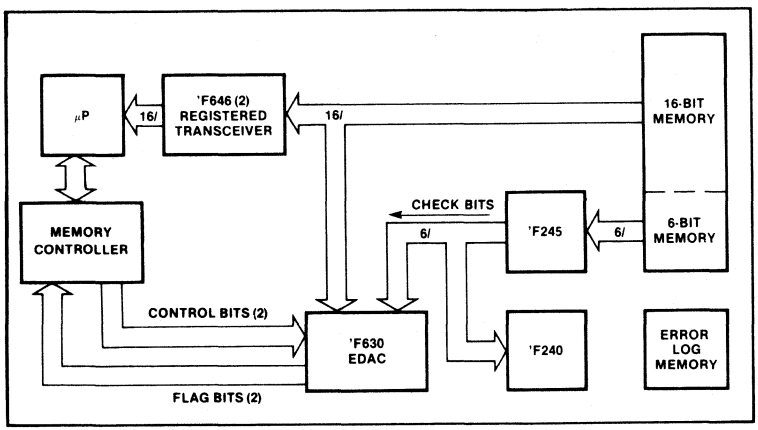


Figure 8. Error Detection and Correction (Read Cycle)

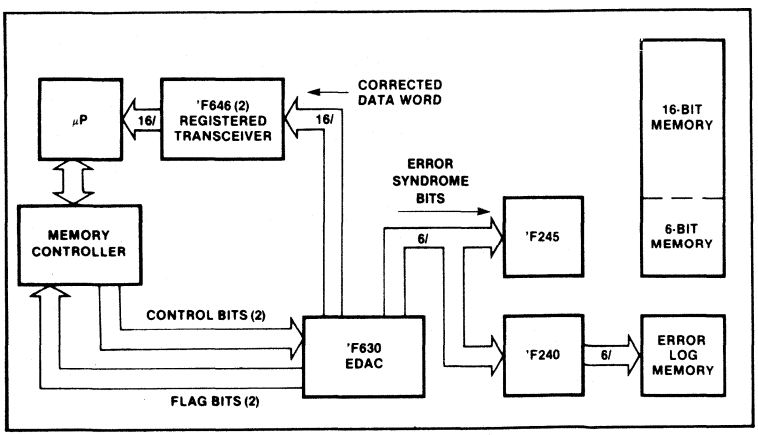


Figure 9. Error Detection and Correction (Error Correction Mode)

Table 5. Error Detection/ Correction Functions

'F280A	9-Bit Parity Generator/Checker
'F655	Octal Buffer/Line Drivers with Parity Generator/Checker—Inverting 3-State Outputs
'F656	Octal Buffer/Line Drivers with Parity Generator/Checker—Non-Inverting 3-State Outputs
'F657	Octal Transceiver with Parity Generator/Checker—Non-Inverting 3-State Outputs
'F630	16-Bit Error Detection and Correction Circuit—3-State Outputs
'F631	16-Bit Error Detection and Correction Circuit—Open Collector Outputs
'F401	CRC Generator/Checker
'F402	Expandable CRC Generator/ Checker
'F418	32-Bit Error Detection and Correction Circuit—3-State Outputs

Many of the larger microprocessor systems are now beginning to use dual-port memory as a vehicle for passing data and parameter blocks between two or more processors. Although the arbitration circuitry for this operation is fairly straightforward when static memories are used, it becomes very involved with dynamic memories because of the attendant problems of dynamic memory refresh. As a result, dual-port memory tends to be implemented with static RAMs, which are comparatively expensive and only available in smaller sizes.

The 'LS764 from Signetics is not a member of the FAST family, but has speed that approaches FAST performance and provides a combination of dynamic memory refresh and the dual-port bus arbitration circuitry in a single 40-pin package. All of the handshaking signals are provided so that any microprocessor may be used in conjunction with dynamic RAMs up to 256K. In effect, there are actually three inputs to the controller—the first and highest priority is the refresh counter. The other two are the memory request lines from the processors. Memory grant signals are returned to the processors and may be used to select address buffers so that the multiplexing of addresses between the two processors is done by the 3-state octals directly. Multiplexing of the address lines into row and column addresses is done internally within the controller. As a result, a complete 256K-byte dual-port memory can be implemented

with only the controller and eight RAM chips. The maximum size of the memory that can be driven by one controller is set by the maximum output capacitance that can be safely driven by any output—256pF. The input capacitance of 256K NMOS DRAM is on the order of 8pF. This brings the effective fanout of the controller to 32 and the maximum memory size to 1M byte.

SUMMARY

The FAST family of oxide-isolated TTL has addressed the problems of interfacing high-performance microprocessors to the rest of the system. The family has been optimized for octal functions that combine simple buffer and transceivers with other, more complex functions such as error detection and correction, specialized memory control circuits, and dual-bus data transfer functions.

TESTING AND SPECIFYING FAST LOGIC

App Note 202

INTRODUCTION

FAST[1] Advanced Schottky TTL is a second generation Schottky logic family that utilizes advanced oxide-isolation techniques to increase the speed and decrease the power dissipation beyond the levels achievable with conventional junction-isolated families. The improved performance of the family is exhibited in two ways — first, the speed and power characteristics of the devices are improved, and second, the conditions under which speed and power are specified are much tighter. For instance, LS and S TTL families offer AC limits only at a nominal +5.00V V_{CC} supply voltage and at room temperature, 25° C. By contrast, FAST guarantees improved AC performance and specifies that performance over a supply variation of +5.00V ±5% and at temperatures from 0° to 70° C. Thus the designer no longer needs to derate his propagation delays from the data sheet limits to compensate for speed degradation over the temperature range.

With every advance of this magnitude, there arise new considerations that must be kept in mind both by the system designer and the user setting up test procedures. FAST is no exception, and it is these considerations that will be addressed in this application note. This paper represents an attempt to describe the way the FAST logic parts are specified, why they are spec'd in the way they are, and how the parts may be tested in the qualification lab and at incoming inspection to verify their performance.

THE FAST DATA SHEET PHILOSOPHY

Signetics FAST data sheets have been configured with an eye to quick useability . . . they are self contained and should require no reference to other sections for information. The typical propagation delays listed at the top of the page are the average between t_{PLH} and t_{PHL} for the most significant data path through the part. In the case of clocked products, this is sometimes the max frequency of operation, but in any event this number is a 5.00V - 25° C typical specification. The ICC typical current shown in that same specification block is the average current (in the case of a gate, this will be the average of the I_{CCH} and I_{CCL} currents) at room temperature and V_{CC} = 5.00V. It represents the total current through the package, not the current through individual functions.

Other considerations are the FANOUT AND LOADING TABLES. Some manufacturers relate these numbers in terms of 7400 gate loads . . . Signetics feels that FAST is unlikely to be mixed with other logic families and so gives the loading factors in terms of FAST unit loads. A FAST unit load is defined to be 0.6 mA in the LOW state and 20 μA in the HIGH state. Thus in the case of the 74F00 gate, the inputs are specified as 1 Ful (FAST unit load) each . . . the outputs need a little explanation. The standard FAST output is specified with an I_{OL} sink current of 20 mA and an I_{OH} of -1.0 mA. Thus the fanout of this gate in the LOW state is 20 mA/0.6 mA or 33 FAST unit loads. In the HIGH state the fanout is 1 mA/20 μA or 50 FAST unit loads. In each case, the Fanout and Loading Table on the Signetics data sheets states the HIGH/LOW fanout numbers . . . thus the 74F00 output fanout is specified as 50/33 Ful.

ABSOLUTE MAXIMUM RATINGS

The ABSOLUTE MAXIMUM RATINGS TABLE carries the maximum limits to which the part can be subjected without damaging it . . . there is no implication that the part will function at these extreme conditions. Thus, specifications such as the most negative voltage that may be applied to the outputs only guarantees that if less than -0.5V is applied to the output pin, after that voltage is removed the part will still be functional and its useful life will not have been shortened — it is difficult to imagine the meaning of the term "functionality" WHILE that voltage is applied to the output.

Input voltage and output voltage specs in this table reflect the device breakdown voltages in the positive direction (+7.0V) and the effect of the clamping diodes in the negative direction (-0.5V).

RECOMMENDED OPERATING CONDITIONS

The RECOMMENDED OPERATING CONDITIONS TABLE has a dual-purpose. In one sense, it sets some environmental conditions (operating free-air temperature), and in another, it sets the conditions under which the limits set forth in the DC ELECTRICAL CHARACTERISTICS TABLE and AC ELECTRICAL CHARACTERISTICS TABLE will be met. Another way of looking at this table is to think of it, not as a set of limits guaranteed by Signetics, but as the conditions Signetics uses to test the parts and guarantee that they will then meet the limits set forth in the DC and AC ELECTRICAL CHARACTERISTICS TABLES.

Some care must be used in interpreting the numbers in this table. Signetics feels strongly that the specifications set forth in a data sheet should reflect as accurately as possible the operation of the part in an actual system. In particular, the input threshold values of V_{IH} and V_{IL} can be tested by the user with parametric test equipment . . . if V_{IH} and V_{IL} are applied to the inputs, the outputs will be at the voltages guaranteed by the DC Electrical Characteristics Table. There is a tendency on the part of some users to use V_{IH} and V_{IL} as conditions applied to the inputs to test the part for functionality in a "truth-table exerciser" mode. This frequently causes problems because of the noise present at the test head of automated test equipment. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, on the order of milliseconds, and any noise present at the inputs has settled out before the outputs are measured. But in functionality testing, the outputs are examined much faster, before the noise on the inputs has settled out and the part has assumed its final and correct output state. Thus V_{IH} and V_{IL} should never be used in testing the functionality of any TTL part including FAST. For these types of tests input voltages of +4.5V and 0.0V should be used for the HIGH and LOW states respectively.

In no way does this imply that the devices are noise sensitive in the final system. The use of "hard" HIGHs and LOWs during functional testing is done primarily to reduce the effects of the large amounts of noise typically present at the test heads of automated test equipment with cables that may at times reach several feet. The situation in a system on a PC board is less severe than in a noisy production environment.

DC ELECTRICAL CHARACTERISTICS

This table reflects the DC limits used by Signetics during its testing operations and conducted under the conditions set forth under the RECOMMENDED

[1] FAST is a trademark of Fairchild Camera and Instrument Corporation.

OPERATING CONDITIONS TABLE. V_{OH}, for example, is guaranteed to be no less than 2.7V when tested with V_{CC} = +4.75V, V_{IH} = 2.0V, V_{IL} = 0.8V, across the temperature range from 0° to 70° C, and with an output current of I_{OH} = -1.0 mA. In this table, one sees the heritage of the original junction-isolated Schottky family . . . V_{OL} = 0.5V at I_{OL} = 20 mA. This gives the user a guaranteed worst-case LOW state noise immunity of 0.3V. In the HIGH state the noise immunity is 0.7V worst case. Although at first glance it would seem one-sided to have greater noise immunity in the HIGH state than in the LOW, this is a useful state of affairs. Because the impedance of an output in the HIGH state is generally much higher than in the LOW state, more noise immunity in the HIGH state is needed. This is because the noise source couples noise onto the output connection of the device — that output tries to pull the noise source down by sinking the energy to ground or to V_{CC} depending on the state. The ability of the output to do that is determined by its output impedance. The lower half of the output stage is a very low impedance transistor which can effectively pull the noise source down. Because of the higher impedance of the upper stage of the output, it is not as effective in shunting the noise energy to V_{CC}, so that an extra 0.4V of noise immunity in the HIGH state compensates for the higher impedance. The result is a nice balance of sink and drive current capabilities with the optimum amount of noise immunity in both states.

I_I, the maximum input current at maximum input voltage, is a measure of the input leakage current at the guaranteed minimum input breakdown voltage of 7.0V. Although some users consider this to be a test of the input breakdown itself, that voltage is typically over 15V. At room temperature, this leakage current should be less than 10 μA.

Short-Circuit Output Current is a parameter that has appeared on digital data sheets since the inception of integrated circuit logic devices, but the meaning and implications of that spec have totally changed. Originally I_{OS} was an attempt to reassure the user that if a stray oscilloscope probe accidentally shorted an output to ground the device would not be damaged. In this manner, an extremely long time was associated with the I_{OS} test. However, thermally induced malfunctions could occur after several seconds of sustained test.

Over a period of time, I_{OS} became a measure of the ability of an output to charge line capacitance. Assume a device is driving a long line and is in the LOW state. When the output is switched HIGH, the rise time of the output waveform is limited by the rate at which the line capacitance can be charged to its new state of V_{OH}. At the instant that the output switches, the line capacitance looks like a short to ground. I_{OS} is the current demanded by the capacitive load as the voltage begins to rise and the demand decreases. We now reach the critical point in our discussion. The full value of I_{OS} need only be supplied for a few hundred microseconds at most, even with 1.0 μFd of line capacitance tied to the output, a load that is unrealistically high by several orders of magnitude.

The effect of a large I_{OS} surge through the relatively small transistors that make up the upper part of the output stage is not serious, AS LONG AS THAT CURRENT IS LIMITED TO A SHORT DURATION. If the hard short is allowed to remain, the full I_{OS} current will flow through that output state and may cause functional failure or damage to the structure. A test induced failure may occur if the I_{OS} test time is excessive. As long as the I_{OS} condition is very brief, typically 50 ms or less with ATE equipment, the local heating does not reach the point where damage or functional failures might occur. As we have already seen, this is considerably longer than the time of the effective current surge that must be supplied by the device in the case of charging line capacitance. The Signetics data sheet limits for I_{OS} reflect the conditions that the part will see in the system — full I_{OS} spikes for extremely short periods of time. Problems could occur if slow test equipment or test methods ground an output for too long a time causing functional failure or damage.

AC TESTING

FAST data sheets carry several types of AC information. The AC CHARACTERISTICS TABLE contains the guaranteed limits when tested under the conditions set forth under the AC TEST CIRCUITS AND WAVEFORMS. In some cases, the test conditions are further defined by the AC SETUP CONDITIONS — this is generally the case with counters and flip-flops where setup and hold times are involved. All of the AC Characteristics are guaranteed with 50 pF load capacitances. One of the sets of limits is spec'd at 25° C and +5.00V V_{CC} — these relate closely to the standard Schottky specs which are under similar conditions but use only 15 pF load capacitances. While these numbers are convenient for comparing the two families, keep in mind that using full 50 pF loads with the Schottky devices would add several nanoseconds to their propagation delays. These numbers are ideal for checking out test jigs and correlating data since they do not involve temperature or supply voltage spreads. For system design, full specifications are included that include temperature and supply voltage variations — in one case the military ranges and in the other, the commercial ranges.

AC TEST JIGS AND SETUPS

Each FAST data sheet spells out the test circuit used to check AC performance, the waveforms, meaurement points, rep rate, test loads, etc. But these are only the quantifiable variables involved in this testing. There is another more complex side to the issue — test jigs and equipment setups.

To get an appreciation for the problems involved in testing FAST, consider these facts. The output rise and fall times on FAST outputs are very sharp. Translating these edge rates into the effective sine wave equivalents generates frequencies on the order of several hundred MHz. At these frequencies, attention to RF phenomena is required.

Because of these RF frequencies, it is necessary to have an AC test jig that has minimal modifying effect on the input and output waveforms. To do this the jig must be constructed properly. The following items are key in dealing with AC jig construction.

DECOUPLING CAPACITORS

Signetics uses high quality capacitors that have good RF qualities to decouple the power supply lines on the test jig, right at the V_{CC} pin to the ground plane. Three capacitors with absolute minimum lead length are used. These are one each, 1 μFd dipped tantalum, 0.1 μFd dipped tantalum or ceramic, and .002 μFd ceramic.

GROUNDING

One of the biggest contributors to waveform degradation is improper grounding. In reference to the test jig,

the grounding is best done with a large ground plane that is directly connected to the ground pin of the test socket. The Signetics AC test jig is constructed out of solid copper and provides an excellent ground to the pin and prevents ground loops, which are problems on most jigs constructed out of PC board material. The metal surface of the Signetics jig also provides a very low inductance, low resistance ground path. In this type of construction, the stray ground currents are negligible and the part is provided with a very "clean" environment.

WIRING

The next concern is getting the input signal to the part and the output signal to the measurement system. The main requirement at this point is to keep the wires to the socket as short as possible, thereby reducing inductance and reflections. At the same time the wires should be close to the ground plane to maintain a somewhat constant impedance over the entire length. Wire should be 18 gauge to minimize inductance and to facilitate jig construction. The length of wire on each pin should be identical to provide uniform jig delay.

JIG DELAY

One factor that must be considered when taking measurements on the jig is the delay introduced by the jig itself. This delay will now be described. The stimulus (generator) is monitored by a probe at the point where the signal enters the jig. At the time the signal enters the jig, the signal is also traveling up the probe. It takes a finite amount of time to travel from the connector of the jig to the pin of the device. That time cannot be considered in the propagation delay of the device and must therefore be subtracted. For reference, this time is known as t_{in} delay. This time, t_{in} delay, has also elapsed for the probe, so the measurement system sees this signal, t_{in} delay, before the part does. On the output, a similar situation occurs. The probe on the connector of the jig sees the signal from the output only after it has traveled from the pin to the jig connector. This is known as t_{out} delay. Because the measurement system sees this signal after the t_{out} delay, this too must be subtracted. Consequently, if both delay times are summed, a jig delay factor can be obtained. The jig delay times are not insignificant when compared to extremely low propagation delays obtainable with FAST. Signetics jigs demonstrate typical jig delay times on the order of 0.5–0.75ns, which cannot be ignored. The exact jig delay time is determined by the size of the universal jig that is being used. It is also important to know that the frequency response of the jig must be high to prevent the delay factor from varying with the edge rates. The frequency response of the jig indicates how constant the impedance remains over frequency. The characteristic impedance of a transmission line is expressed as . . .

$$Z_o = \frac{V}{I} = \sqrt{\frac{L_o}{C_o}}$$

where L_o is the inductance per unit length, C_o is the capacitance per unit length, Z_o is in Ohms, L_o in Henrys, and C_o in Farads. Propagation velocity and its inverse, delay per unit length δ, are also expressed in L_o and C_o ...

$$V = \frac{1}{\sqrt{L_o C_o}} \qquad \delta = \sqrt{L_o C_o}$$

where δ is expressed in nanoseconds, L_o is in microhenrys per unit length, and C_o in microfarads per unit length. From this, it is clear that if the Z_o changes over frequency, then the delay per unit length will vary as well. Therefore, it is imperative to know how the jig responds over frequency.

Frequency response also depends on the phase as well as the magnitude of the impedance. If the phase changes so does the delay, since delay is the derivative of phase change with frequency. An S-parameter analysis is needed in evaluating jig performance.

UNIVERSAL JIG CONSTRUCTION

Jig universality is with respect to chip pin count and as such, separate universal test jigs are built for 14, 16, 20, 24 and 28 pin parts.

Signetics FAST bench test jigs are fabricated from 3 inch metal caps. A Textool ZIF socket is mounted in the top center of the jig and connected to BNC connectors spaced equidistantly around the wall of the jig with 18 gauge wire. An S-parameter analysis was performed in a network analyzer to optimize the jig layout. This assured that the jig had a flat frequency response over the spectrum of interest for FAST product. See Figures 1, 2 and 3 for the jig and load response over frequency. The jig itself is

TRANSFER CHARACTERISTICS OF THE LOAD OVER FREQUENCY

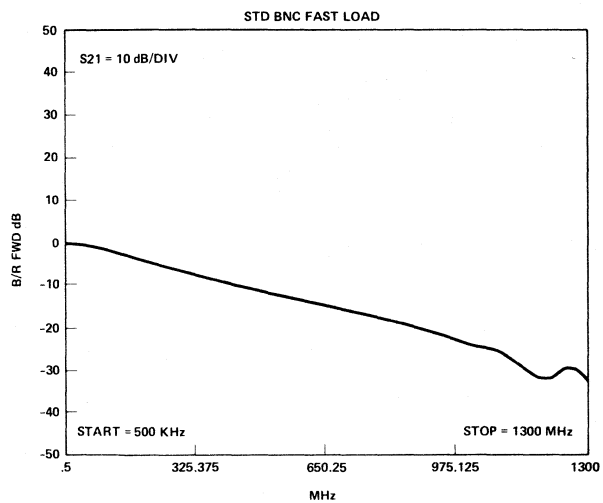


Figure 1.

6

pictured in Figures 4 - 5 and the load in Figures 6 - 8. The equipment used to analyze the jigs and loads was: HP8505A Network Analyzer, HP8503A S-Parameter Test Set, HP8501A Storage Normalizer. In some measurements the equipment was driven by an HP9845B desk-top computer.

Jigs produced in this way should have minimal lead length to reduce the characteristic inductance. This in turn minimizes reflections with their accompanying waveform distortions and measurement inaccuracies.

AC TEST LOADS FOR THE SIGNETICS UNIVERSAL JIG

As stated previously, the Network Analyzer was also used to design and optimize AC test loads to be used with the universal jig. FAST product loads require 50 pF load capacitance and 500Ω resistance to ground.

Signetics meets the 50 pF requirement through the use of a 45 pF load, 4 pF jig capacitance, and 3 pF probe capacitance. The result, 52 pF, is slightly more stringent than required.

A few words about load capacitors are in order. All capacitors have an associated inductance. Due to this inductance, a capacitor will form a series resonant circuit at some frequency. For single 50 pF capacitors, this typically occurs between 200 and 600 MHz depending on the type of capacitor. Above this resonant frequency, the capacitor has inductive characteristics and does not present a capacitive load. This is very important with FAST because harmonics due to the sharp edge transition rates occur at 600 MHz and above.

The Signetics FAST loads solve this problem by reducing the load capacitor lead inductance by paralleling three 15 pF chip capacitors. The resulting load is 45 pF. At the same time, since smaller value caps are used to build up the capacitive load, the associated series resonant point is above 1.2 GHz.

The load resistors are 1/8 watt selected 510 ohm ±10 ohm resistors.

The entire load assembly is constructed inside two standard BNC connectors, the UG-88/u and the UG-1094/u. Slots are machined in the UG-1094/u connectors to allow placement and soldering of the three chip capacitors and the 510 ohm resistor. In the case of tri-state load,

TRANSFER CHARACTERISTICS OVER FREQUENCY THROUGH THE 20-PIN UNIVERSAL TEST JIG

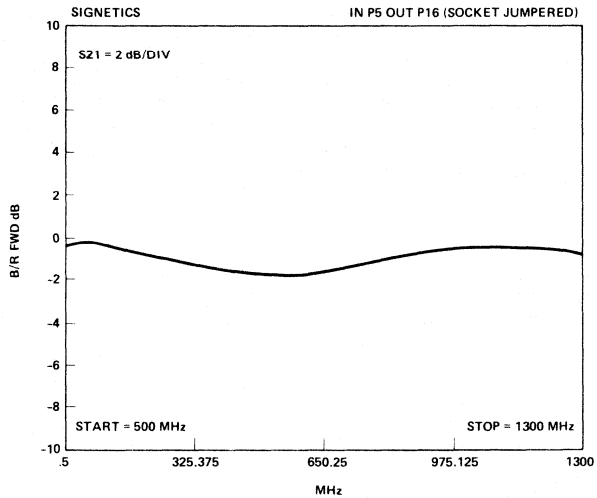


Figure 2.

PLOT SHOWING LINEAR PHASE CHARACTERISTICS OVER FREQUENCY OF THE 20-PIN UNIVERSAL TEST JIG

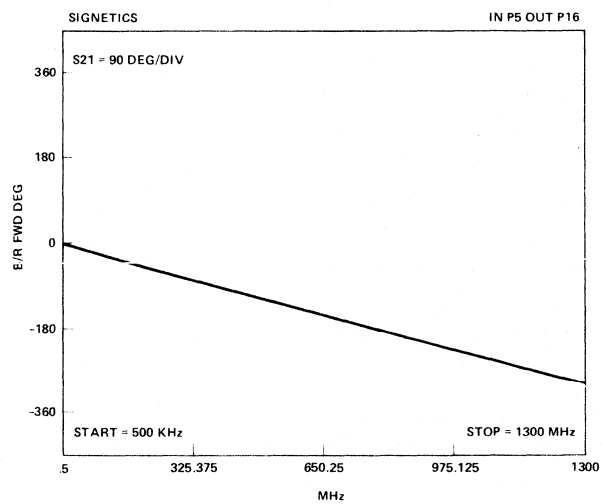


Figure 3.

two 510 ohm resistors are used. Signetics uses BNC connectors with Teflon insulation. Teflon insulation facilitates load construction over other forms of hard plastic insulators found in some connectors. The second resistor is connected to a banana jack which is fastened to the load assembly. The load circuit is detailed on the FAST data sheets for tri-state parts.

CORRELATION

While numerous ATE systems are available, and are very efficient, it is imperative that the ATE correlate to a user's bench setup. Since the Signetics FAST parts are all characterized on the setup described in this note, it is just as important that the user bench jigs meet the same performance criteria. Without similar jigs, it will be very difficult to correlate AC data.

THE SIGNETICS UNIVERSAL TEST JIG

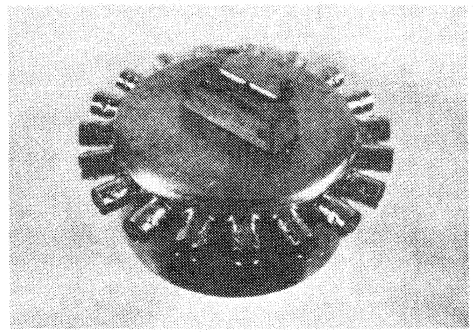


Figure 4.

THE SIGNETICS TEST JIG FROM THE UNDERSIDE. ALL LEAD LENGTHS ARE EQUAL AND ARE DRESSED TIGHTLY AGAINST THE METAL JIG ITSELF.

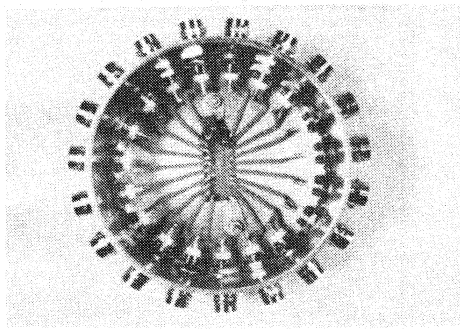


Figure 5.

THE SIGNETICS FAST LOADS ARE CONSTRUCTED FROM TWO BNC CONNECTORS. THE 500Ω RESISTOR IS VISIBLE.

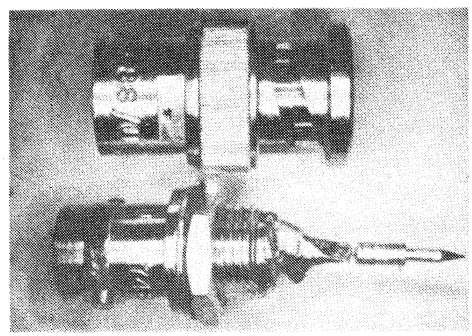


Figure 6.

AXIAL VIEWS OF THE LOAD ILLUSTRATE THE RESISTOR AND THREE CHIP CAPACITORS.

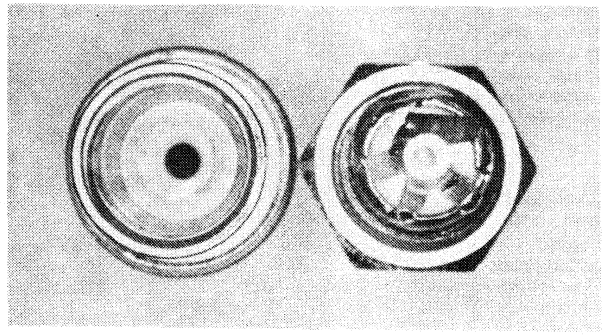


Figure 7.

WHEN THE LOAD IS ASSEMBLED, IT CAN BE MOVED FROM JIG CONNECTOR TO CONNECTOR AND PROVIDES A CONVENIENT WAY OF MONITORING OTHER PATHS THROUGH THE TEST DEVICE. THE RESISTOR AND CAPACITORS ARE MECHANICALLY PROTECTED INSIDE THE CONNECTOR.

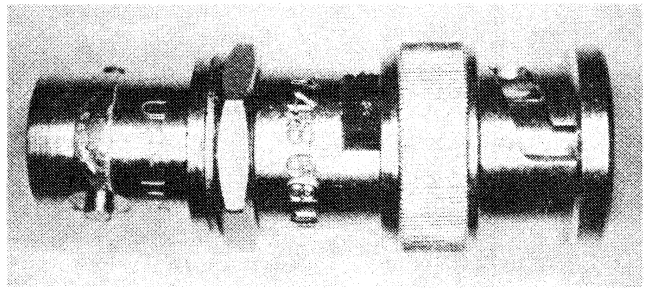


Figure 8.

INTERFACING FAST TO MULTI-PORT MEMORIES App Note 204

INTRODUCTION

As shown in Figure 1, multi-port memories can be accessed by more than one processor; hence, the devices are often referred to as shared memories. Memory elements within a multi-port array can be "random access" (RAM), "read only" (ROM), or some combination of the two. Multi-port memories are frequently interfaced to microprocessors, DMA controllers, I/O processors, state machines, and similar control-type devices. The most common configuration is the dual-port memory with two processors sharing the same array.

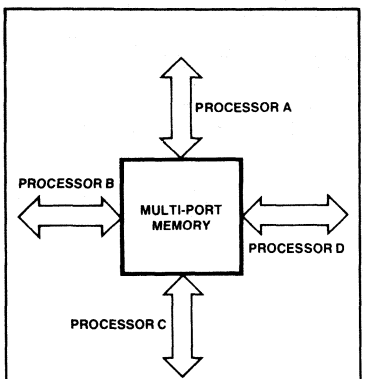


Figure 1. Processors A, B, C, and D Sharing a Multi-Port Memory

Applications for multi-port memories range from simple message passing between processors in a loosely-coupled environment to multiple processors executing from a common program memory in tightly-coupled systems. In some applications it is desirable to have part of the memory addressable from some ports and not from others.

One of the more common shared-memory applications involves CRT controllers. The display memory must be accessed by the controller to refresh the display and by the microprocessor to update and manipulate data on the screen. Another frequent use is in microprocessor development systems where a host processor downloads programs into a dual-port emulation memory and, from there, it is executed by the emulation processor. Other applications include data buffering for mass storage, hard copy output, and a variety of communication devices.

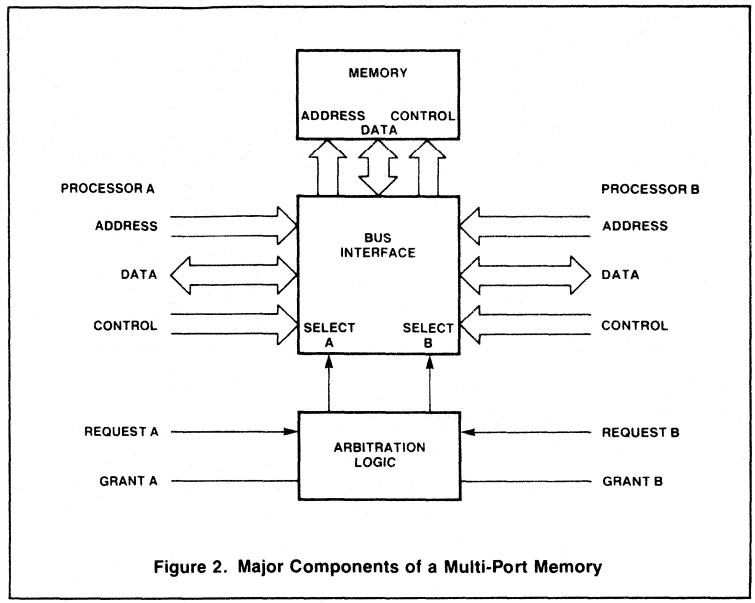


Figure 2. Major Components of a Multi-Port Memory

COMPONENTS OF A MULTI-PORT MEMORY

Major components of the multi-port memory are the memory array, the arbitration logic, and the processor bus-interface logic. Figure 2 shows these components and their relationships in simplified form. The remainder of this document describes each of these components and their interface requirements in an applications environment.

Memory

Memory elements used in the multi-port array can be RAM, ROM, PROM, EPROM, etc. To avoid wasting processor time, the access time of these devices must meet the speed requirements of the fastest processor being used. In computing access time for the memory array, the designer must consider all additional delays of buffering the multi-port bus and other logic.

Static RAMs are generally preferred over dynamic RAMs for multi-port memories because the latter devices require refresh circuitry which effectively adds another port to the array. These additional circuits increase the complexity of system timing and may actually decrease maximum throughput rates. In certain applications, such as display memories, the CRT controller may refresh the memory in the normal course of updating the display, thus requiring no extra port; however, this is not the case for most applications. Since most multi-port memories are small, the increased cost and reduced density of static RAMs are usually not prohibitive.

Arbitration Logic

The arbitration logic is the traffic controller for the multi-port memory system. The arbiter circuits determine which processor should have access to the memory at any given time and initiates the necessary control to see that everything happens in the proper sequence. There are many different arbitration techniques and the one chosen should meet the needs of the particular application. In general, the arbitration logic divides multi-port memory systems into two major classes—"Delayed Access" and "Transparent." Both classes are described in subsequent paragraphs.

Processor Bus Interfaces

Before discussing delayed access and transparent systems, the user should be familiar with conventional methods for interfacing the address, data, and control busses of the processor to the memory array. Two commonly used methods are shown in Figures 3 and 4. In Figure 3, three-state buffers are used for the interface. Unidirectional devices are used for the address and control buffers, whereas, a bidirectional buffer is required for the data bus when read/write (RAM) memory is used. The $\overline{\text{SEL A}}$ and $\overline{\text{SEL B}}$ control signals are used to select the appropriate set of buffers;

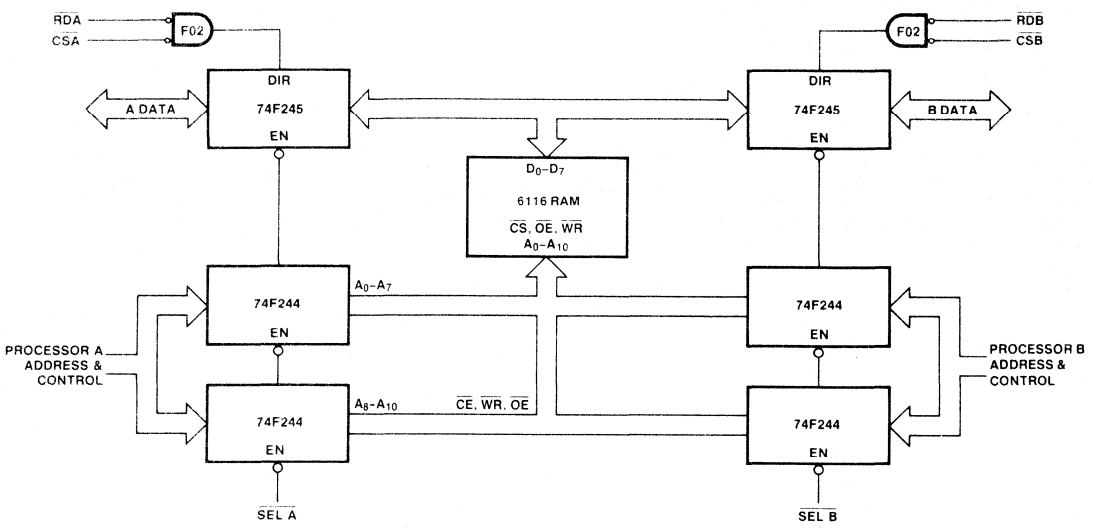


Figure 3. Using Three-State Buffers for Bus Interfaces

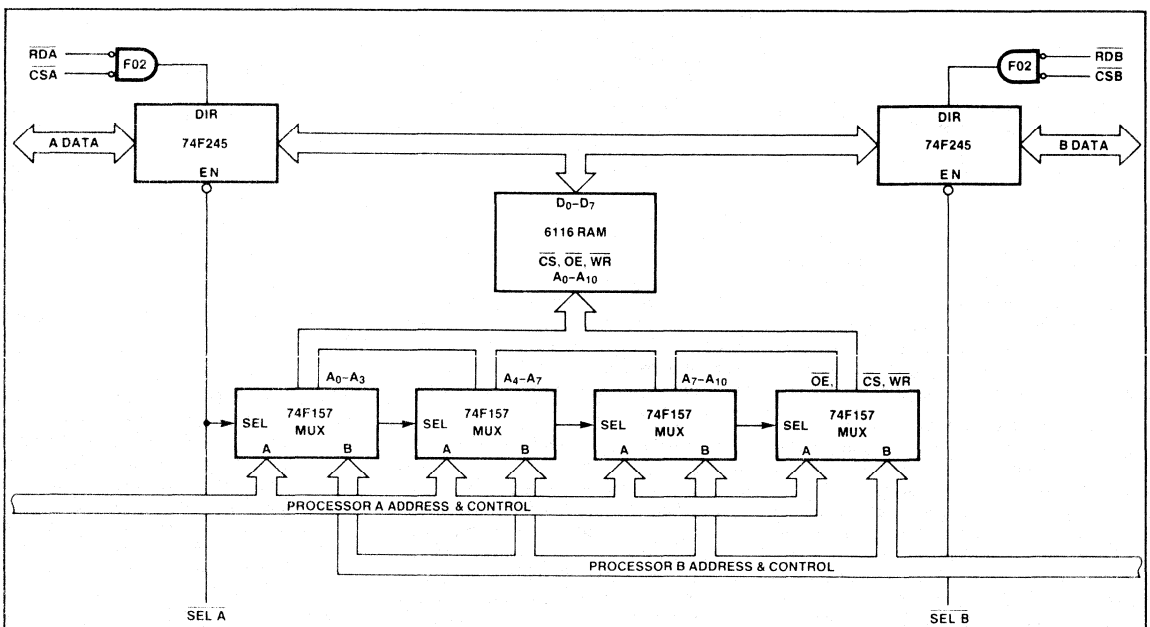


Figure 4. Using Multiplexers to Implement Bus Interfaces

the control signals are mutually exclusive. The configuration shown in Figure 3 has the advantage of PCB layout simplicity but it has the disadvantage of being somewhat sensitive to timing relationships. Care must be taken to avoid bus conflicts caused by two or more buffers trying to drive the bus, resulting in large current spikes. Glitches will occur if one buffer begins to turn on before another completely turns off.

In Figure 4 multiplexers are used to perform the interface functions. This technique eliminates the possibility of conflicts on the address and control busses. The technique has the added advantages of being faster, requiring a smaller package, and using less power. The disadvantages are less drive capabilities and layout complexities.

DELAYED ACCESS MULTI-PORT MEMORIES

In a true delayed access system, each processor is aware that the memory is being shared, that is, when one processor is addressing the memory, all other processors wishing access must wait their turn. This is the most common form of arbitration and the easiest type to implement, especially when using memory arrays with more than two ports. Several methods have evolved for implementing the delayed access type of arbitration; typical examples of such arbitration logic are shown in Figure 5 through 8.

The master/slave arbitration technique is shown in Figure 5. Here, processor A, the master, controls access to the memory; slave processors B and C must always wait for the master to grant permission of access. If the slave processors simultaneously request access, the master makes a decision on the basis of priority. The priority of the slave processors can be a programmed function or determined by hard-wired logic—see Figure 6. A simple two-wire REQUEST/GRANT handshake permits an easy interface to slave processors B and C. Using processor B as an example, the operating sequence can be summarized as follows:

- Slave processor B requests memory access by setting REQUEST B output line true.
- Master processor A responds by connecting busses of processor B to the memory and setting GRANT B output line true.
- Slave processor B accesses memory; when access is completed, the processor sets REQUEST B output line false.
- Master processor A terminates operating cycle by setting GRANT B output line false.

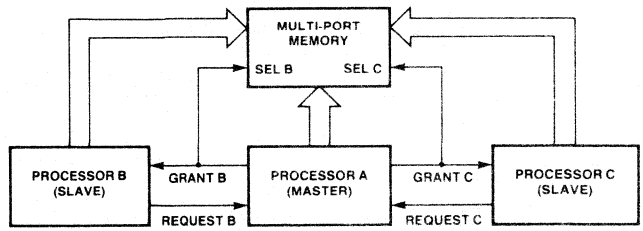


Figure 5. Master/Slave Arbitration

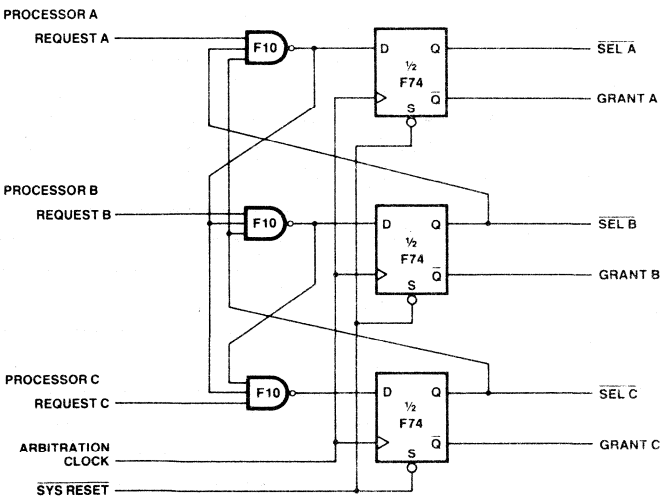


Figure 6. Arbitration Logic for a Multiple Processor System

6

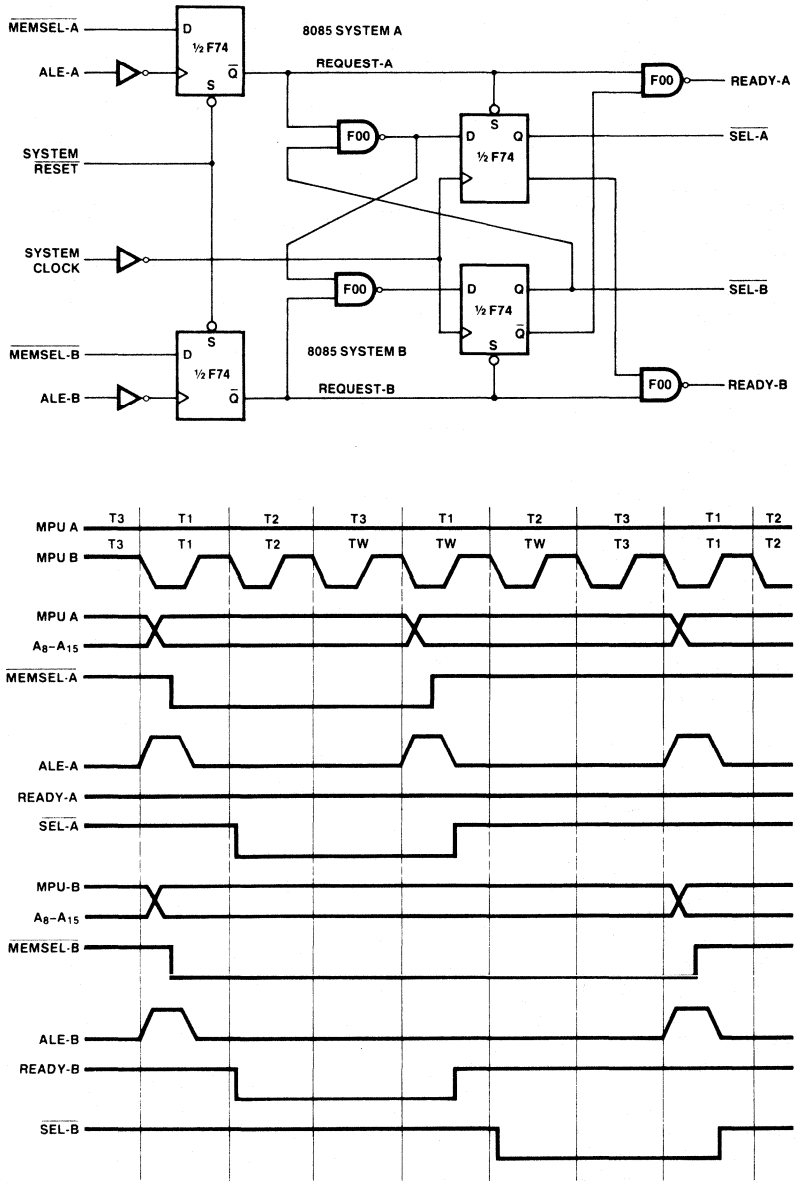


Figure 7. Arbitration Logic Using Processor Dependent Timing

Arbitration logic similar to that shown in Figure 6 is frequently used to interface two or more processors to a multi-port memory. The simple handshake interface can be used with any processor and the system is easily expandable. As structured, processor A has the highest priority and is denied access only when the memory is being used by another processor. Processor B has second highest priority and is denied access only when the REQUEST A line is active or when the memory is being used by processor C. Processor C has the lowest priority and is denied access if either the REQUEST A line or the REQUEST B line is active. Functionally, the REQUEST/GRANT handshake interface is identical to that shown previously for the master/slave arbiter. (Note: To prevent race conditions and/or unstable inputs to the D flip-flops, all REQUEST outputs must be synchronized to the arbitration clock.)

Figure 7 shows how two 8085-based systems can utilize a multi-port memory. Instead of a handshake interface, the arbitration logic uses a READY input to suspend processor operation until the memory can be accessed. If the memory is idle, access is immediate; if the memory is not idle, the processor wishing access must, during the memory cycle, execute wait states (basically NOPs) until the memory is free. In the configuration shown, processor A is given priority over processor B in the event of a simultaneous request for memory access. Either processor can retain access as long as the read and/or write operation is contiguous. Since the timing in this system is processor dependent, the design can be somewhat difficult. The timing diagram in Figure 7 shows idealized waveforms and an access transition from processor A to processor B; the timing sequence is summarized below.

- The MEMory SELect (MEMSEL) generated by the address decoding circuits of each processor is sampled on the falling edge of the Address Latch Enable (ALE) signal to determine if a memory access cycle is in progress. Since both processors have requested access, REQUEST A and REQUEST B lines are set true.
- Because Processor A has priority, the arbitration logic sets SEL A true and sets READY B false on the falling edge of the system clock. With SEL A true, processor A is connected to the memory and completes the specified operation while processor B executes NOPs in the wait state.
- When processor A finishes the memory operation and no longer requests access, MEMSEL A is false when sampled; thus, the REQUEST A line is set to the false state. With REQUEST A false and REQUEST B true, the arbitration logic releases processor B from the wait state by setting READY B true and connects the appropriate busses by setting SEL B true.
- After access is completed by both processors, SEL A and SEL B are set to the false state and the multi-port memory returns to the idle state.

For applications where timing is not super critical, any one of the preceding arbitration techniques can be used with good success. Figure 8 shows a type of arbitration control logic to avoid. The asynchronous arbitration logic shown here can be detrimental to proper operation of the system. A simultaneous request by both processors may cause unstable states, ringing, and/or oscillation, resulting in lost or incorrect data. Whenever possible, arbitration logic and memory access requests from the processor should be synchronized to a system clock.

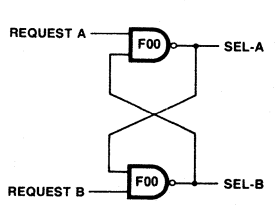


Figure 8. Asynchronous, Non-Clocked Arbitration Logic

TRANSPARENT MULTI-PORT MEMORIES

Transparent memory systems are generally used where timing is a critical factor and memory-access delays cannot be tolerated. In a transparent system, each processor accesses the shared memory as if it were the only user; there is no handshaking, wait states, or other functions that delay access and subsequently degrade system performance. Generally speaking, a transparent system is more difficult to design and somewhat more expensive to implement than the delayed-access type.

One of the more common ways of implementing a transparent multi-port memory system is shown in Figure 9. Here, the memory access time of the two processors is interleaved by the use of a two-phase clock. Each processor accesses memory on opposite phases of the clock signal. During one phase of the clock,

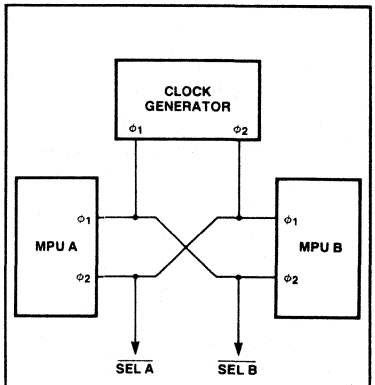


Figure 9. Using a Two-Phase Clock to Achieve Transparency

one of the processors—for instance, processor A—performs internal operations; during this same time interval, processor B accesses memory and performs I/O operations. On the next clock phase, the functions of the two processors are interchanged. By operating the two processors 180° out of phase, complete transparency is achieved. It should be noted that the configuration shown in Figure 9 can only be used with processors that can use two-phase clocks—6800, 6802, 6809, 6502, and like devices. The designer should also be aware that the generation of phased clock signals and, at the same time, meeting other timing parameters of the system can be difficult. This is especially true if overlapping phases or stretching of the clock pulses are required.

Figure 10 shows how a high-speed transparent interface can be achieved between a dual-port memory and two processors operating asynchronously. In this configuration, the read and write cycles are initiated by the processors but actually performed by the timing generator. The timing generator makes memory available to each processor on alternate memory cycles by switching the input multiplexer at the beginning of each read or write operation. The input latches then freeze the state of the address, data, and control busses and temporarily connect the busses to the high-speed memory. If a write cycle is in progress, as determined by the states of CS and WR, the timing generator strobes the data into the specified address. If a read cycle is in progress, data is read from the specified address and strobed into the output latch for access by the processor.

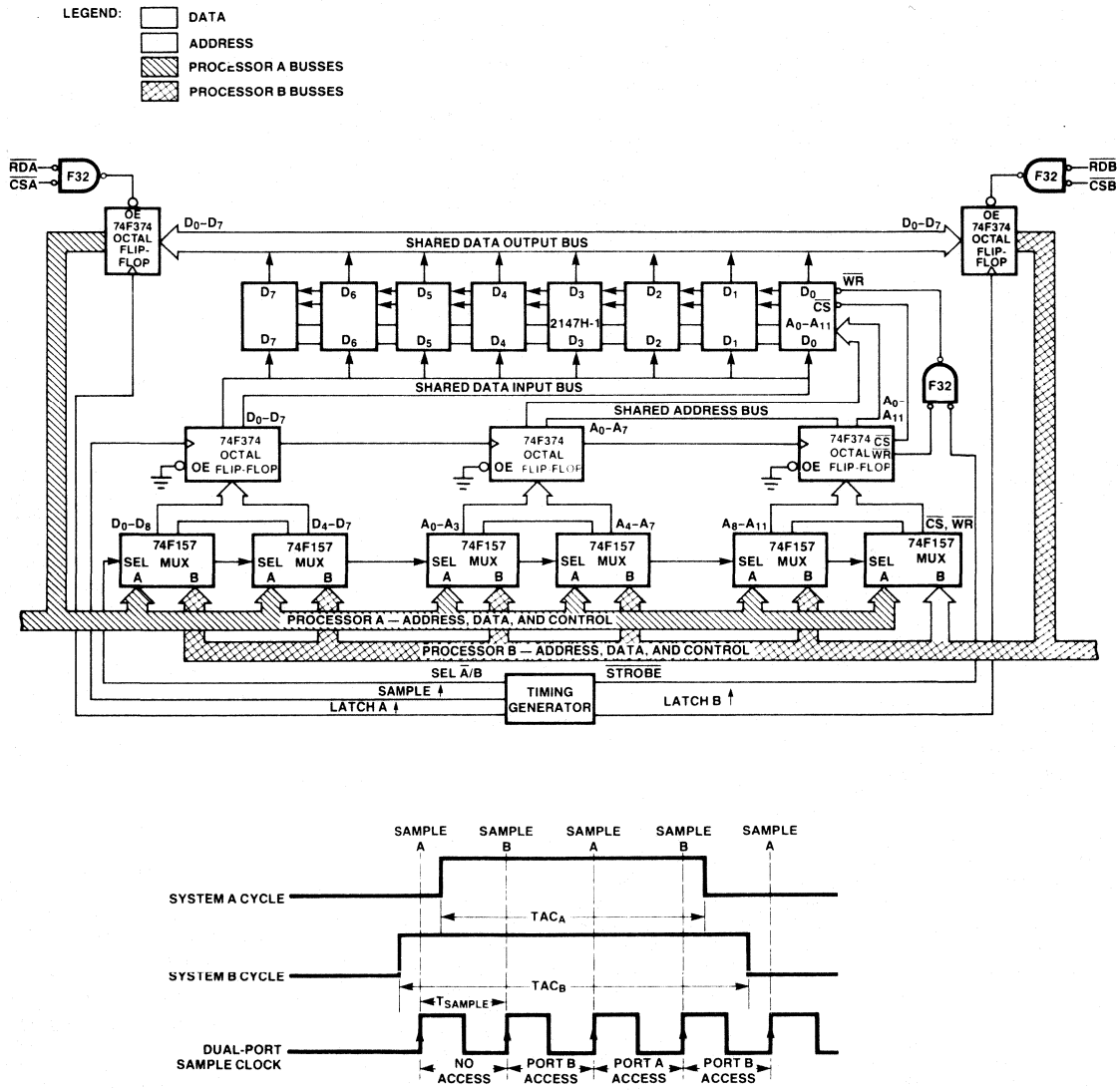


Figure 10. High-Speed Transparent Interface with Asynchronously-Operated Processors

In Figure 10, the memory access time for each processor appears to be 200 nanoseconds but the actual access rate is 65 nanoseconds; thus, the FAST logic family from Signetics is used to meet these high-speed requirements. As shown in the accompanying timing diagram, each processor memory cycle—TAC_A and TAC_B—is sampled at the beginning of alternate cycles of the dual-port memory. To ensure that one cycle of the dual-port memory occurs during the memory cycle of each processor, the cycle time of the memory device must exceed the memory cycle time of the fastest processor by a factor of three. In the case cited, a dual-port memory cycle of 65 nanoseconds is necessary to provide each processor with an apparent memory access time of 200 nanoseconds.

SUMMARY

Many of the applications and concepts provided in this document were direct contributions or heavily influenced by entries in the Signetics' Interface Circuit Design contest. Our special thanks to those individuals whose entries are referenced in whole or in part.

Karta S. Khalsa	Ram N. Sahni
Gregory D. Harris	D. David Walker
David McCraken	Barbara A. Clauson
Daniel Smolenski	Charles M. Lewis
Daniel Appleman	David Pearson
Thomas E. Brown	E. K. Sledge
Phillip B Hunter	Jeff Slama
David M. Skerkoski	Tom Dahlin

In the current marketplace, the use of shared memories, with both delayed-access and transparent type interfaces, is growing. The development of the FAST logic family is only one of many ways Signetics can satisfy your applications needs in this growing market. Whether your requirements are simple, complex, or radical in nature, Signetics can provide silicon solutions—be it logic, memory, gate arrays, or other. For further documentation and/or applications assistance, call or write to your nearest Signetics Sales and Service Office—there is one near you.

NOTES

USING FAST ICs FOR μP-TO-MEMORY INTERFACES App Note 205

INTRODUCTION

Most microprocessor-based systems use some form of bipolar interface between the processor and memory; only a very primitive system does not require such interface support. TTL devices in quad, hex, or octal configurations are used to meet functional and circuit-interface requirements of the system. For complex systems, the interface support may be extensive while, for simple systems, only a few devices may be required to ensure operational integrity. In a majority of system designs, one or more of the following interface requirements must be addressed.

- Buffering and Demultiplexing of Data/Address Buses
- Signal Timing and Signal Isolation
- Address Decoding
- Bank Switching
- Handling of Wait States
- Adjusting Read/Write Data Rates
- Refreshing Dynamic RAM
- Unique Interface Requirements such as Multi-Processor Networks, Data Communication Links, etc.

Interface support is an important part of the overall design job; when implemented with the proper parts, system efficiency can be dramatically improved, higher reliability can be obtained and the design can be executed with minimum parts. This Application Note shows how common interface problems can be solved by using a minimum of high-performance bipolar devices from Signetics.

BUFFERING AND DEMULTIPLEXING

Microprocessor outputs are inherently fanout-limited; thus, some form of buffering is required to drive multiple loads such as those found on address and data buses. Extended bus configurations coupled with MOS loads tend to produce large capacitive sinks which degrade waveforms and also increase propagation delays. The use of TTL buffers provides an easy and economical way of overcoming or, at least, minimizing these harmful effects. In those systems that use shared memories and direct memory access (DMA), buffers are frequently used for isolation and as a method for switching between multiple buses. Buffers are also commonly used to optimize signal-to-noise ratios and to drive multicard bus interfaces. For the most part, buffer and latch-control functions can be summarized as follows:

- Latch the address information in systems that use multiplexed buses.
- During read operations, avoid bus contention by preventing the system from driving the multiplexed address/data bus until the address information is removed.
- Control the direction of data transceivers according to processor operation while preserving write-data and read-data hold times and avoiding bus contention when switching direction.
- Isolate the microprocessor from the system bus during DMA and multiprocessor operations.

With the use of 16-bit microprocessors, systems have become more sophisticated; likewise, buffer control and interface circuits have become somewhat more complex. Many of the 16-bit machines use multiplexed address/data buses to reduce I/O pin count; as a result, latches are required to demultiplex, hold, and buffer the address bus. Not only must the address information be latched at the correct time but the data bus must usually be buffered with bidirectional transceivers to provide the necessary drive. As previously indicated, the interface circuits must be able to avoid bus contention and, when required, to isolate the processor from the system bus.

Buffers and latch-control signals for three popular 16-bit microprocessors — the 8086, the Z8001, and the 68000 — are shown in Figure 1. For each processor, the buffer and interface functions are summarized at the bottom of the figure. Although the timing-and-control functions of the interface support circuits are fairly complex, these internal complexities are transparent to the user; only the bus connections and a few control lines are required to achieve the management goals of the system.

INTERFACE FUNCTIONS (8086 SYSTEM)

- Multiplexed address/data bus (AD_0–AD_{15})
- Three-state latches (74F373) used for demultiplexing; latches are continuously enabled by ALE until data is stable on the bus and a timing pulse is delivered by the microprocessor.
- HLDA is used to float address bus during DMA operation.
- Data bus buffered by 74F245 Transceivers; data direction controlled by DT/$\overline{R}$ in minimum mode.
- Bus control and DMA isolation controlled by $\overline{DEN}$ is minimum mode.

INTERFACE FUNCTIONS (Z8001 SYSTEM)

- Address bus (AD_0–AD_{15}) latched with 74F373s using $\overline{AS}$ for latch enable and $\overline{BUSAK}$ for isolation. (Note. The segmented outputs are designed to drive a Memory Management Unit with internal latches; however, in this application, the address outputs are prelatched since they are not stable for the entire cycle.)
- Data bus buffered with 74F245s; $\overline{DS}$ and R/$\overline{W}$, respectively, control data direction and bus contention.
- BUSAK controls DMA isolation.

INTERFACE FUNCTIONS (68000 SYSTEM)

- Address bus buffered by 74F244s and DMA isolation contolled by BGACK.
- Data bus buffered by 74F245 Transceivers with R/W and BGACK, respectively, controlling data direction and bus isolation. (Note. In this configuration, a larger processor package is required since the address and data buses are separate; some advantage in speed and simplified timing are to be gained.)

Figure 2 shows the effects of buffers and an address decoder on the memory access time in a system configuration. The access time of the 8086 microprocessor is defined as the time from which a valid address appears at the input of the processor assuming that there are no wait states. Observe that each buffer and the decoding function adds a specific delay to the data-processing chain. In addition to these propagation delays, the system designer must consider capacitive loading, buffer access delays, (that is, are buffers enabled when valid data appears at input) and any other delay parameters that would extend the memory access time. (Note. The normal 8086 buffer control does not affect access time.) The delay should be calculated using maximum propagation delays over the operating temperature range of the system. Based on these considerations, the memory access time for the system shown in Figure 2 can be approximated as follows:

8086 READ CYCLE—Address Valid Output to Data Valid Input 460 ns
2732 MEMORY ACCESS TIME (T_{CE})-T_{CE} =460 ns–3 (7 ns)—6.2 ns–9 ns = 423.8 ns

BIDIRECTIONAL BUS INTERFACES

Virtually all microprocessor-based systems use a bidirectional bus interface between the processor and I/O peripherals; the memory interface may require separate-or-common bus connections. In either case, the 8T28 Quad Transceiver is well suited to this type of application. The 8T28 is able to drive a capacitive load of 300-picofarads without waveform degradation and the three-state outputs provide the switching speeds of TTL while offering the drive capabilities of open-collector gates. Typical bus interfaces are shown in Figure 3.

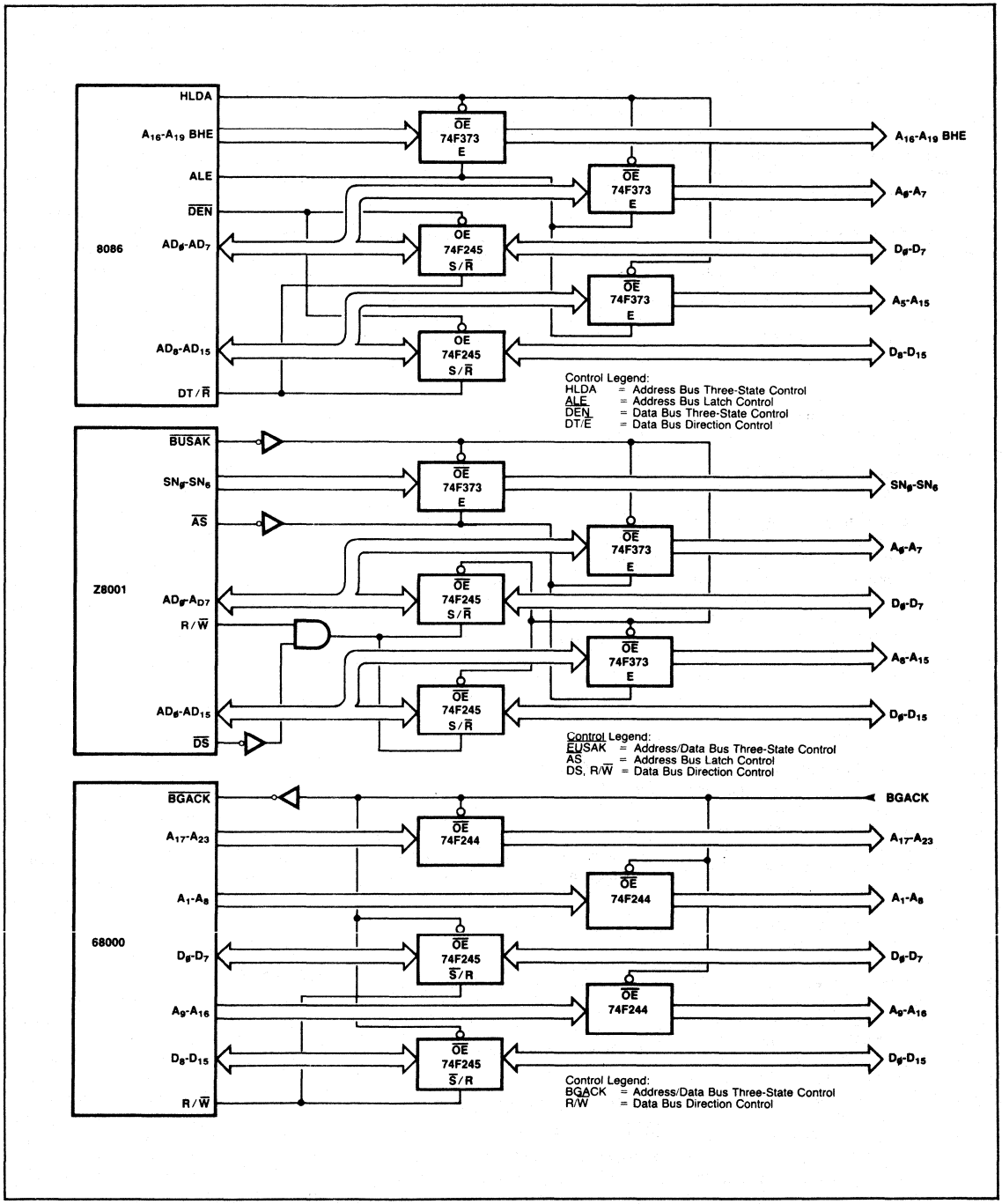


Figure 1. Examples of Processor-to-Bus Interfaces

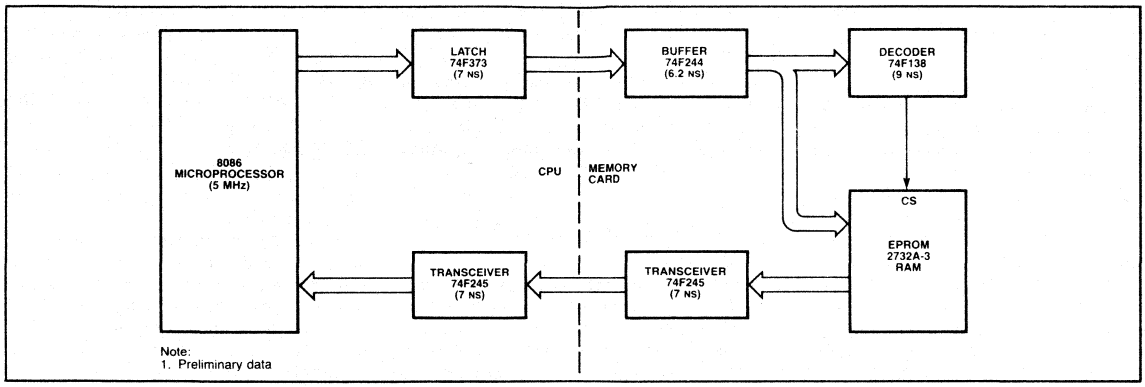


Figure 2. System Showing Typical Interface Delays

In Figure 3a, the transceiver provides a bidirectional interface between the system bus and separate input/output buses of the dynamic RAM. The D_{IN} bus is continuously driven while the D_{OUT} bus is gated onto the system bus via D/E.

Figure 3b shows a static RAM interface implemented by tying R_{OUT} and D_{IN} together. Here, the 8T28 functions as a normal bidirectional transceiver, providing buffered drive between the system bus on one hand and the memory I/O bus on the other. The bottom panel shows how the 8T28 can be used in the dual capacity of an on-board/off-board buffer/driver. To prevent signal degradation in such multi-board systems, the address/data/control buses must be buffered if off-board extensions are to be driven. Furthermore, the on-board/off-board buses should be buffer-isolated to prevent downstream noise and/or failures from feeding back to the mother board. In Figure 3, observe that driver gates of the 8T28 are used to drive the on-board bus and receiver gates are used for the off-board bus. Low cost and minimum component count make the 8T28 ideally suited for such double-buffered applications.

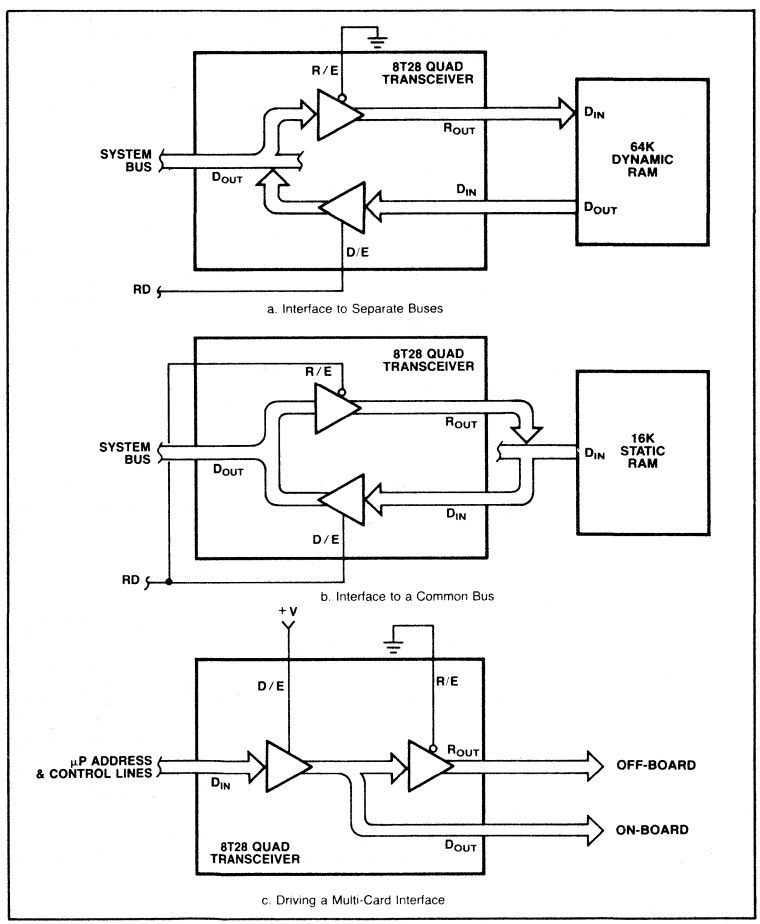


Figure 3. Using 8T28 Transceiver to Obtain Optimum Interface Flexibility

MEMORY ADDRESS DECODING

In any computer system, information on the address bus must be decoded to generate select signals for memory and any I/O peripherals. There are numerous decoding schemes and a variety of implementation techniques. Generally, the methods used depend on system complexity which, in turn, depends on memory size, mapping parameters, access time, the particular technology, etc. Although simple decoders are frequently used in uncomplicated systems, the more sophisticated applications use PROMs to

provide the required flexibility and to satisfy the mapping complexities that are usually encountered.

To develop trouble-free decoding circuits, the designer must be aware of those areas that can degrade system performance. For instance, caution is advised when using decoder outputs to terminate data write cycles. When read/write strobes (such as "E" on the 6801) are used to enable the address decoder, the data hold time is reduced because the trailing edge of the address decoder output now follows the trailing edge of the strobe signal to which the "hold time" is referenced. In systems that are sensitive to hold time, read and write strobes should not be used to enable address decoding circuits. Instead, the strobes should be gated with the decoder outputs to reduce the hold time.

Signetics makes a wide range of decoders, demultiplexers, and PROMs that are suitable for both simple and complex decoding functions. Some of the more common decoding applications are summarized in Figures 4 through 7.

OPERATION & APPLICATIONS SUMMARY

For small uncomplicated systems, the 74F138 decoder provides a cost-effective interface between the system address bus and memory. The configuration shown above is not only economical, it is fast, uses very little power, and requires no programming. Such systems are commonly used to generate contiguous memory addresses and to decode memory segments of equal size. With additional decoding circuits, the memory mapping capabilities of the system can be expanded.

Where speed is not a critical factor, the PROM decoder shown below adds considerable flexibility with no increase in chip count. The 82S123 can generate contiguous or non-contiguous address space and can be memory-mapped to satisfy the requirements of most applications. Although the PROM decoder is a bit more expensive and uses slightly more power, it has the advantage of being field programmable.

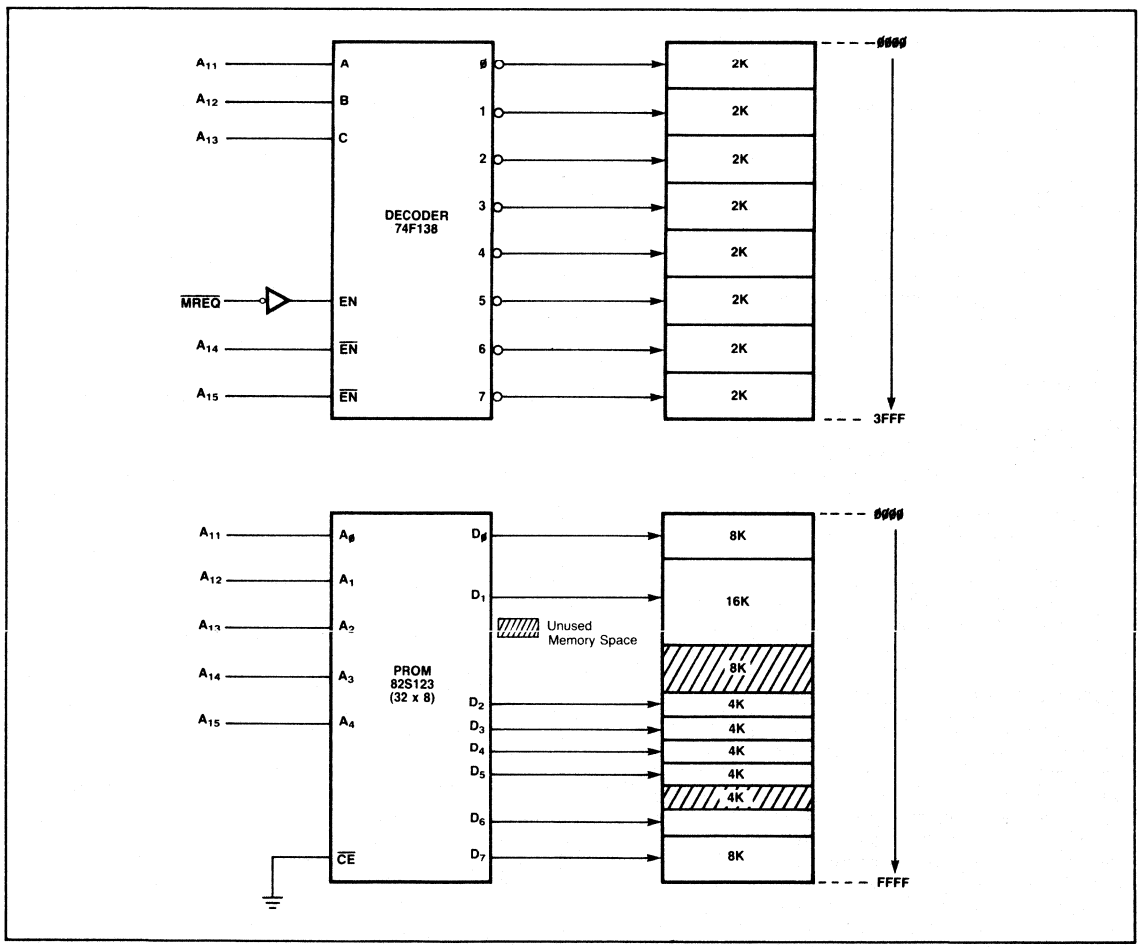
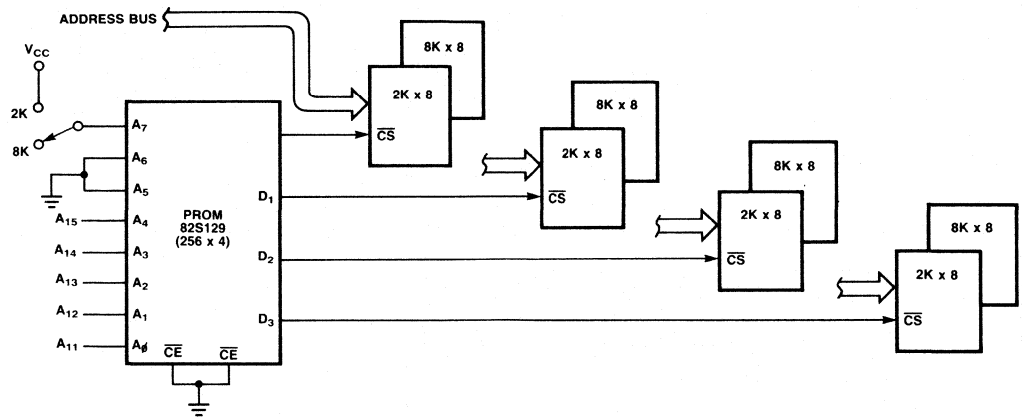


Figure 4. Two Simple Decoding Methods



PROM PROGRAMMING

PROM ADDRESS								PROM DATA				SYSTEM ADDRESS BUS
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	D_0	D_1	D_2	D_3	
1	0	0	0	0	0	0	0	0	1	1	1	0000–07FF
1	0	0	0	0	0	0	1	1	0	1	1	0800–0FFF
1	0	0	0	0	0	1	0	1	1	0	1	1000–17FF
1	0	0	0	0	0	1	1	1	1	1	0	1800–1FFF
0	0	0	0	0	0	x	x	0	1	1	1	0000–1FFF
0	0	0	0	0	1	x	x	1	0	1	1	2000–3FFF
0	0	0	0	1	0	x	x	1	1	0	1	4000–5FFF
0	0	0	0	1	1	x	x	1	1	1	0	6000–7FFF
ALL OTHERS								1	1	1	1	

Note:
1. Higher density memory devices can be used to meet the requirements of the system.

Figure 5. Switch-Controlled PROM Decoder

OPERATION & APPLICATIONS SUMMARY

The switch input to this PROM decoder permits easy upgrades to higher density memory arrays (up to 64K devices) without any hardware changes. Contents of the PROM for 2K and 8K devices are as shown. In this configuration, any number of memory maps can reside in the same PROM; output port lines or switches connected to the PROM address inputs can be used to select the appropriate memory map. As previously indicated in the general discussion, read or write strobes can be used to enable the PROM; however, this delays the trailing edge of the chip selects and reduces the data hold time. For systems sensitive to hold time, it is recommended that the read/ write strobes be used to drive multiple enables on the memory array or that the PROM outputs be gated.

The chief advantages for this type of decoder is simplicity, the ability to change memory mapping for memories of different densities, and the flexibility of programming address changes for the memory devices.

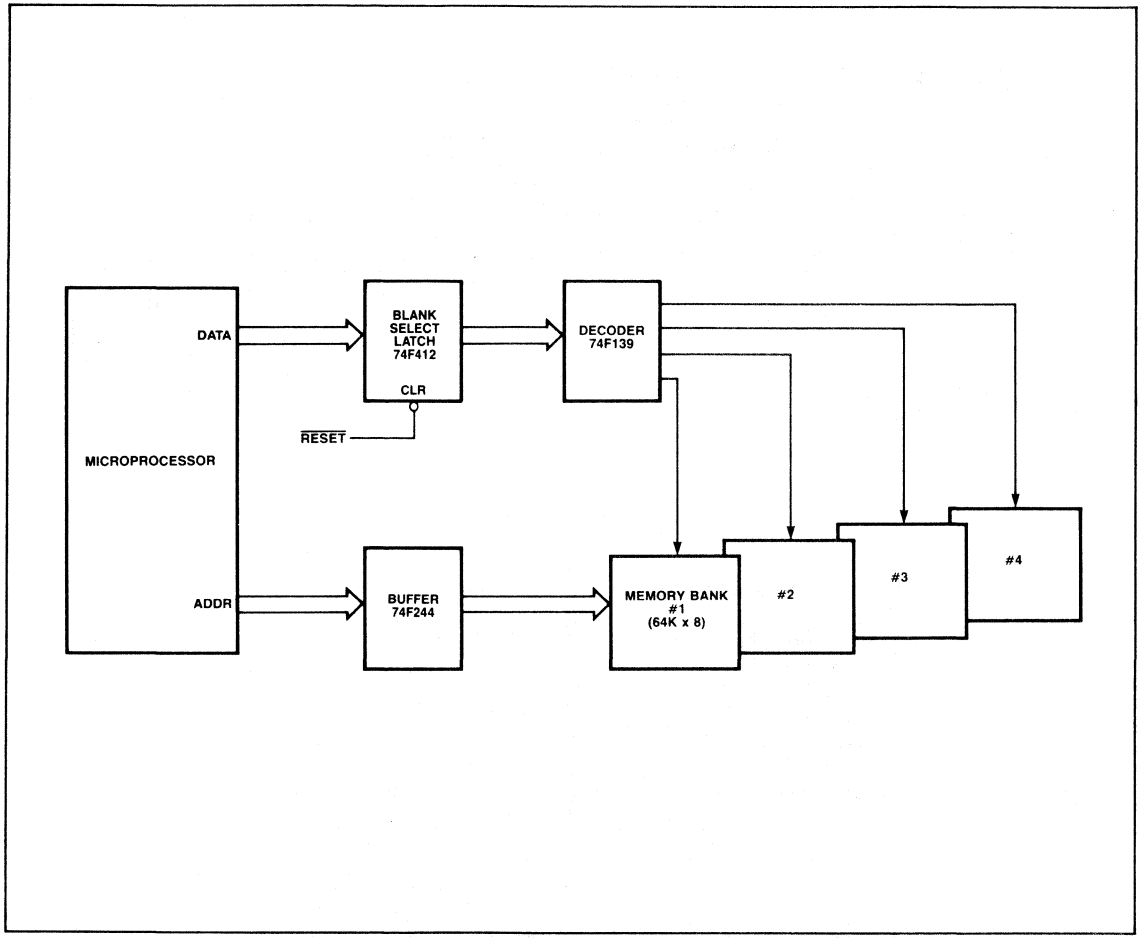


Figure 6. Extending the Logical Address Space Via Bank Switching

OPERATION & APPLICATIONS SUMMARY

In some applications, it is desirable for the system memory to extend beyond the logical address space of the processor. As shown, such a system can be easily implemented with a few interface parts and a bit of software. The four memory banks are wired in parallel; each bank can be as large as the logical memory space of the microprocessor — 512 bytes for 8-bits of address and 64K for a 16-bit address bus. An output port under software control selects the active bank; the bank address is decoded to ensure that only the appropriate memory bank is enabled. In this way, the possibility of bank contention is eliminated.

Memory allocation schemes such as these are frequently used in multiprocessor environments and, in this type of application, a copy of the operating system kernel must reside in each memory bank. The system can be enhanced by providing direct switching between the memory banks; however, additional hardware is required for such operations.

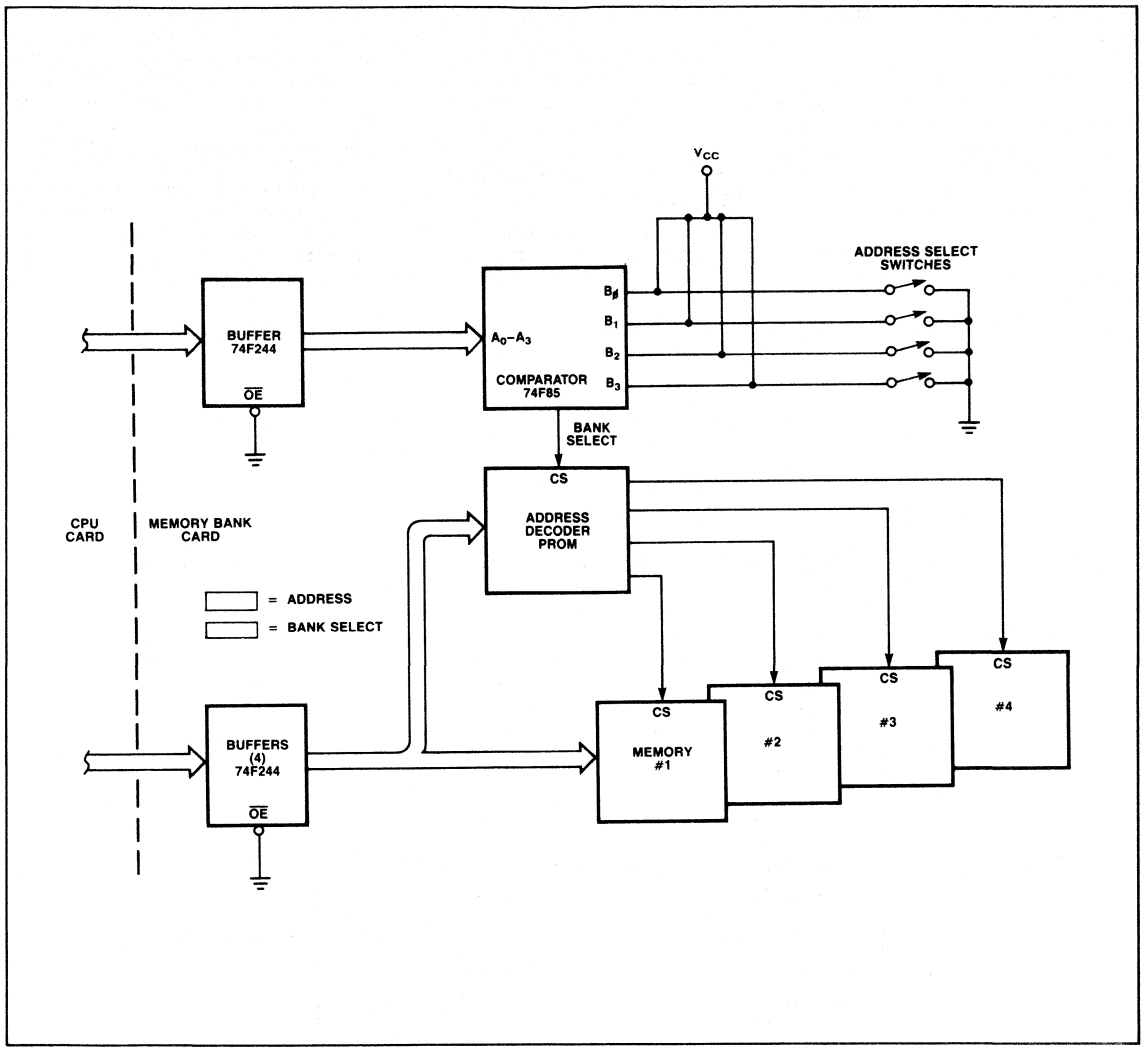


Figure 7. Multi-Board Decoding System with Extended Address Space

OPERATION & APPLICATIONS SUMMARY

In a multi-board system, the address decoding and memory-bank select functions can be implemented as shown here. The bank address on the memory card is identified by setting the address select switches of the comparator to a predetermined configuration. When the bank select signals from the CPU card match the preset bank address, the PROM is enabled and the appropriate memory bank is placed on-line. Data bus control for the system is not shown.

The system shown in Figure 6 and the one shown here are similar in that the four memory banks are wired in parallel and each bank can be as large as the logical address space of the microprocessor.

USING FAST ICs FOR μP-TO-MEMORY INTERFACES App Note 205

SPECIAL MEMORY-INTERFACE CIRCUITS

In some applications, the memory interface circuits must be adapted to the unique requirements of the system. For instance, a system may use devices whose response time and wait-state requirements are vastly different, necessitating programmed wait states for optimum throughput.

Other examples include capturing a high-speed bit stream without the use of high speed (high cost) memories, refreshing dynamic RAM via interleaving, and minimizing leakage problems when driving open-collector buses. Figures 8 through 11 show how Signetics ICs can be used to solve interface problems of this type.

OPERATION & APPLICATIONS SUMMARY

Using the "slowest" device in the system as a reference for data through-put is a gross waste of processor time. ROM is usually slower than RAM, and I/O devices are generally slowest of all. One way of reducing the harmful effects of these diverse characteristics is to program wait states for each device such that inactive periods for the CPU will be minimized. With the PROM decoder in the system shown above programmed in this manner, the multiplexer selects the appropriate tap of the shift register to initiate the required number of wait states. The wait cycle is terminated when a "1" is shifted to the selected tap; the shift register is cleared at the end of each wait-state cycle.

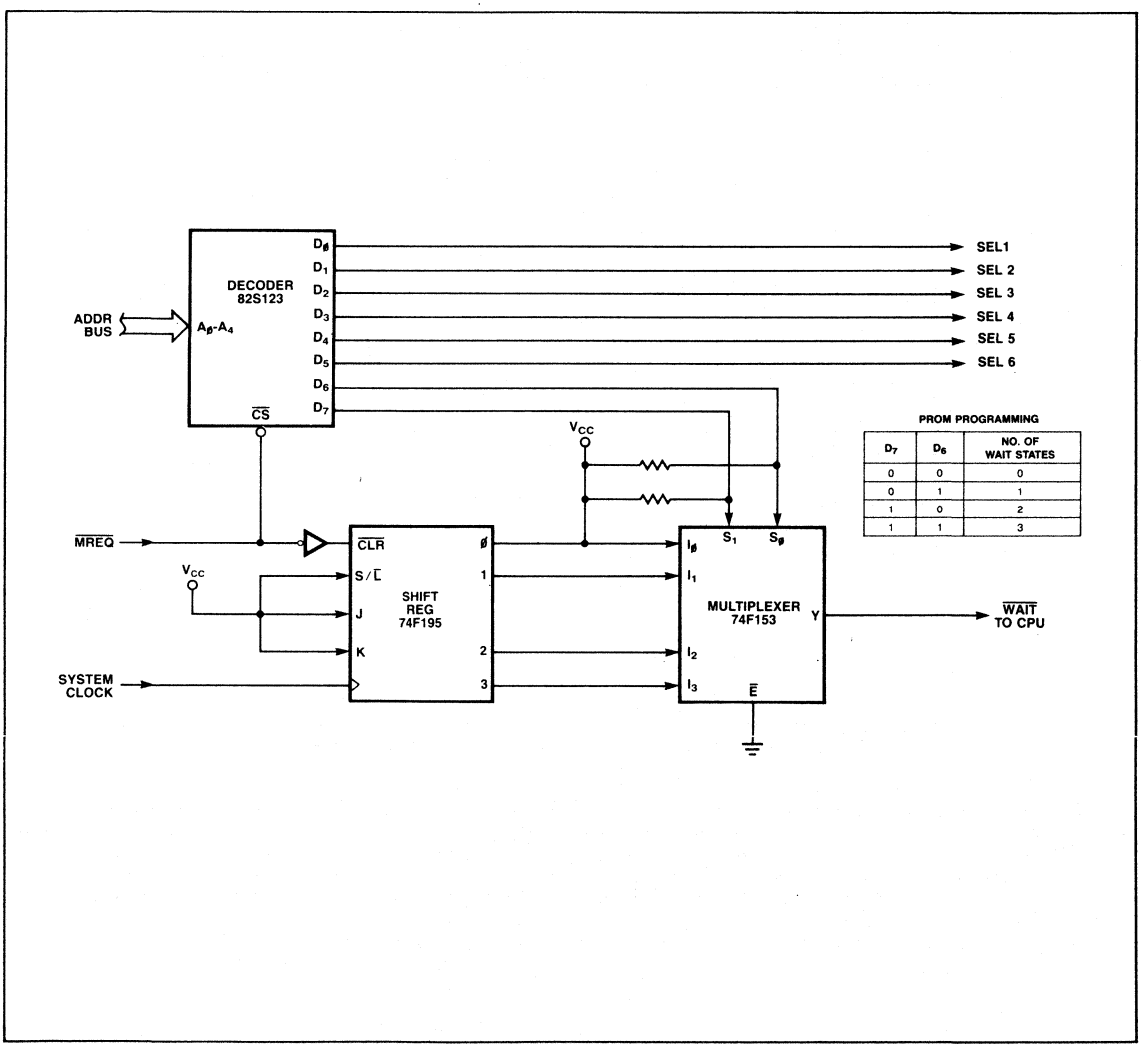


Figure 8. Programming Wait States to Optimize Data Throughput

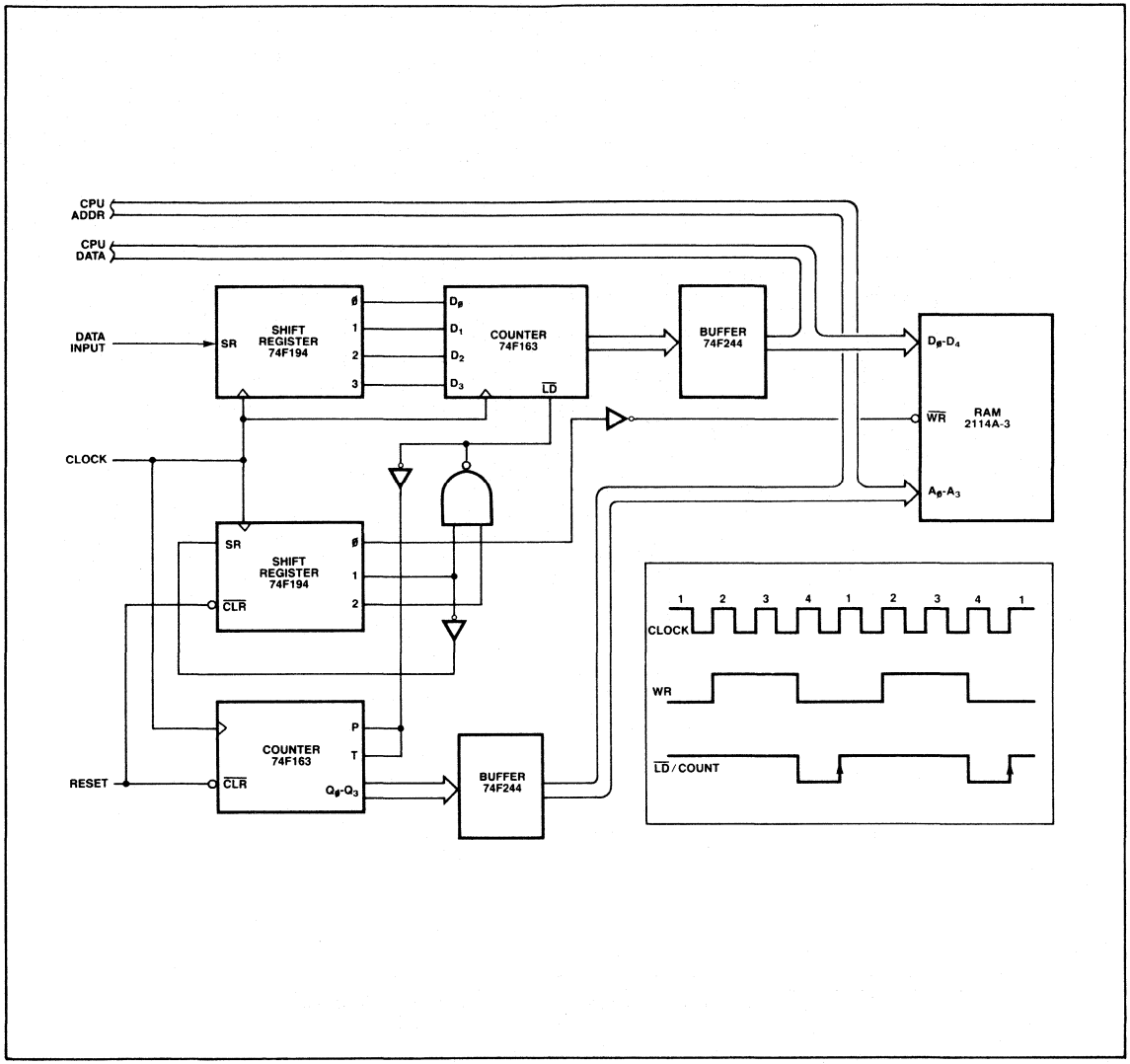


Figure 9. Storing High-Speed Serial Bit Stream with Low-Speed RAM

OPERATION & APPLICATIONS SUMMARY

In the design and use of logic analyzers, disk media, modems, and other similar equipment, a high-speed serial bit stream must be stored in memory. The above system shows how a 20 MHz serial data stream can be captured and stored in a relatively low-speed RAM that has a 5 MHz (200ns) cycle rate. The system uses a simple parallel to serial converter, thus, saving the cost of high-speed memory devices. Other than the synchronizing clock being supplied by the serial-input system and the setup/hold times of the shift registers being met, operation is simple and straight-forward.

- Incoming serial data is clocked into shift register.
- After each fourth bit, data is transferred in parallel to a 4-bit counter (74F163) used as a latch.
- Data is written into RAM while four new bits enter shift register.
- Memory addressing is performed by incrementing the 74F163s and timing is controlled by a simple ring counter.

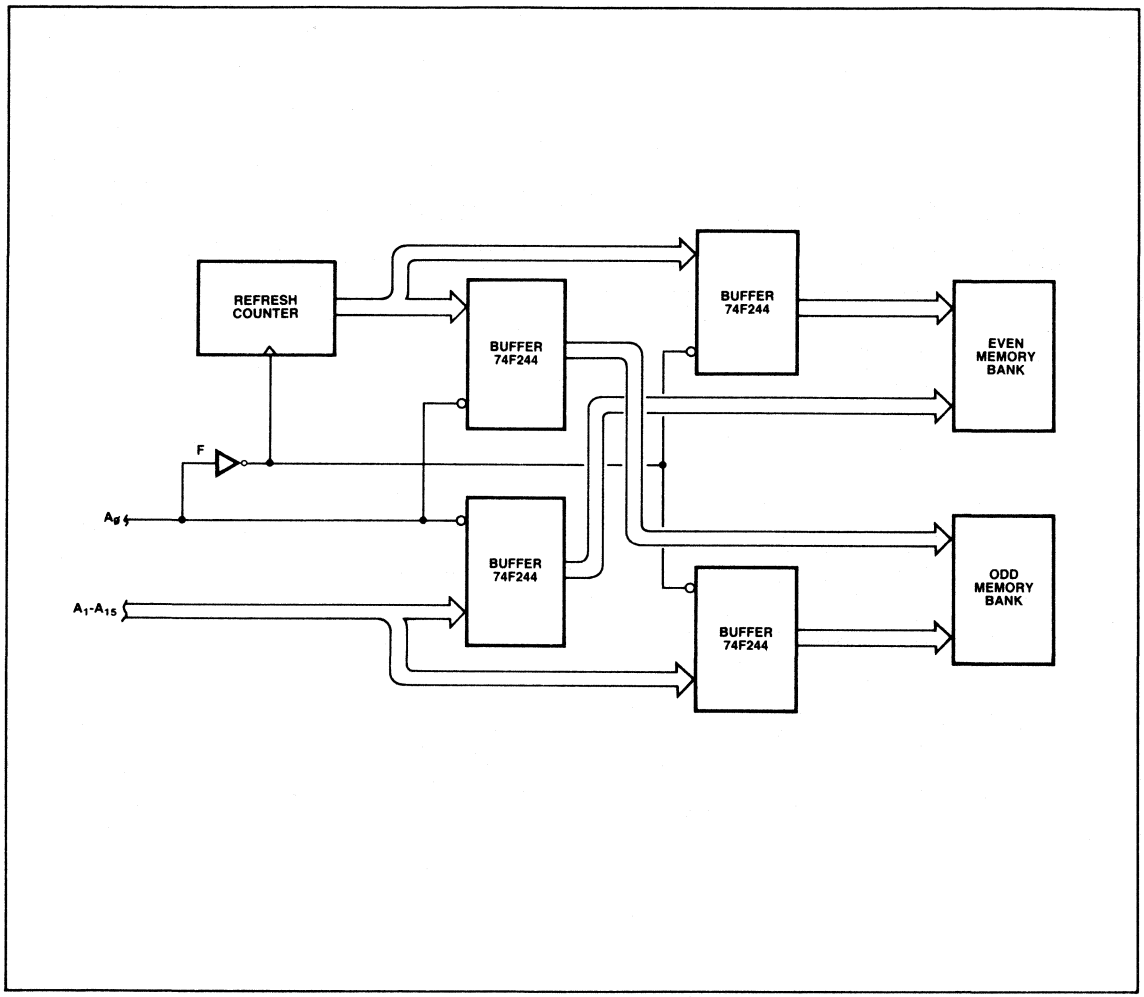


Figure 10. Using Interleaving Technique to Refresh Dynamic RAM Memories

OPERATION & APPLICATIONS SUMMARY

Most dynamic RAMs must be refreshed at least every 2-milliseconds to ensure retention of valid data. One method of memory refresh is shown in the above example. This system uses interleaving and relies on the premise that, during normal program execution, A_0 toggles frequently enough to refresh the RAM without slowing the microprocessor with wait-states or DMA cycles to refresh the counter. If the system program uses wait-states, halt instructions, or address incrementing is otherwise limited, A_0 may not toggle at a rate sufficient to accomplish refresh. For such situations, additional circuits or special programming may be required to prevent loss of data. Operation of the system can be summarized as follows:

- When even bank is addressed by CPU, odd bank is refreshed by address counter.
- Even bank is refreshed when CPU addresses the odd bank.
- A_0 increments the refresh counter before each odd-bank refresh.

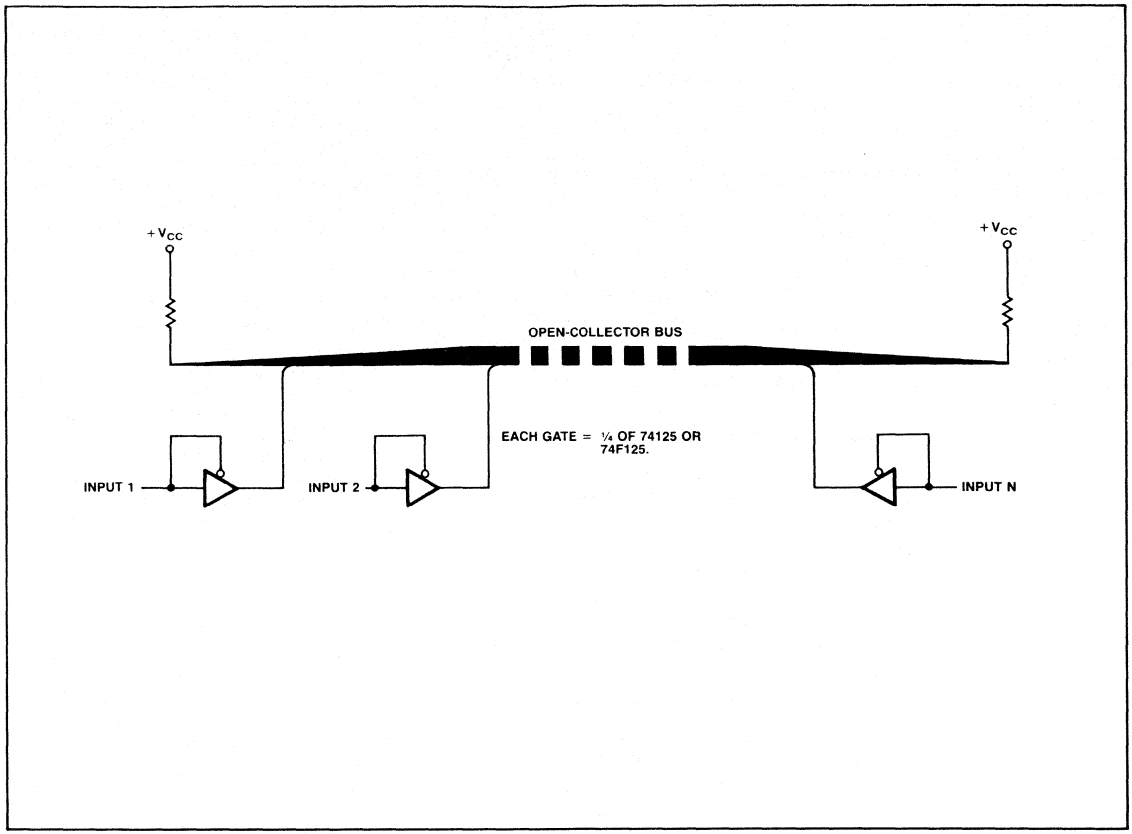


Figure 11. Reducing Leakage Current When Driving Open Collector Buses

OPERATION & APPLICATIONS SUMMARY

The number of buffers (7406 type) that can share an open-collector bus is often limited by device leakage or by the increased power consumption caused by lowering the values of the pullup resistors. A method of reducing the leakage current is shown in the above example. Here, the logic input and output enables of each gate are tied together; thus, the gate output is floated high to drive the open-collector bus. Floating the gate outputs provides a significant reduction in leakage current which allows the use of more gates and/or reduced power consumption by the pullups.

SUMMARY

Many of the applications and concepts provided in this document were direct contributions or heavily influenced by entries in the Signetics' Interface Circuit Design contest. Our special thanks to those individuals whose entries are referenced in whole or in part.

As integrated circuits become more and more complex, fewer and fewer parts are required to implement a functional system; thus, interface support is a major consideration in the overall design process. To produce a competitive and cost-effective product, the user must choose interface components that are efficient, reliable, and those that reflect the best features of current technologies. Signetics has met these challenges in the past and will continue to meet them in the future, providing silicon solutions that are truly state of the art — be it logic, memories, gate arrays, or other. For further documentation and/or applications assistance, call or write to your nearest Signetics Sales and Service Office — there is one near you.

USING μP I/O PORTS WITH FAST LOGIC App Note 206

INTRODUCTION

Signetics interface ICs are most often used to implement input and output ports in microprocessor based systems. This application note illustrates the effective use of Signetics FAST devices to interface microprocessor data and address buses to general purpose I/O ports. Topics illustrated include handshaking, multiplexing, arbitration, and bit manipulating. More complex circuits involving memory interfacing, shared memory, and multiple processors are covered in other application notes.

Simple I/O Ports

The simple Input/Output ports shown in Figure 1 use 74F374 octal flip-flops and 74F244 octal 3-state buffers to interface to a microprocessor's data bus. The input port is enabled by $\overline{RD}$ AND $\overline{PORTSEL}$. The output is enabled by $\overline{WR}$ and $\overline{PORTSEL}$.

When 16 pin packages are preferable to 20 pin packages for physical design considerations, 3-state multiplexers may be used as input ports. In Figure 2, 74F257 quad two-input multiplexers are used. A_0 selects between port A and port B.

In Figure 3, a 74F373 octal transparent latch is used to drive a light emitting diode annunciator array. The output follows the data bus while E is high, and the display freezes when E goes low. The 20 mA sink current of the 74F373 permits interface to most LED devices.

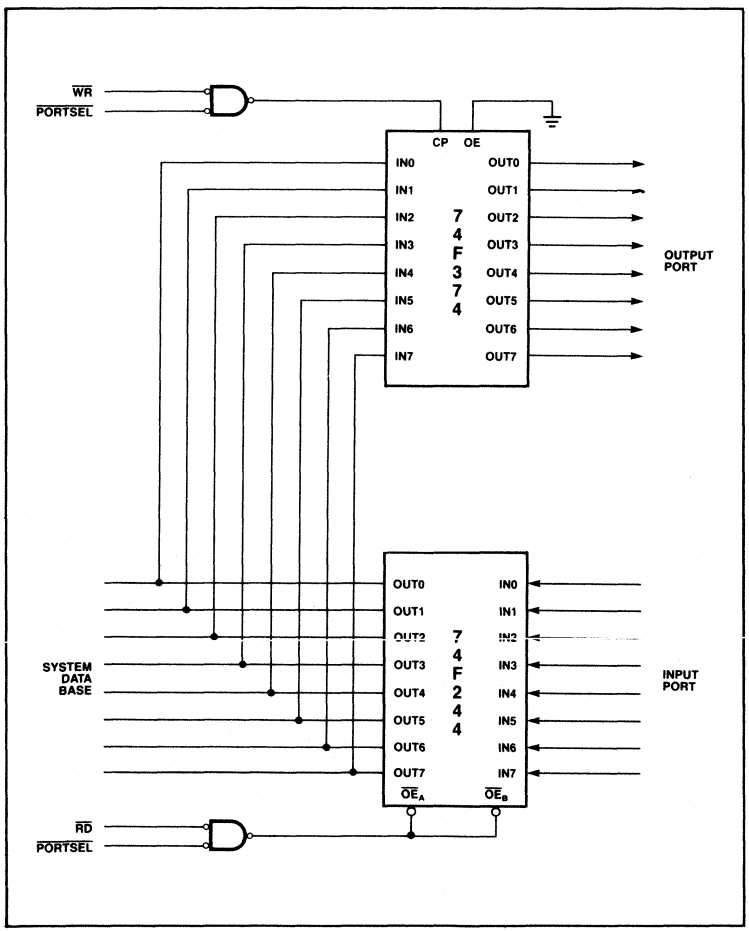


Figure 1. Simple Input/Output Ports Interface With Microprocessor Data Bus

A potential hazard exists when using transparent latches as output ports. The timing diagram of Figure 4 shows that data may not be valid when E is brought high, causing invalid data to be present on the output for a brief period. This will not cause a problem when driving LEDs because the duration of the invalid data is too short to be seen. But, problems will occur if the outputs are used to trigger other circuits that cannot tolerate glitches. Flip-flops should be used instead of transparent latches when these conditions exist.

Interfacing microprocessors to slow peripherals, such as printers, usually requires handshaking logic. In Figure 5, the 74F374, 3-state octal flip-flop acts as an output port for the microprocessor and as an input port for peripheral. The microprocessor writes data to the output port which sets /data available low. The peripheral then reads input port which sets /data accepted low and /data available back to high. The low /data accepted line interrupts microprocessor indicating that peripheral is ready for another data transfer.

Bit Manipulation

In Figure 6, the 74F251, three-state 8 to 1 multiplexer provides a bit-oriented input port. This technique permits processors which do not have built-in bit manipulating capability to examine single bits at input ports efficiently. In addition, parallel inputs may be read bit-serially over a single data line. Address lines A_0, A_1, and A_2 select the bit to be read, and data bus line D_7 is selected to permit a simple software decision based on JUMP-ON-SIGN or SHIFT-LEFT & JUMP-ON-CARRY.

A versatile bit-oriented output port may be implemented with a 74F259, eight-bit addressable latch as shown in Figure 7. With this technique single output bits may be manipulated without maintaining a copy of the output port contents in memory. This is useful in bit-oriented control appplications. The addressable latch effectively performs serial to parallel conversion on data supplied from the system bus. Data is written to 1 of 8 output bit locations specified by address lines A_0, A_1, and A_2.

Caution: Address inputs must be stable before latch is enabled or data can be entered into incorrect locations. If output glitches cannot be tolerated, data input must also be stable before the latch is enabled.

A similar technique is used in Figure 8, to accomplish bit manipulation without using the data bus. Each bit is associated with two addresses. If A_0 is high, the bit is set high; if

A_0 is low, the bit is set low. With this approach bit-manipulation is faster and requires less program memory because data does not have to be loaded and output from the accumulator. Also PCB layout complexity is reduced by removing the data bus from the output port.

I/O Timing

In many applications it is necessary to adjust timing to match microprocessor specifications to bus specifications. For example, the MC6809 microprocessor has data write hold time of 30ns, making it difficult to interface to peripheral chips such as floppy disk controllers that have longer hold time requirements.

Figure 9 extends this hold time for interface to slow peripheral devices. A 74F373 3-state octal transparent latch is used to freeze data on I/O bus during write operations. During read operations, the 74F373 outputs are floated and data is read through the 74F244 3-state octal buffer.

Figure 10 shows the timing diagram for an I/O bus with extended hold time. During the write cycle, data is latched by 74F373 on the falling edge of E. Data remains on the outputs of the 74F373 until the rising edge of Q at the beginning of the next cycle, when the outputs are floated. The read cycle is unaffected. Data hold time is extended to ¼ cycle —from 30ns to 250ns for a 1MHz cycle rate. Note that a latch is used instead of a flip-flop to preserve the data setup time of the 6809.

A dedicated hardware solution is faster in systems requiring high throughput rates where the required function is performed frequently. In Figure 11, a 74F374 3-state octal flip-flop is used as both input and output port. By jumpering the output data lines of the 74F374 to different system data bus lines, various dedicated functions can be realized—examples are nibble swapping, bit transposing, and data encryption. The software to perform data manipulation is simple —data is written to the octal flip-flop, and manipulated data is read back into the processor using the following instructions:

```
OUT    (DATA MANIPULATOR), A
IN     A, (DATA MANIPULATOR)
```

BIBLIOGRAPHY

Many of the applications illustrated in this note were contributed or influenced by entries in Signetics' Interface Circuit design contest. Special thanks are due to the following individuals whose entries were referenced in whole or in part in this note:

V.K. Agrawal
Timothy Anderson
Wiley M. Bird
James A. Ciarpella
Mark Forbes
Loren H. Johnson
Prakash R. Kollaram
G.B. Livingston
Joseph Mastroieni
Jonathan A. Titus
Eugene M. Zumchak

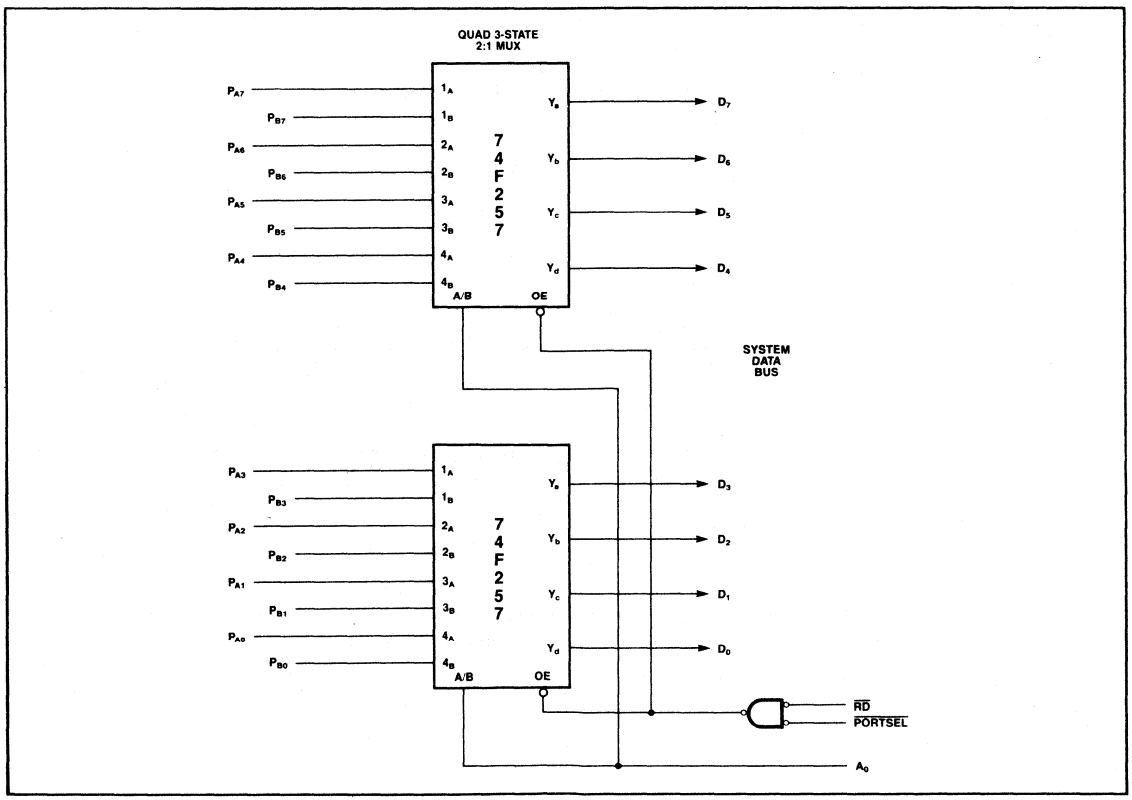


Figure 2. Use of 3-State Multiplexers as Input Ports

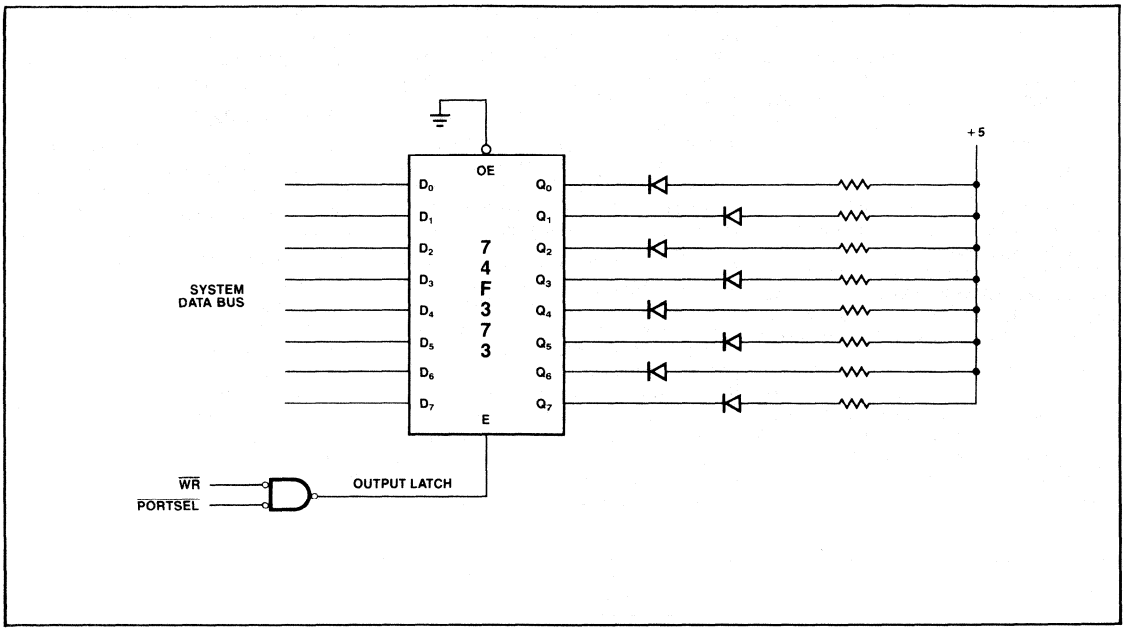


Figure 3. Output Port Driving LED's Using 74F373 Octal Transparent Latch

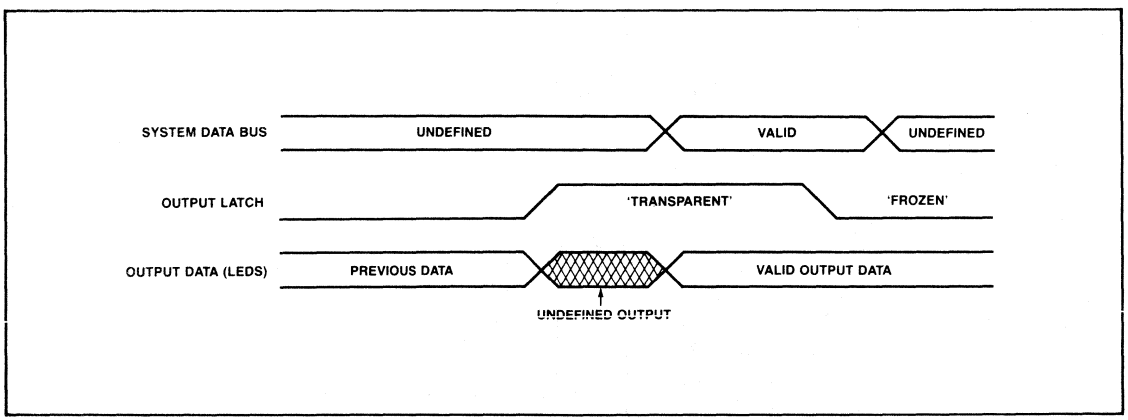


Figure 4. Potential Hazard Exists When Using Transparent Latch as Output Port

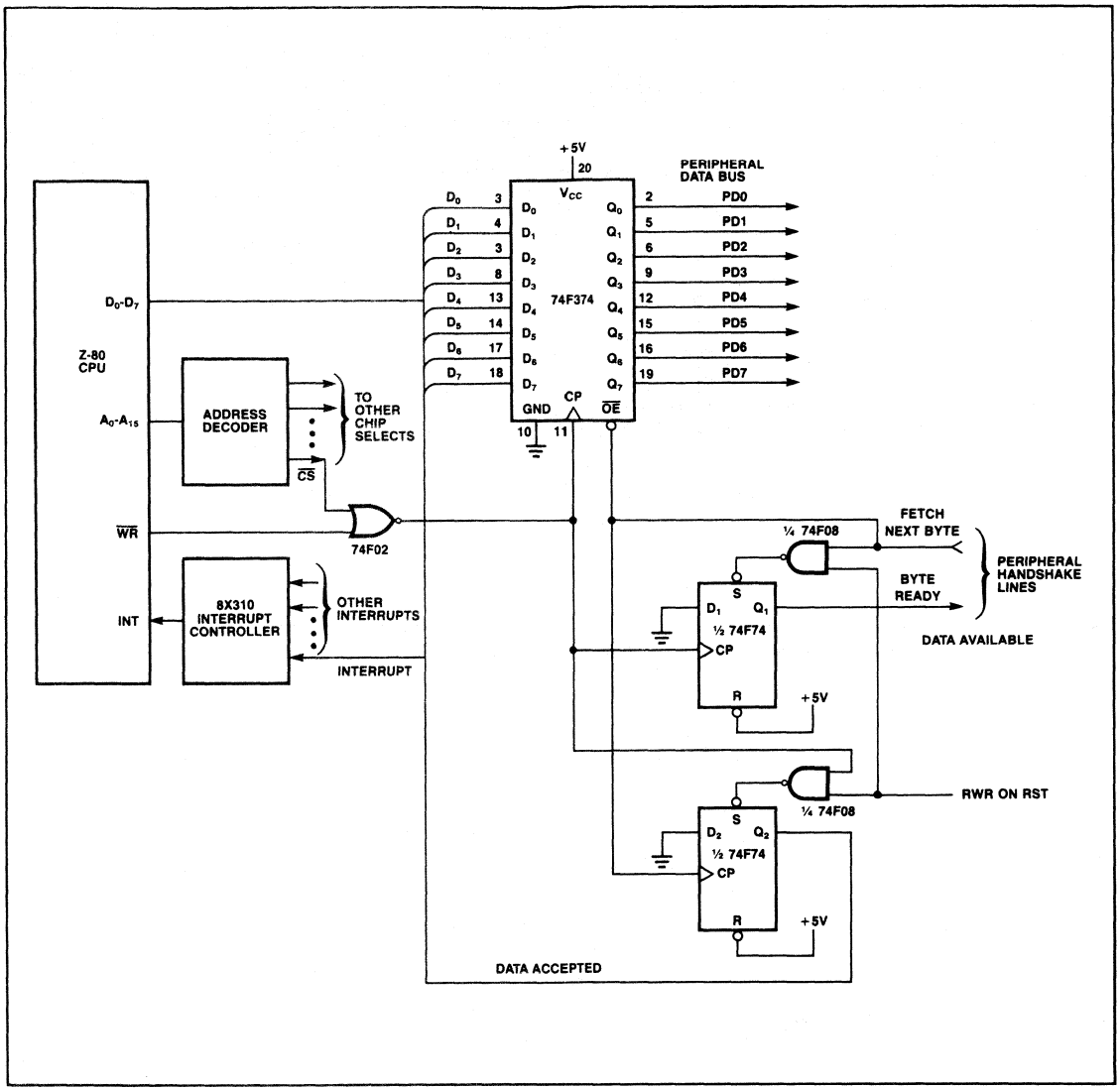


Figure 5. Interfacing Microprocessors to Slow Peripherals, Such as Printers, Using Handshaking Logic

6

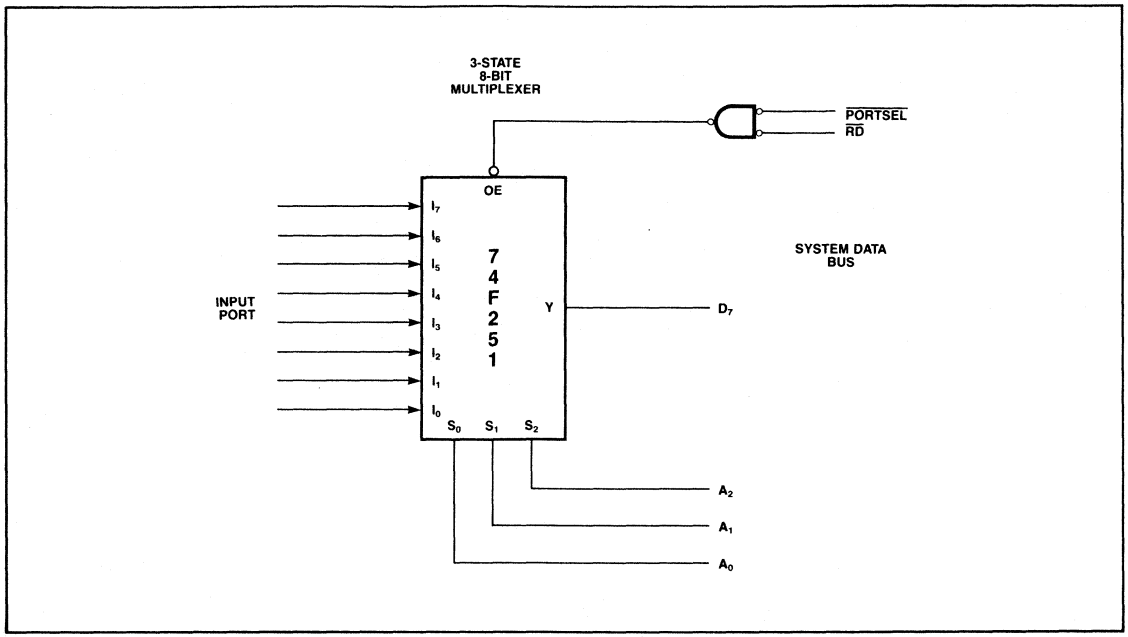


Figure 6. Three-State 8 to 1 Multiplexer Provides Versatile Bit-Oriented Input Port

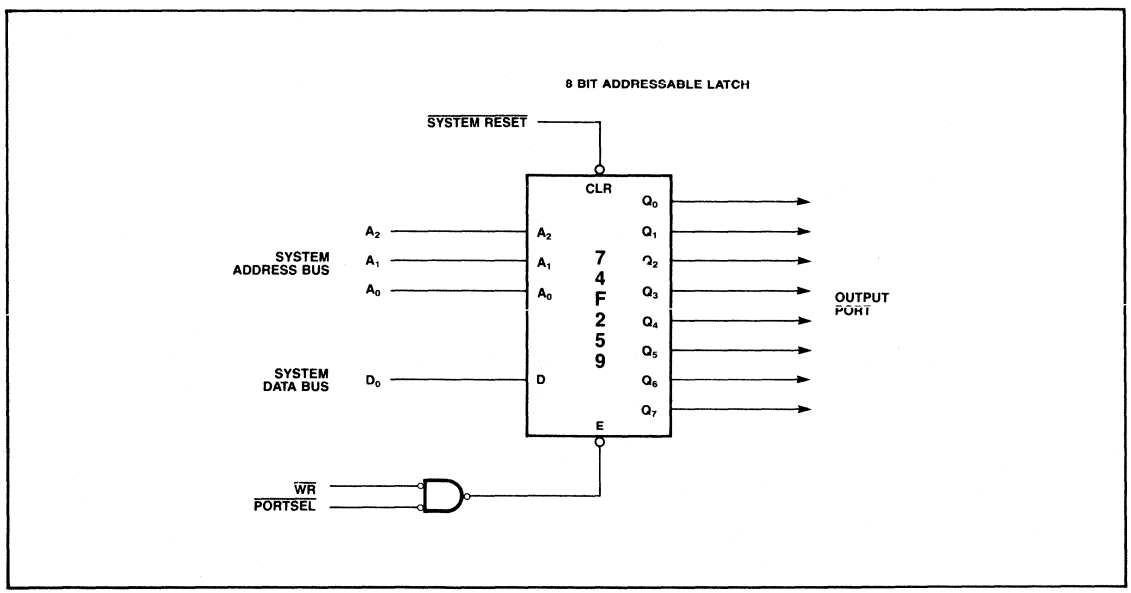


Figure 7. Eight-Bit Addressable Latch Provides Versatile Bit-Oriented Output Port

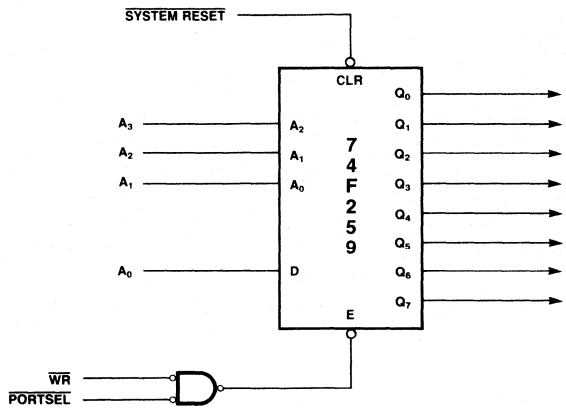


Figure 8. Bit Addressable Output Port Does Not Require Data Bus

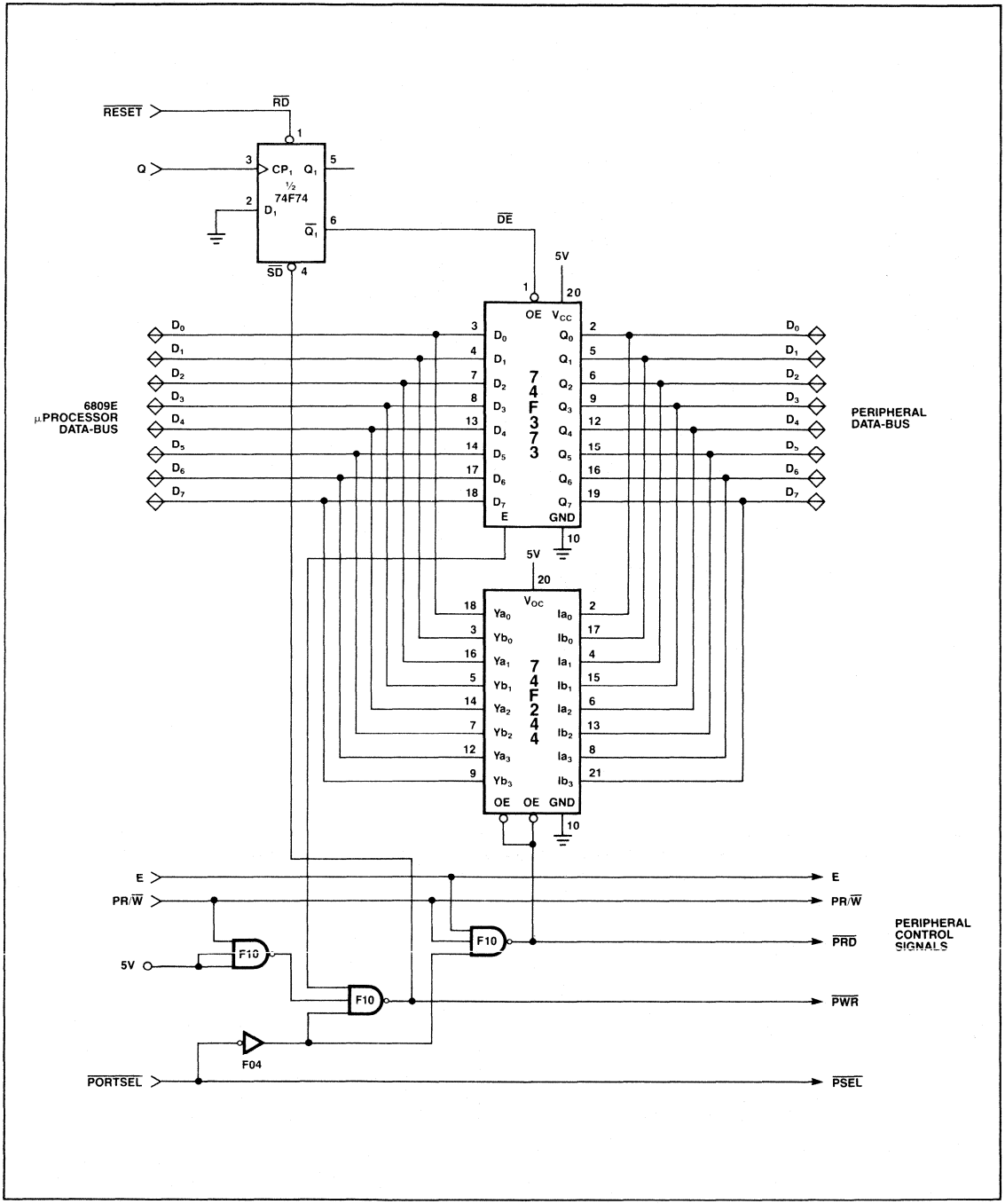
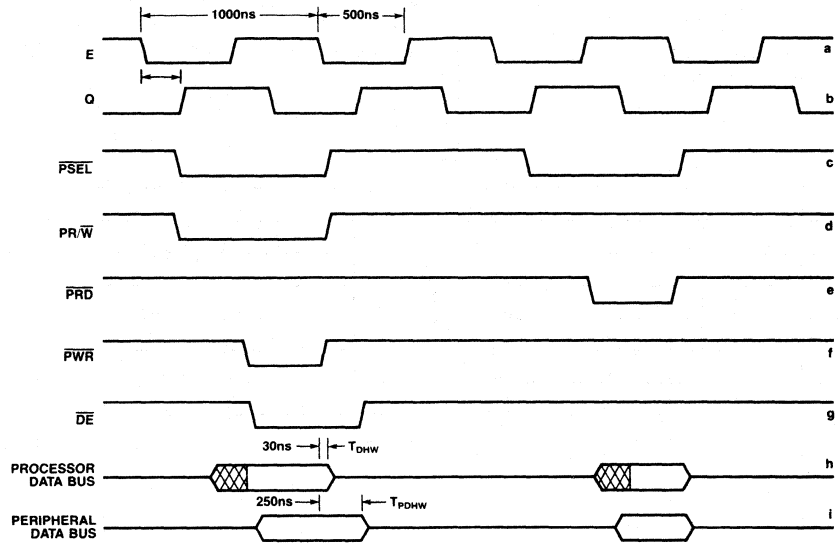


Figure 9. Hold Time Extended for Interface to Slow Peripheral With MC6809 Microprocessor



NOTES:
1. RESET - Power on reset
2. Q - 6809E Processor clock (1MHz shown)
3. Q - Quadrature clock for 5809?
4. DE - Peripheral bus driver enable
5. PR/W - Peripheral READ/WRITE
6. PSEL - Peripheral select
7. PRD - Peripheral read
8. PWR - Peripheral write
9. T_{DHW} - 6809E Output data hold time
10. T_{PDHW} - Peripheral write data hold time

Figure 10. Timing Diagram for I/O Bus With Extended Hold Time

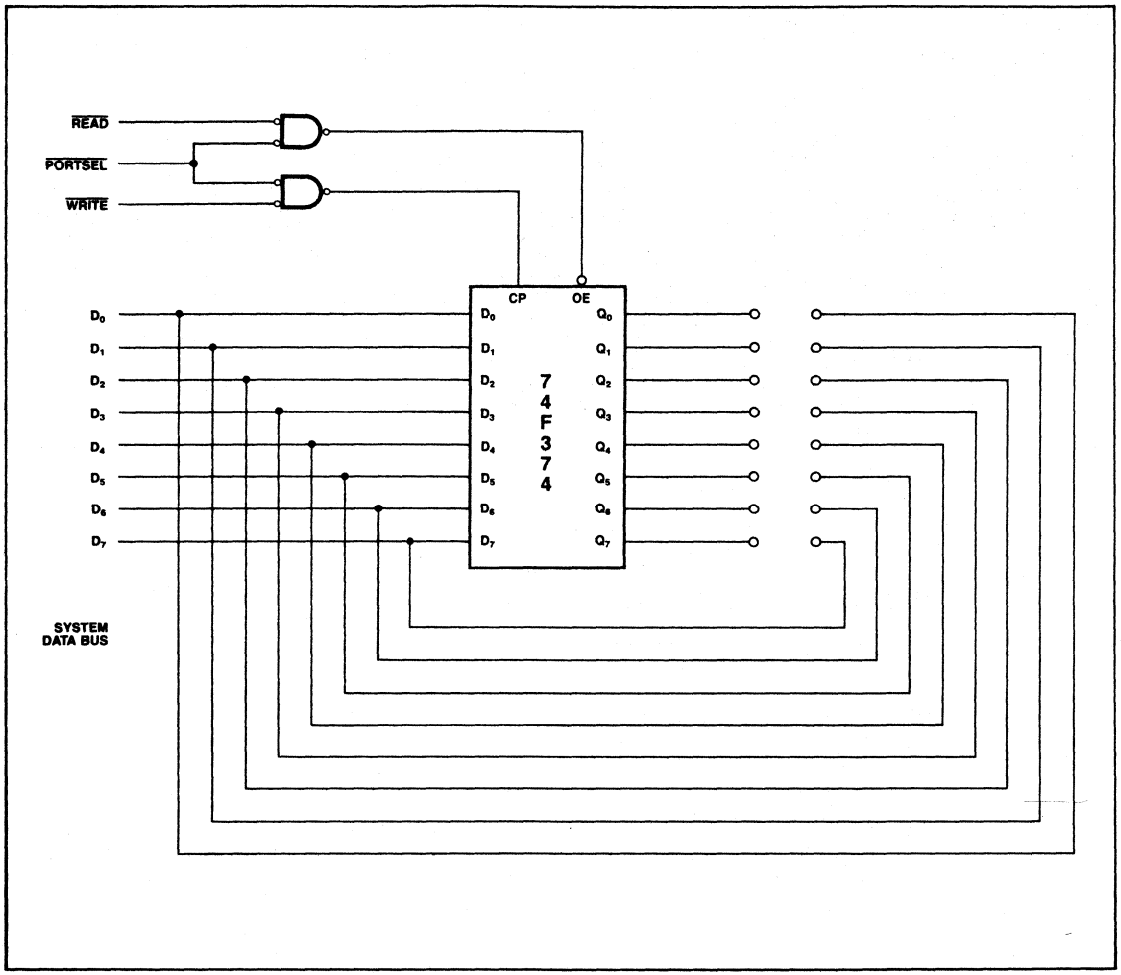


Figure 11. Data Manipulator Uses Dedicated Hardware

MULTIPLE μP INTERFACING WITH FAST ICs App Note 207

INTRODUCTION

As microprocessor costs continue to decrease and the demands on product performance continue to increase, designers are increasingly turning to multiple microprocessor systems to meet the performance challenge. The introduction of many "peripheral controller" type processors has made this choice even more attractive. This application note addresses typical problems associated with interfacing multiple microprocessors, and illustrates the use of Signetics Interface Circuits in solving these problems.

A multi-processor system contains two or more processors communicating through parallel ports, multi-port memories, serial data links, and/or shared buses. The most popular multi-processor architectures are "loosely coupled" systems. In loosely coupled systems each processor operates asynchronously with the other processors, usually performing a separate function. Communication is not continuous, and occurs only when necessary.

A special application for multiple microprocessor systems is in redundant systems. As the price of microprocessors dropped, it became economically feasible to achieve greatly increased reliability by employing several processors operating in parallel, performing identical functions. After each operation a vote is taken on the result. If there is disagreement, a fault has been detected, and appropriate corrective action can be taken. Appropriate action might be switching in a third processor, repeating the process, or activating an error sequence and/or an alarm.

In the typical loosely coupled multiple processor system of Figure 1, a main processor "delegates" processing work to four other processors. A keyboard scanner microprocessor scans the keyboard continuously, debounces key closures, performs code conversions, and transmits key codes to the main processor in a format that it can easily assimilate. A separate arithmetic processor accepts parameters from the main processor, performs arithmetic calculations, and provides the results for the main processor to read when it is not busy with other tasks. The display controller accepts data and commands from the main processor, then displays and manipulates data on CRT or other displays. The display controller refreshes the display and supports graphic displays without tying up the main processor. The print spooler is a separate processor that accepts files to be printed from the main processor using high speed data transfers. Then the print spooler stores and feeds data to the printer at the printer's lower data rate, freeing the main processor for other chores. Each processor module contains its own "local" ROM, RAM, or I/O, so that it performs its task independently, and communicates with other processors only when necessary. As a result, the system as a whole operates closer to its maximum speed.

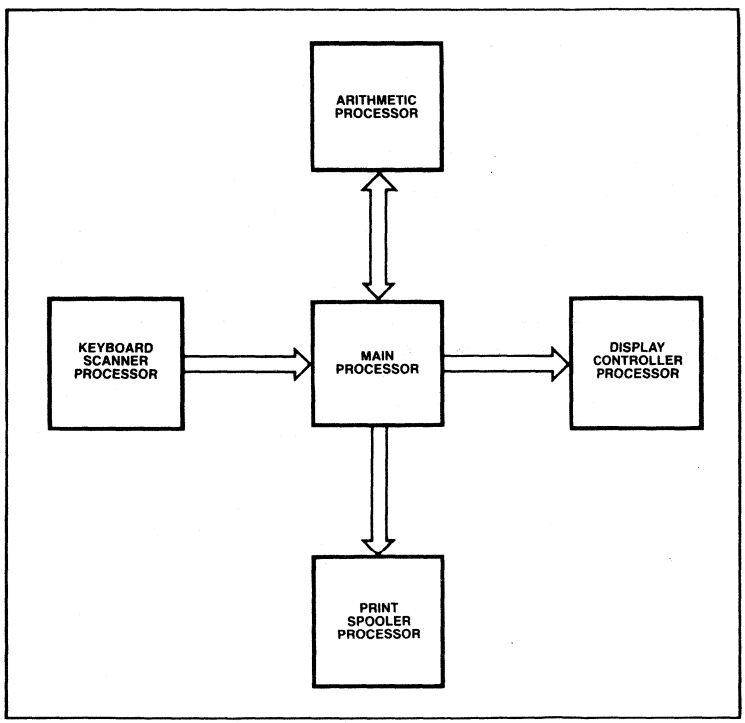


Figure 1. Typical Multi-processor System

Some of the advantages of multiple microprocessor systems are:

- Each processor performs a relatively independent task.
  - —Design is easily split among team members.
  - —Testing is easily performed on a modular level.
  - —Modules can be added or modified without affecting other modules.
- Multi-processing allows distributed processing where modules may be physically separated from the main system.
- Parallel processing greatly increases system performance and throughput.
- Hardware cost is less than single-processor systems with similar performance.
- Reliability can be increased easily by redundant processing.

The following application examples illustrate the use of Signetics FAST Interface Circuits in multiple processor systems.

PARALLEL I/O PORT COMMUNICATIONS

Figure 2 shows how parallel I/O ports using Signetics FAST Interface devices are used to accomplish simple 2-processor communications. Two 74F374 octal 3-state registers are used to implement bi-directional parallel data communication. Each 74F374 acts as output port to one processor and input port to the other. The handshake lines are needed when the processors operate asynchronously to ensure that data has been received before new data is transmitted. A handshake timing protocol (Figure 3) implemented in software acts as a traffic cop to assure valid data communications. The transmitting processor starts the handshake by setting Data Available to indicate that data is valid. The receiving processor sets Data Accepted to indicate data has been read. The transmitter then resets Data Available allowing the receiver to reset Data Accepted. The transmitter will not send new data until Data Accepted is reset.

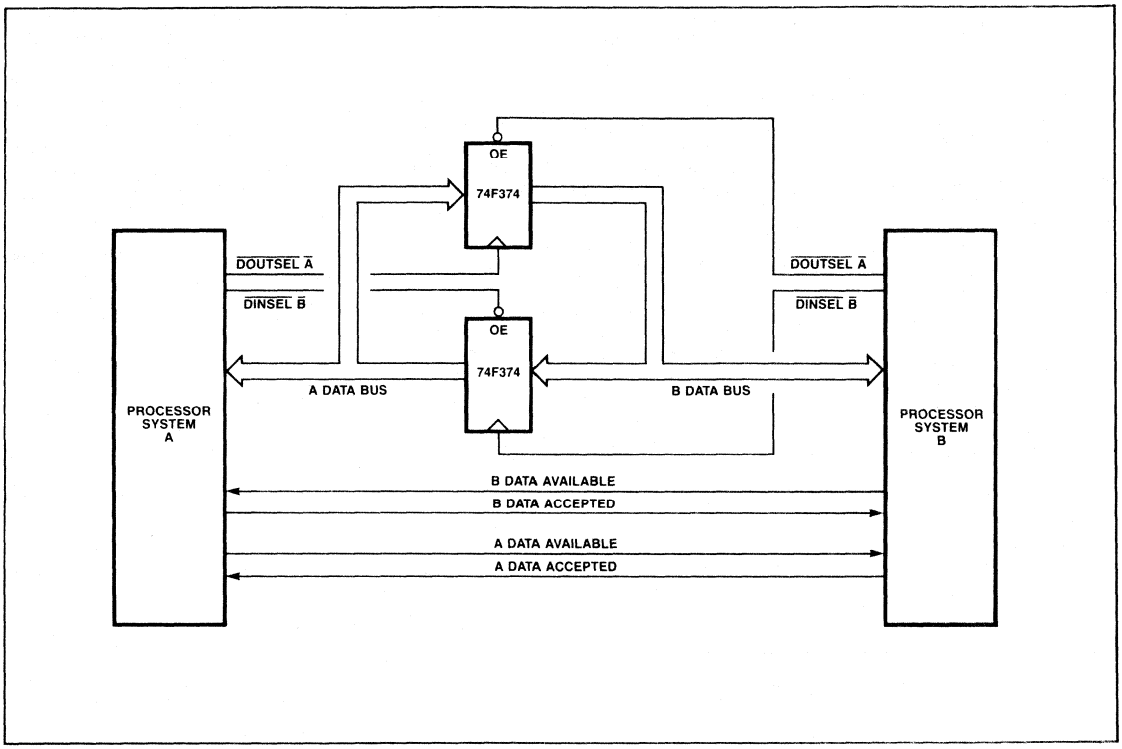


Figure 2. Basic Inter-processor Communication Using Parallel I/O Ports

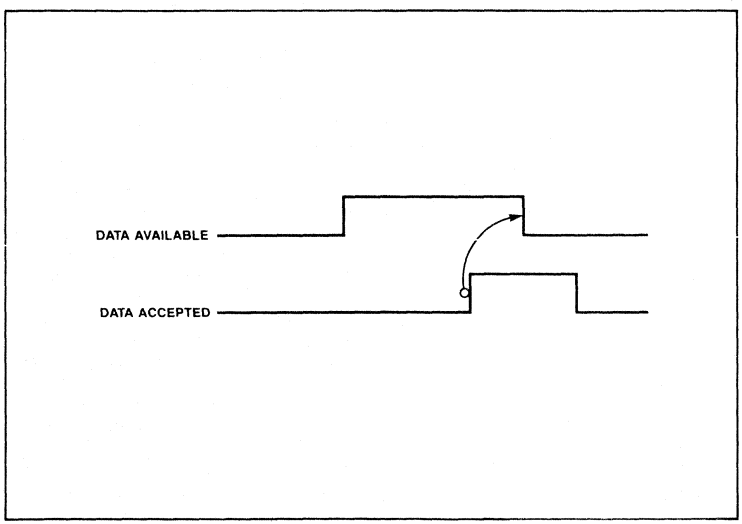


Figure 3. Handshake for Parallel Port Communication

COMMUNICATIONS VIA MULTI-PORT MEMORY

Figure 4 shows the logic required for two processors to communicate through a multi-port memory. The RAM is accessible from both processor A and processor B via 74F157 multiplexers used to select one processor's bus at a time. Multi-byte messages and data blocks may be written into the memory by one processor and read out by the other at a later time. No byte-by-byte handshake is required. The multi-port memory provides increased system performance at somewhat higher cost compared to a parallel port technique. Because of the use of multi-port memories in microprocessor systems, these systems can become quite complex. Another application note in this series covers interfacing to multi-port memories in greater depth.

SERIAL COMMUNICATIONS

Although serial communications between multiple processors is slower than the paral-

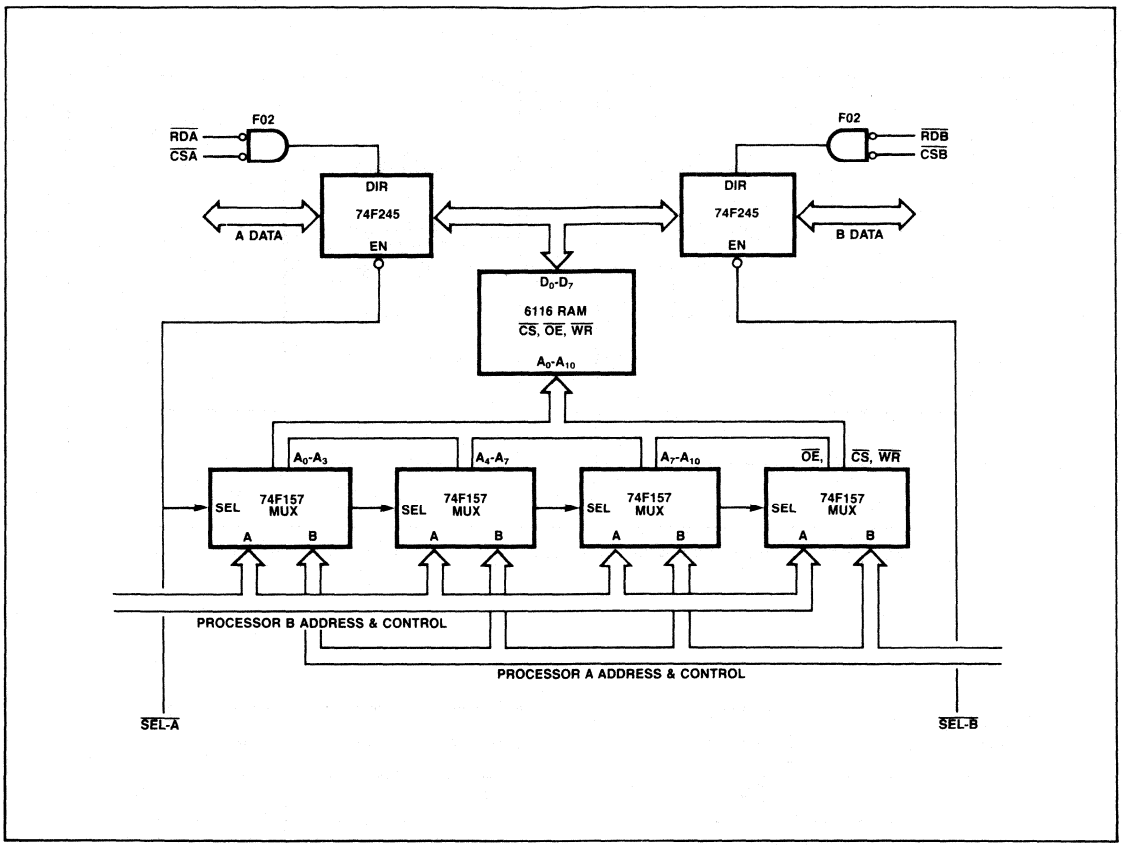


Figure 4. Multiport Memory Provides High-performance Multi-processor Communications

lel methods examined above, it is usually less expensive and very useful for communicating with remote units. Serial communications via RS-232 or RS-422 links can provide reliable communications over great distances. Implementation of serial communications is simplified by the availability of Universal Asynchronous Receiver Transmitter (UART) devices and well established standards for circuit interfaces and protocols. Figure 5 shows local/remote processor communication using Signetics SC2681 UART devices. In many cases additional interface lines are required for handshaking.

SHARED BUS ARCHITECTURE

One of the most powerful multiple processor architectures uses the popular shared bus concept. In Figure 6, each processor has its own local bus with some combination of RAM, ROM, and I/O available locally. The shared bus permits use of "global resources" such as global memory and global I/O which are accessible to all processors on the shared bus. Common interfaces such as printer ports do not have to be implemented for each processor, and may be connected to the shared bus. Multiple processors communicate indirectly with one another through the global RAM. This technique provides highest throughput when interconnecting more than two processors. It also reduces cost through sharing of global resources.

Any processor permitted to drive the system address, data, and control buses is known as a "master." Processors not having this capability are "slaves." A useful attribute of shared bus systems is the ability to add whole new functions by connecting a new master to the bus.

Figure 7 shows a typical shared system bus interface using Signetics Interface circuits. Three 74F244 octal 3-state buffers are used to drive the 24 bit system address bus (16 bits in some cases). Two 74F245 octal bidirectional 3-state buffers are used to drive the 16 bit data bus (8 bits in some cases). In addition, half a 74F244 is used to drive the system command bus, composed of the signals $\overline{IORD}$, $\overline{IOWR}$, $\overline{MEMRD}$, and $\overline{MEMWR}$.

Multiple local processors may request use of the shared bus by setting $\overline{BUS\ REQUEST}$ active and waiting for the arbitration logic to assert $\overline{BUS\ GRANT}$. The arbitration logic indicates to the local processor when it may access the shared bus after a request has been made. This is necessary to prevent more than one local processor from accessing the system bus at the same time, resulting in bus contention and possible system failure.

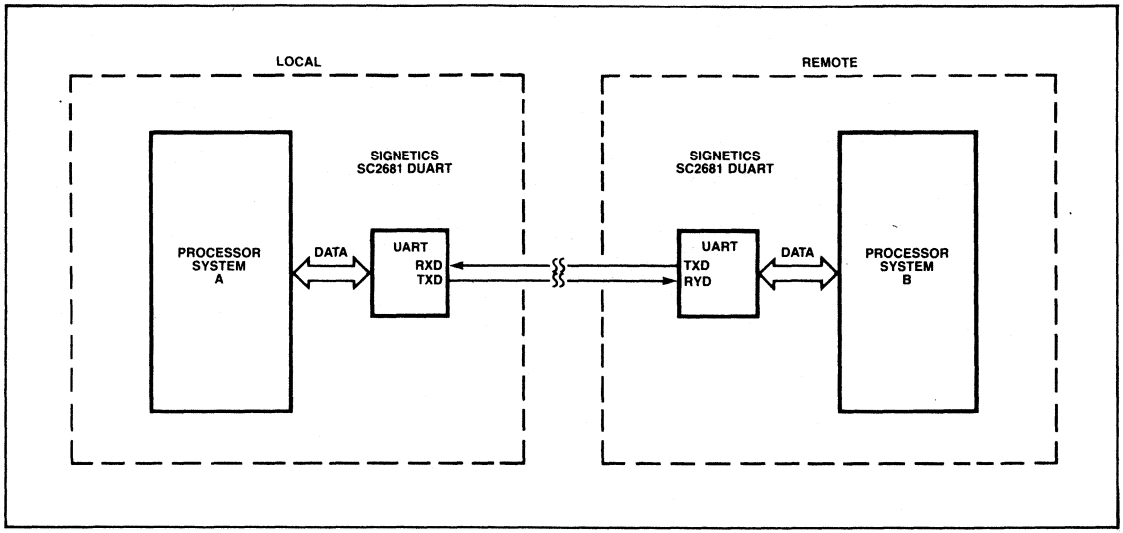


Figure 5. Serial Communications Link Provides Economical Inter-processor Communications

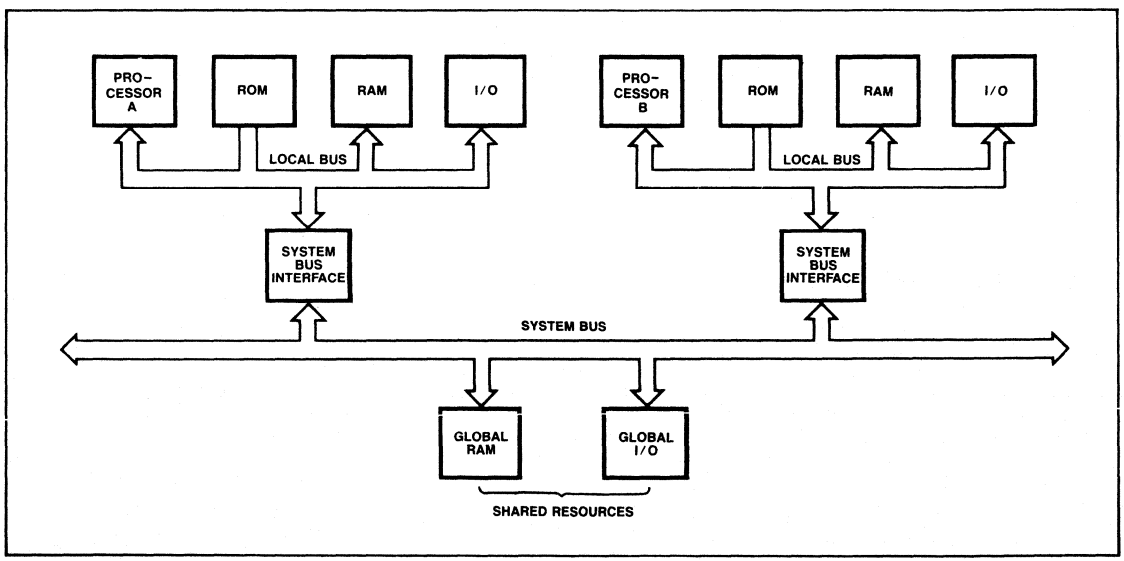


Figure 6. Shared Bus Provides Most Powerful Multiple Processor Architecture

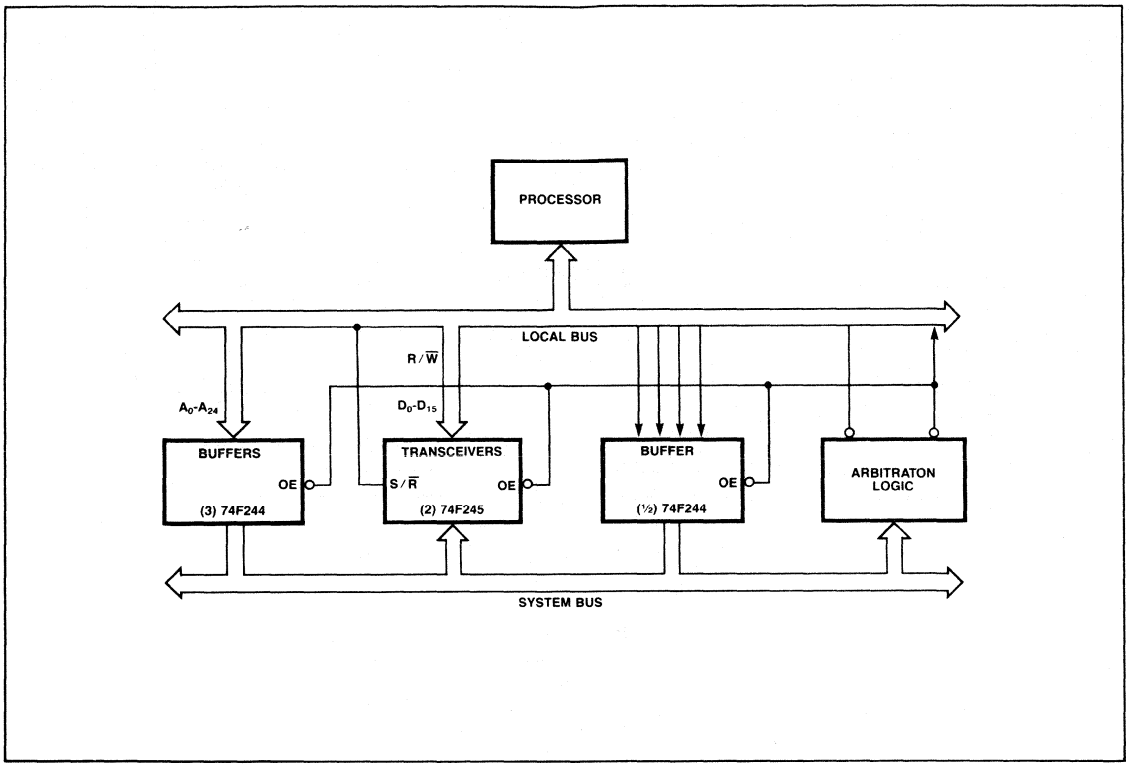


Figure 7. Typical System Bus Interface

6

ARBITRATION

Contention by several processors for use of shared resources can create sticky timing problems unless care is exercised in the design of appropriate arbitration logic to resolve timing conflicts. Schemes for bus arbitration vary in speed, cost, and flexibility and involve parallel, serial, transparent, pseudo-transparent, polled, and flag operations.

Parallel Priority Resolution

Parallel priority resolution is most useful in systems with 4 or more masters, where its speed outweighs the disadvantage of the additional hardware. A scheme for system bus arbitration using parallel priority resolution is shown in Figure 8.

A master's priority is determined by using a 74F148 priority encoder. Each master's arbitration logic generates a $\overline{\text{REQ}}$ to the priority encoder. When there is contention, the master whose $\overline{\text{REQ}}$ is connected to the highest priority input will be granted access. A 74F138 is used to decode the encoder outputs to generate the $\overline{\text{EI}}$ (enable input) to the arbitration logic of the master which has been granted access. $\overline{\text{CLEAR}}$ is used to remove all masters from the bus during reset or when an error condition is present. $\overline{\text{ARB CLOCK}}$ is used to synchronize all bus arbitration inputs and outputs to prevent race conditions and to facilitate a standard interface design. $\overline{\text{BUSY}}$ is generated by the master currently accessing the bus to indicate that the bus is in use. Even after a master has been granted access by the priority resolution, it must still wait for the current master to vacate the bus, i.e., $\overline{\text{BUSY}}$ going inactive. The arbitration logic generates a $\overline{\text{BUS GRANT}}$ to a master when $\overline{\text{EI}}$ is asserted and $\overline{\text{BUSY}}$ is not.

Serial Priority Resolution

Serial priority resolution eliminates the need for encoder/decoder hardware at the expense of speed. In Figure 9 a master's priority is determined by its physical location in a daisy chain configuration. A master negates its $\overline{\text{EO}}$ (enable output) when its $\overline{\text{EI}}$ (enable input) is negated or when it wants to access the bus. This negates $\overline{\text{EO}}$ for all masters further down the line *to go inactive.* If a master requests the bus, and no higher priority master is requesting the bus, as indicated by $\overline{\text{EI}}$ being asserted, the master may access the bus when the current master is finished. The ARB clock rate is limited to the speed at which the daisy chain signals can propagate through all masters.

Arbitration Logic

Aribitration logic suitable for either parallel or serial priority resolution is shown in Figure 10. The logic shown synchronizes a master's $\overline{\text{BUS REQUEST}}$ input to $\overline{\text{ARB CLOCK}}$ using flip-flop 1, asserting $\overline{\text{REQ}}$ and negating $\overline{\text{EO}}$. If $\overline{\text{EI}}$ is asserted and $\overline{\text{BUSY}}$ is not, the master may access the bus on the next falling edge of $\overline{\text{ARB CLOCK}}$. This arbitration is provided by flip-flop 2. $\overline{\text{BUS GRANT}}$ and $\overline{\text{BUSY}}$ are asserted. When the access is complete, the master negates $\overline{\text{BUS REQUEST}}$ inactive. On the falling edge of $\overline{\text{ARB CLOCK}}$,

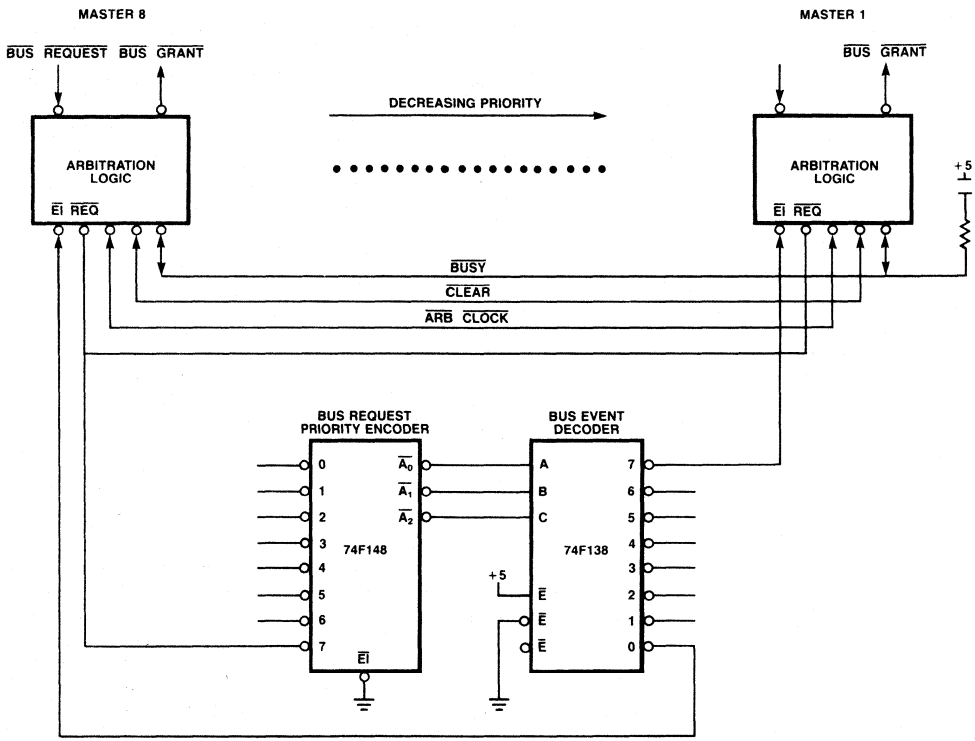


Figure 8. System Bus Arbitration Using Parallel Priority Resolution

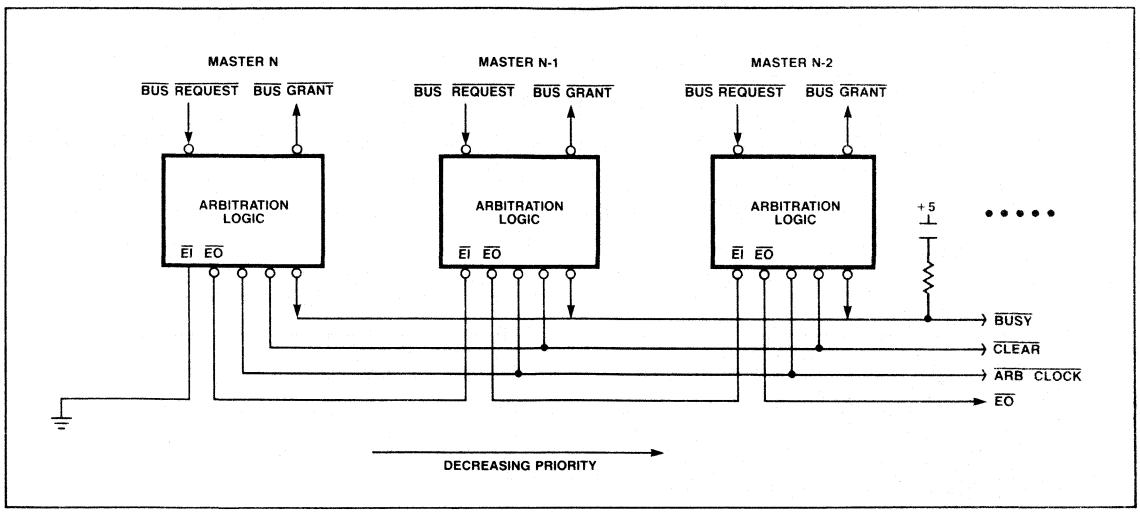


Figure 9. System Bus Arbitration Using Serial Priority Resolution

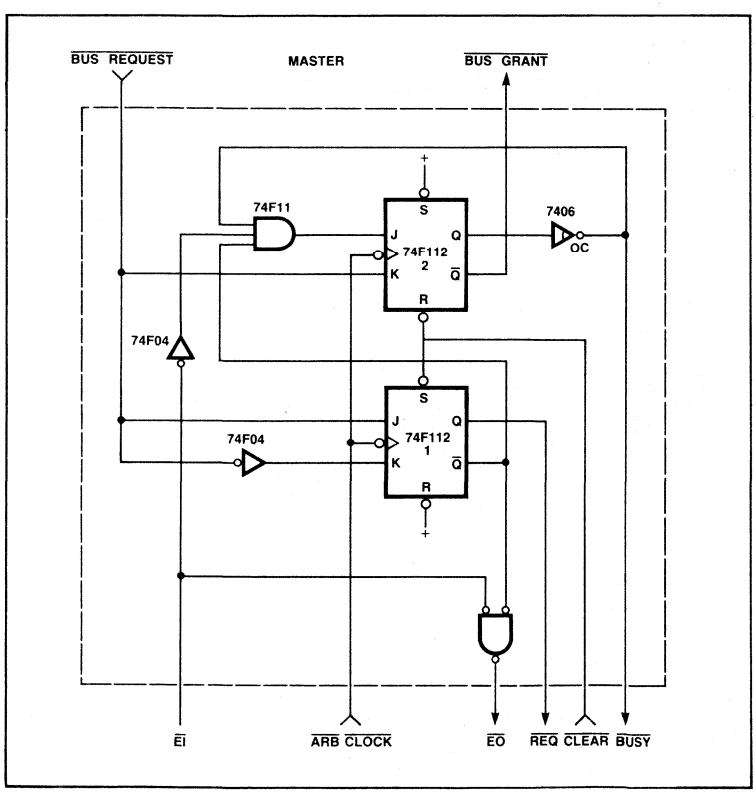


Figure 10. Arbitration Logic Supports Serial or Parallel Priority Resolution Techniques

REQ negated and, if EI is asserted EO is asserted. On the next falling edge BUSY and BUS GRANT are negated. The timing diagram for this sequence is shown in Figure 11. Note that a master must wait for the current master to complete a transfer and negate BUSY before it may access the bus.

Pseudo-Transparent Priority Resolution

The logic of Figure 12 uses "cycle stealing" to permit single byte transfers with pseudo-transparent arbitration. When the address decoder determines that a master requires access to shared bus, it asserts BUS REQUEST. The processor's READY line is held negated, "freezing" the processor until the arbitration logic asserts BUS GRANT. Then READY is asserted and the shared bus cycle occurs. The processor is unaware of arbitration and unaware that the bus is shared. With this technique, a watchdog timer should be used to ensure that the processor doesn't "hang up" if faulty bus operation prevents access. Access occurs one cycle at a time, preventing any one master from "hogging" the bus.

Polled Access to Shared Bus

The logic in Figure 13 uses an output port to request access to the bus, and polls an input port to determine when access has been granted. Once access is granted, the master retains the bus until it negates the BUS REQUEST output port bit. Large block moves may occur without fear of another master

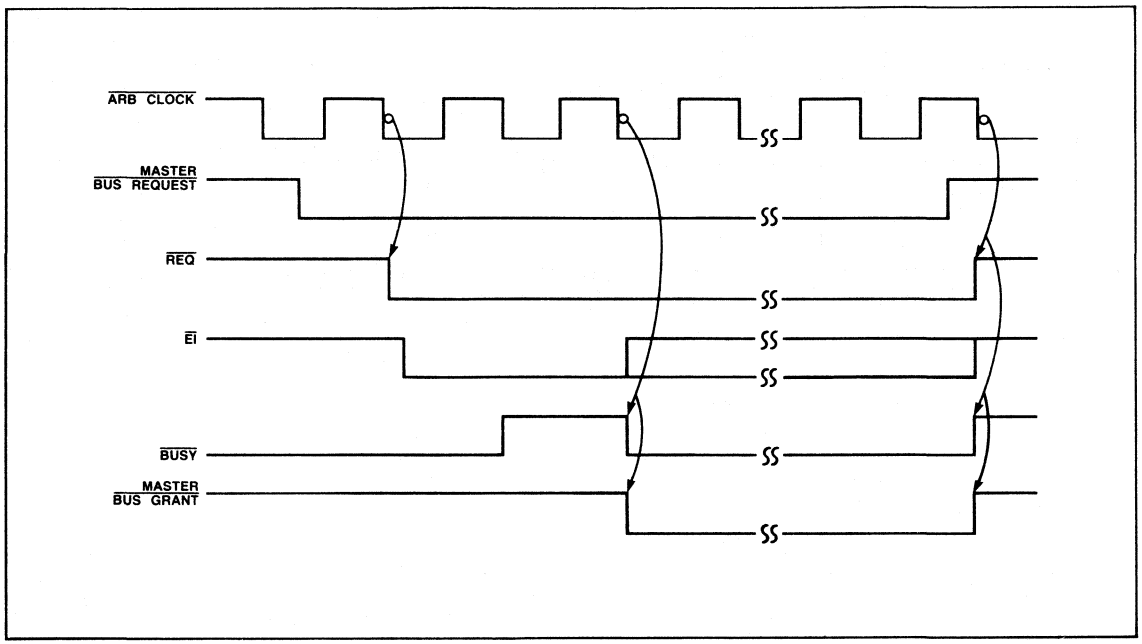


Figure 11. Timing Diagram for Arbitration Logic

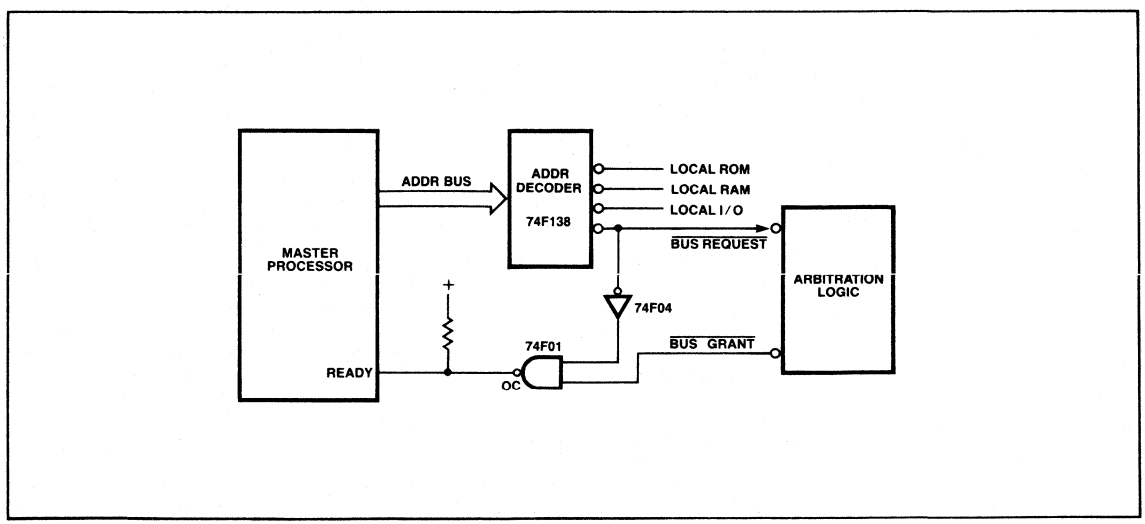


Figure 12. Pseudo-transparent Access to Shared Bus

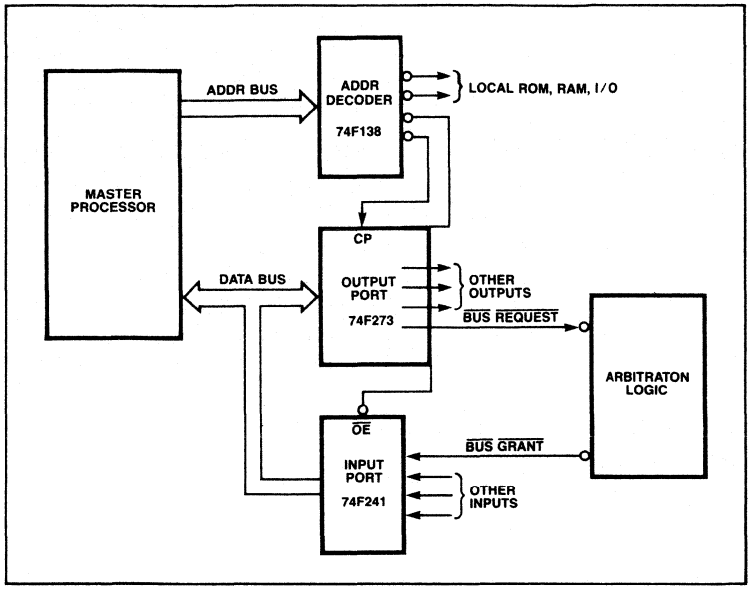


Figure 13. Polled Access to Shared Bus

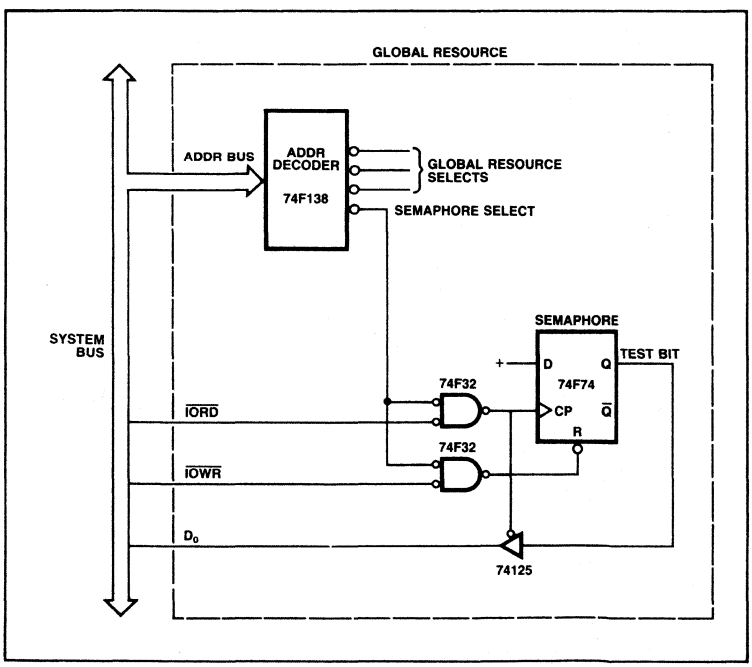


Figure 14. Semaphore (Flag) Register Permits Access to Shared Resource Without Monopolizing Shared Bus

changing the data as with cycle-by-cycle arbitration. However, this approach greatly slows down the response time of the system, because of the waiting while each master performs. All other masters must wait, even if they do not require the use of the same shared resource.

Semaphore (Flag) Arbitration

The logic of Figure 14 improves on the polled access technique by permitting access to a shared resource when that resource is available. A master first reads the semaphore register associated with the resource it wishes to access. The master may not access the resource unless the semaphore bit is false. When the semaphore bit is false, reading the register automatically sets the bit true. When the master reads a false semaphore, it may then access the resource. All other masters reading the semaphore will see it set and will not access the resource. The master may access the resource until it is no longer needed. By writing to the semaphore register, it is automatically reset, allowing other masters to access the resource. Only the one resource, not the entire shared bus, is monopolized by one master at a time. The hardware performs a function similar to a software read-modify-write operation.

The timing for the semaphore operation is shown in Figure 15. If the semaphore bit is false and the register is read, the bit is set true at the end of the read cycle (rising edge of $\overline{IORD}$). The semaphore bit is reset by doing a "dummy" write to the semaphore register. The bit is set false at the beginning of the cycle ($\overline{IOWR}$ going low).

INTERFACING THE MC68000 TO THE MULTIBUS™*

One of the best examples of a multi-processor shared bus is the MULTIBUS. One of the most popular 16 bit processors in new designs today is the MC68000. Yet, to our knowledge, there are currently (mid-83) no LSI MULTIBUS arbiter ICs available to allow a designer to easily interface the two. There are arbiter ICs available, but they were designed for other processors and are cumbersome and limited in performance when interfaced to the 68000.

The following is the design for a 68000 MULTIBUS interface. The design supports serial or parallel arbitration and performs with a 10 MHz bus clock. Operation is similar

*MULTIBUS™ is a trademark of Intel Corporation.

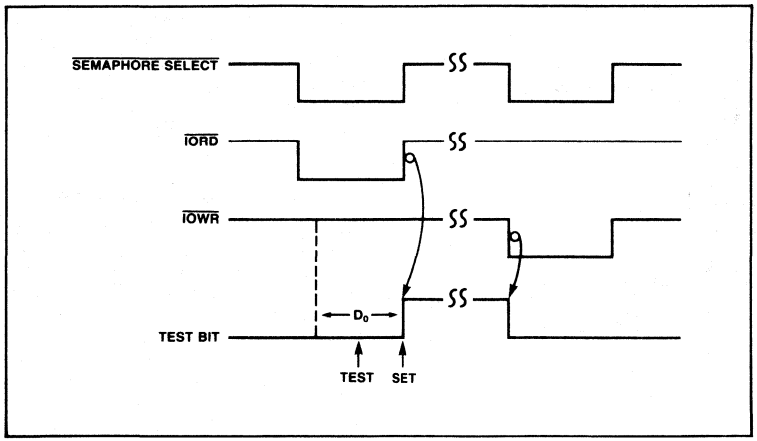


Figure 15. Timing Diagram for Semaphore Operation

to the example described previously. Tables 1 and 2 define the MC68000 bus control signals and the MULTIBUS arbitration signals. The timing diagram for MC68000 read and write cycles is shown in Figure 16.

Figure 17 shows the control circuitry for the MC68000 to MULTIBUS interface. The master initiates a MULTIBUS transfer by asserting $\overline{\text{MULTIREQ}}$ active. This is usually the output of address decode circuitry. $\overline{\text{AS}}$ clears the request at the end of the transfer. Flip-flops 1, 2, and 3 sample and synchronize the bus request to the falling edge of $\overline{\text{BCLK}}$. Since $\overline{\text{MULTIREQ}}$ is asynchronous to $\overline{\text{BCLK}}$, flip-flop 2 serves as a synchronizer and is clocked on the rising edge of $\overline{\text{BCLK}}$. All inputs to the arbiter are thus synchronous so that race conditions at flip-flop inputs are avoided.

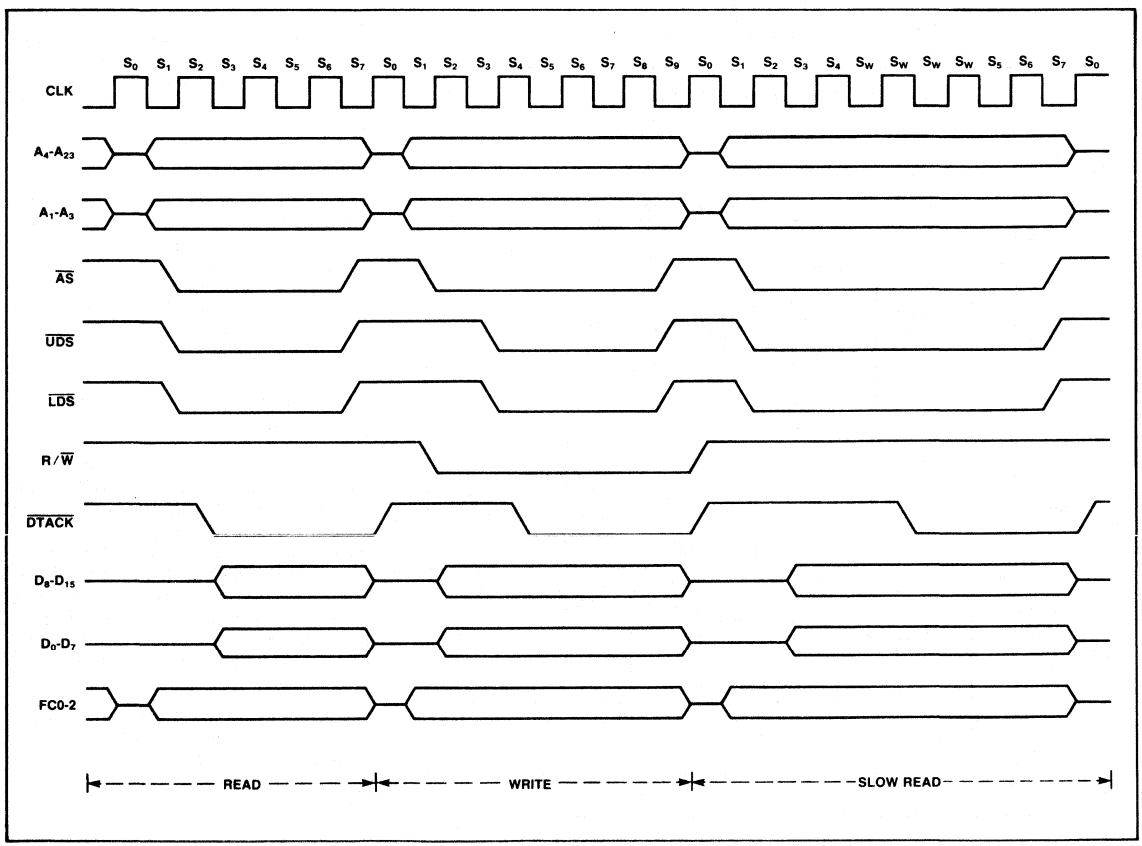


Figure 16. MC68000 Read and Write Cycle Timing Diagram

Table 1. MC68000 BUS CONTROL SIGNALS. (REFER TO THE SIGNETICS 68000 MICROPROCESSOR DATA SHEET FOR MORE INFORMATION.)

CLK	Clock. Time reference for 68000 microprocessor bus control.
$\overline{AS}$	Address Strobe. Indicates that address on address bus is valid.
$\overline{UDS}$, $\overline{LDS}$	Upper and Lower Data Strobe. Indicates that the processor is reading from or writing to the upper data byte (D_7–D_{15}) and/or the lower data byte (D_0–D_7).
R/$\overline{W}$	Read/Write. Indicates whether the current bus cycle is a read or a write cycle.
$\overline{DTAK}$	Data Transfer Acknowledge. Input to the 68000 indicating that the data transfer can be completed, on the high to low transition.

If the bus is not in use ($\overline{BUSY}$ is not asserted), and no higher priority master requests the bus ($\overline{BRPN}$ is asserted), the master is granted access on the next falling edge of $\overline{BCLK}$. Flip-flop 4 provides this function. If these conditions are not satisfied, $\overline{DTACK}$ is used to force the CPU to wait. Once the master is granted access, it sets $\overline{BUSY}$ active to indicate that the bus is in use. $\overline{BUSEN}$ (bus enable) also becomes active and gates the master's address, data, and control buses onto the MULTIBUS. One half cycle later, on the rising edge of $\overline{BCLK}$, flip-flop 5 sets CMDEN (Command Enable) active. This allows RD or WR strobes to be asserted on the MULTIBUS. This delay is necessary because the MULTIBUS requires data and address valid 50 ns before read or write commands. DS is used to generate the read or write strobes.

The MULTIBUS transfer is completed when $\overline{XACK}$ is asserted terminating the 68000 cycle by asserting $\overline{DTACK}$. The master

Table 1. MC68000 BUS CONTROL SIGNALS. (REFER TO THE SIGNETICS 68000 MICROPROCESSOR DATA SHEET FOR MORE INFORMATION.)

$\overline{BCLK}$	Bus Clock. All arbitration signals listed below must be synchronized to the negative edge of this clock. It is independent of any processor clock.
$\overline{BPRN}$	Bus Priority In. Indicates that no higher priority master is requesting the bus. Similar to $\overline{EI}$ in previous examples.
$\overline{BPRO}$	Bus Priority Out. Used in serial priority resolution circuits. Similar to $\overline{EO}$ in previous examples.
$\overline{BUSY}$	Bus Busy. Driven by current bus master to indicate that the bus is in use.
$\overline{BREQ}$	Bus Request. Used in parallel priority resolution circuits. Similar to $\overline{REQ}$ in previous examples.
$\overline{CBRQ}$	Common Bus Request. Driven by all potential bus masters requesting bus. Used to save time by allowing the present bus master to avoid arbitration after each cycle if no other requests are active.
$\overline{XACK}$	Transfer Acknowledge. Indicates that the MULTIBUS data transfer is completed on high to low transition.

maintains control of the MULTIBUS until another master requests access, as indicated by asserted $\overline{CBRQ}$. If the current master is not performing a MULTIBUS transfer, it loses the bus on the next falling edge of $\overline{BCLK}$. CMDEN, $\overline{BUSEN}$, and $\overline{BUSY}$ are negated. Flip-flop 4 provides this function.

The logic that interfaces the MC68000 to the MULTIBUS is shown in Figure 18. 74F533 inverting octal 3-state latches are used to gate the 20 bit address and 16 bits of data onto the MULTIBUS. Note that the data and address bus is negative true. 74F240 octal 3-state inverting buffers are used to gate 16 bits of data onto and off of the MULTIBUS. Data direction is determined by the MC68000's R/W line. A 74F139, 2 to 4 decoder is used to decode I/O and RD/WR to generate the 4 MULTIBUS commands. I/O is the output of address decode circuitry which decodes I/O addresses. A 74F244 is used to gate the commands onto the MULTIBUS.

Signetics FAST logic family is used in this design to increase speed and bus drive capability while minimizing MULTIBUS loading.

REDUNDANT MICROPROCESSORS ENHANCE RELIABILITY

Figure 19 shows how two 6809E microprocessors are used in a parallel redundancy scheme to prevent faulty operation from damaging external systems. Two systems with identical processors, RAM, ROM, and I/O are first synchronized. After synchronization, their data buses are compared every cycle. If the data on the two buses is different, an error has occurred and the system shuts down.

A common clock is used to drive the 6809E processor in each system so that a timing reference is established. Upon reset, both processors execute a sync instruction and the critical output circuits are turned off. When both processors have executed the sync instruction, as indicated by BA=0 and BS=1, the START button is used to interrupt the processors and they begin program execution in synchronism. The critical outputs are also turned on. On the falling edge of E, the data buses of the two systems are compared using the 74F521 octal comparator. If the data does not match, at least one system is operating incorrectly. The 74F74 flip-flop latches the error condition and turns off the critical outputs.

A similar technique should be used on outputs to ensure that an output goes active only when the output of both systems goes active.

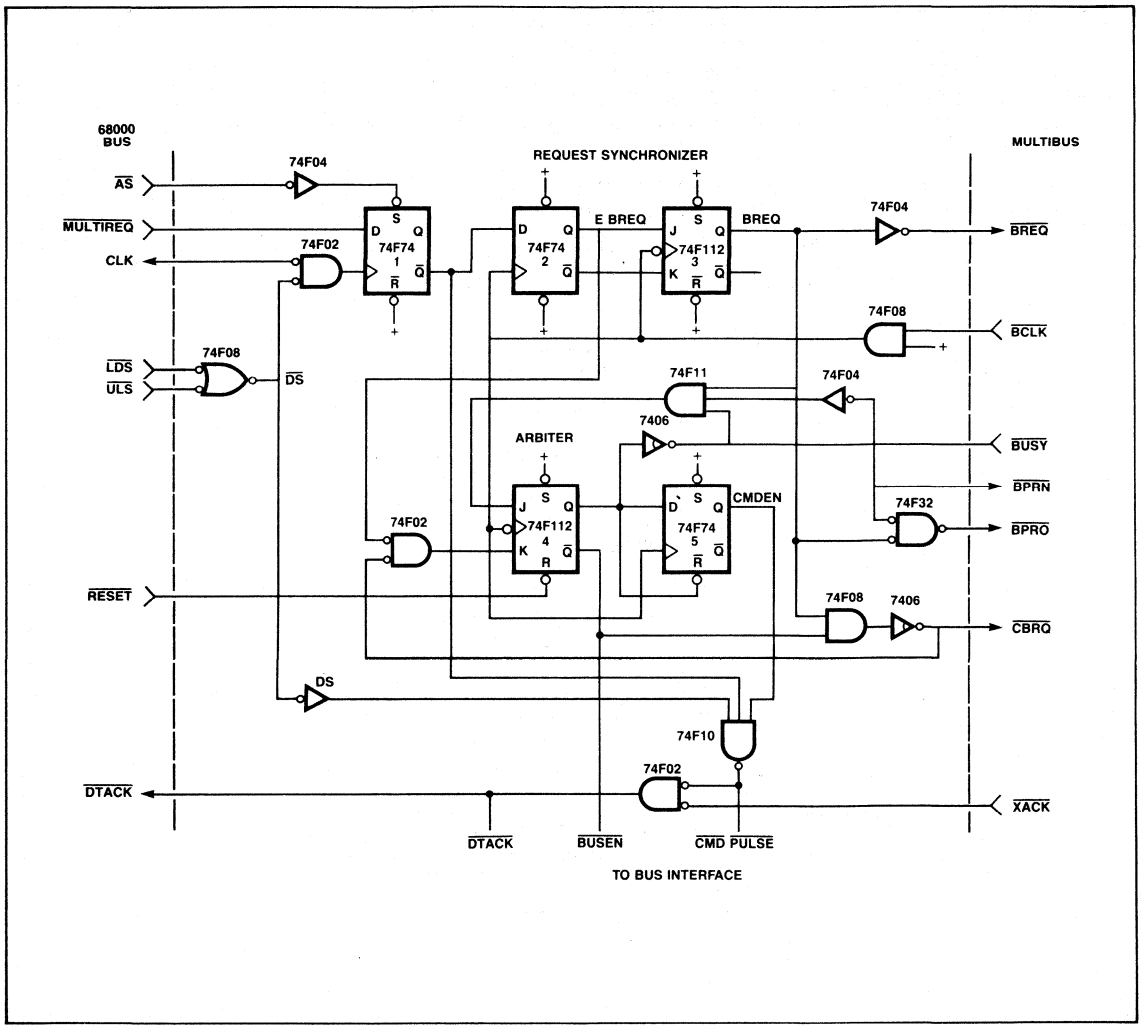


Figure 17. MC68000 MULTIBUS Interface Control Circuitry

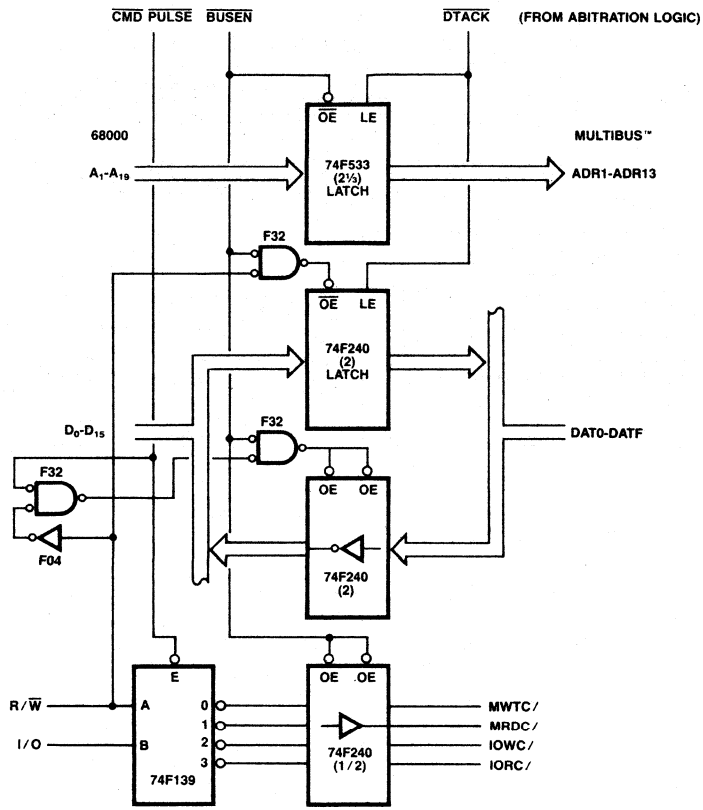


Figure 18. MC68000 to MULTIBUS Interface Logic

6

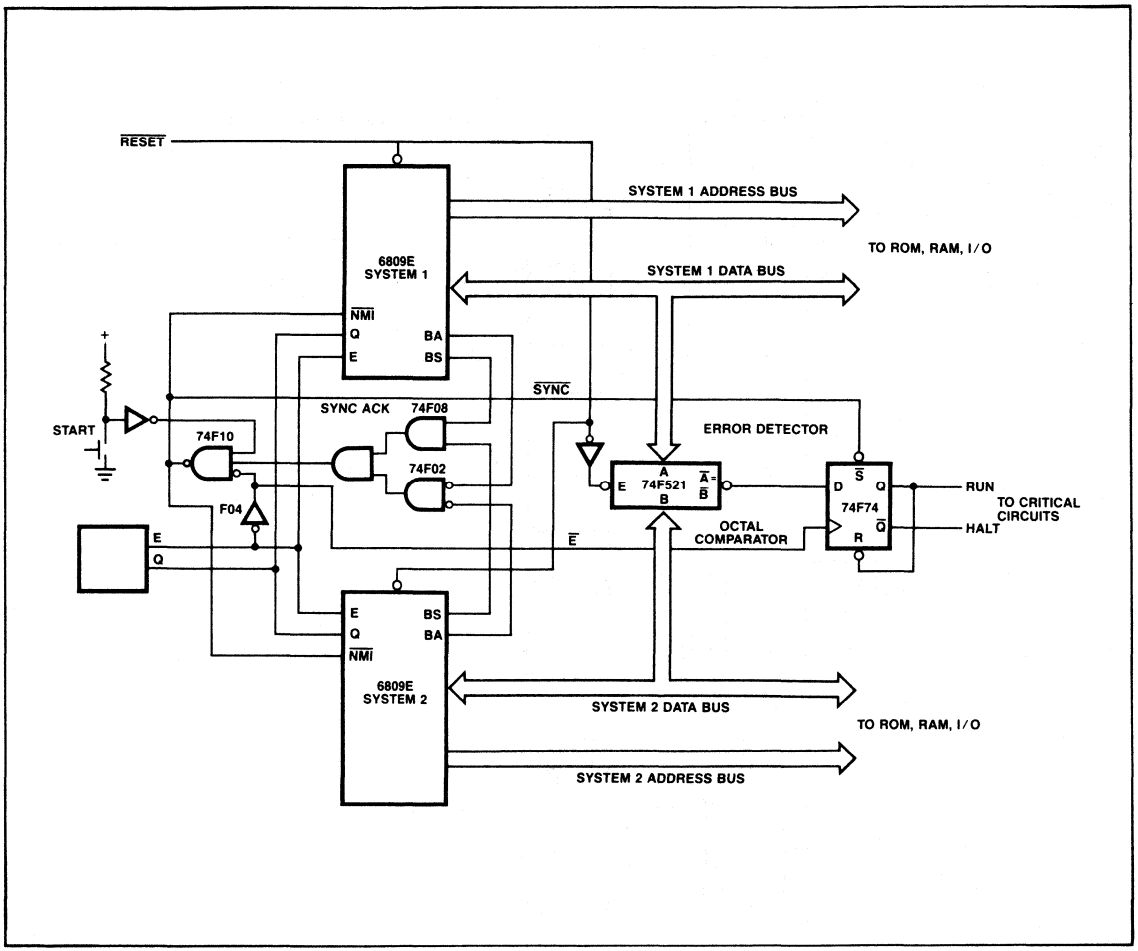


Figure 19. Redundant 6809E Microprocessors Prevent I/O Damage

BIBLIOGRAPHY

Many of the applications illustrated in this note were contributed or influenced by entries in Signetics' Interface Circuit design contest. Special thanks are due to the individuals whose entries were referenced in whole or in part in this note.

INTERRUPT CONTROL LOGIC USING FAST ICs

App Note 208

INTRODUCTION

This application note shows how Signetics FAST circuits can be used to implement interrupt control logic for a variety of microprocessors. The circuits presented serve a variety of functions, which include:

- Masking: How to selectively enable interrupt inputs
- Prioritizing: Which interrupt is serviced when more than one interrupt occurs.
- Vector Generation: How the interrupt service routine is selected

An interrupt is an asynchronous input to a microprocessor that suspends current program execution and causes a jump to an interrupt service routine. Interrupts are especially useful in real-time systems and have become a standard feature in microprocessor designs.

REASONS FOR USING INTERRUPTS

The use of interrupts generally increases the efficiency of the system. Without interrupts, the microprocessor must poll each peripheral to determine when it is ready for service. The time spent polling cuts down available processing time, and polling is unnecessary when the peripheral devices are not ready for service. With interrupts, the peripheral device informs the processor when it is ready; thus no time is wasted.

Interrupts also provide faster response to service requests from a peripheral. The high data rate of many devices, (e.g. disk drives) requires immediate response to prevent loss of data. As another example, a power-fail interrupt can be used to initiate an orderly shutdown in the remaining moments.

Interrupts can also be used for error handling. If a parity error is detected in the memory, for example, an interrupt can be generated to suspend the operation of the program or invoke an error-handling routine.

INTERRUPT LATCHING

Figure 1 shows a circuit that captures asynchronous events and generates an interrupt to the microprocessor. The 74F533 inverting octal latch is used to "freeze" the state of the interrupt inputs. This is necessary to catch short interrupt request pulses.

When all interrupt requests are inactive, the latch enable (LE) input of the 74F533 is asserted. When any request is asserted, the interrupt signal to the microprocessor ($\overline{INT}$) is asserted and the latch is disabled. Thus, the state of the interrupt inputs is latched.

During its interrupt service routine, the microprocessor reads the interrupt latch outputs via the 74F244 octal 3-state buffer to determine which event caused the interrupt. This scheme is most useful with microprocessors such as the 6800 family that do not have vectored interrupts.

At the end of the interrupt service routine, the microprocessor resets the latch by pulsing the /CLEARINT output line. This would typically be generated by decoding a write to a particular address.

INTERRUPT MASKING

Figure 2 shows an interrupt controller that allows each interrupt input to be individually enabled or disabled (masked). A 74F273 octal D flip-flop stores the state of the interrupt inputs whenever any input changes.

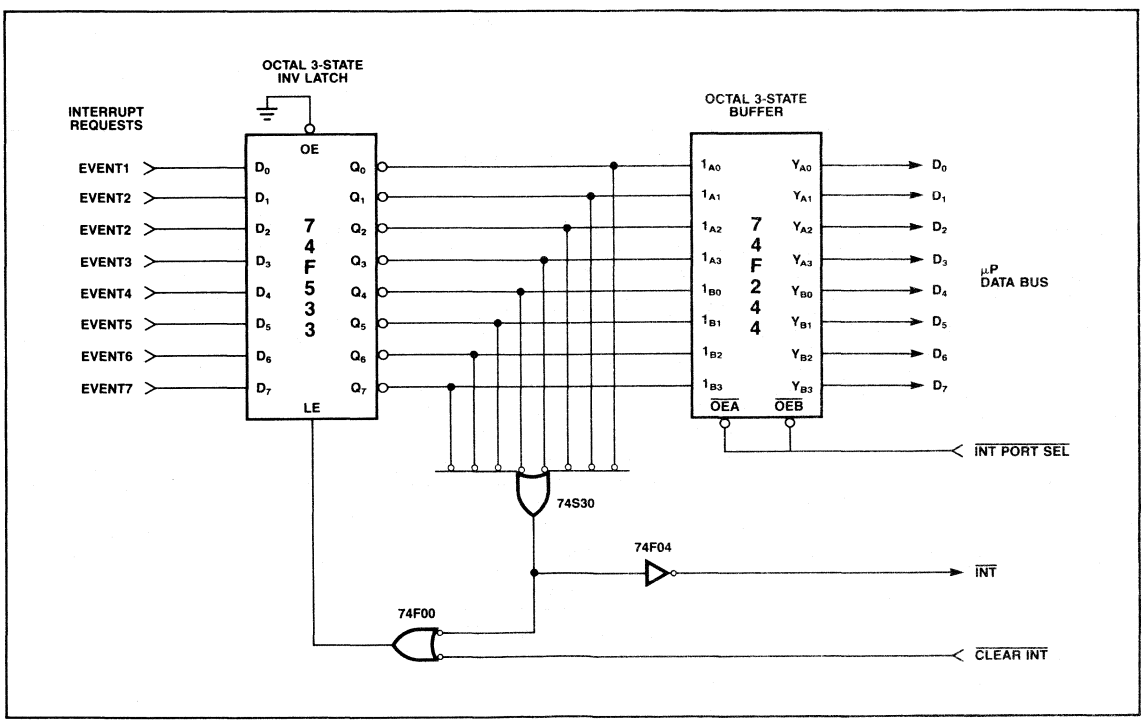


Figure 1. Interrupt Latching

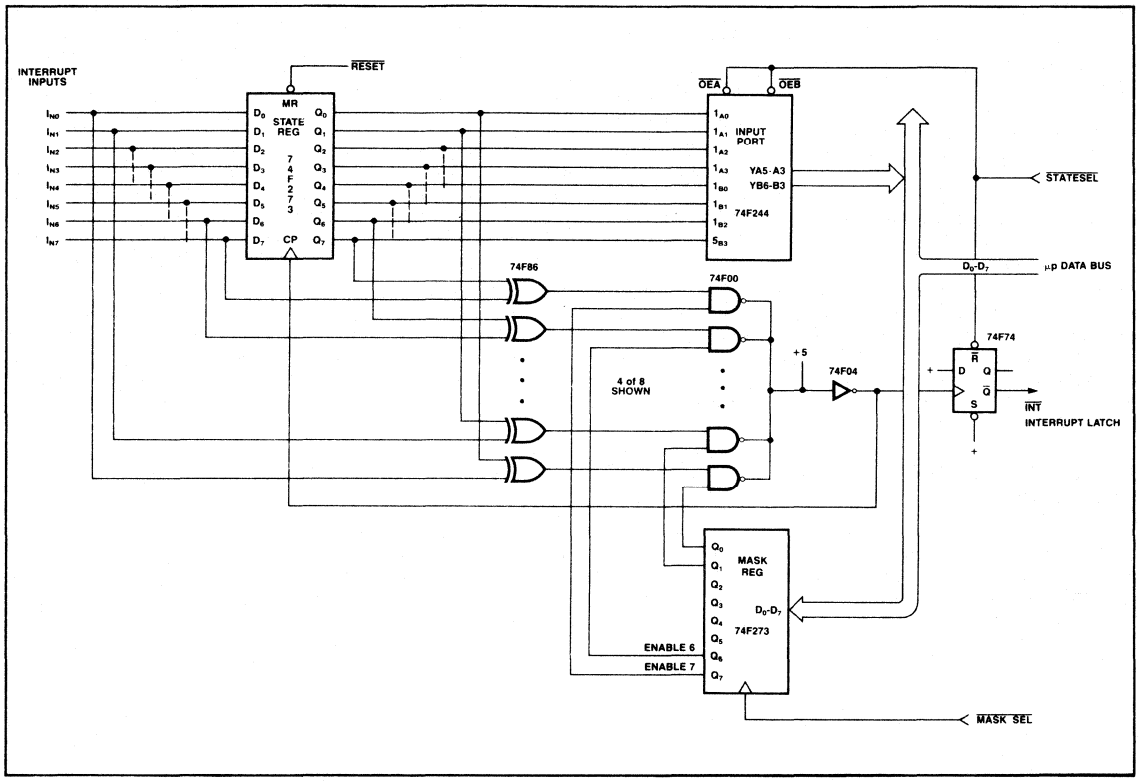


Figure 2. Interrupt Masking

Exclusive-OR gates 74F86 compare the inputs of the state register to its outputs; whenever an input changes, the corresponding exclusive-OR gate output goes high.

Another 74F273, connected as an output port, serves as the mask register. The microprocessor writes a bit pattern to this port to determine which interrupts are enabled. The outputs of the exclusive-OR gates are then ANDed with the mask register outputs, so that interrupt inputs with a zero in their mask bit are ignored.

Whenever any unmasked input changes state, the state register is clocked, and the interrupt latch is set. The microprocessor reads the state register via the 74F244 3-state buffer acting as an input port, and the interrupt latch is cleared.

Caution: This circuit can be fooled if an interrupt input changes twice before the microprocessor reads the state register. Therefore, this design should be used only for relatively slow-changing interrupt inputs.

INTERRUPT PRIORITIZING

In the previous circuits, the hardware does not select which interrupt has highest priority. If two or more interrupts are simultaneously asserted, the microprocessor software must decide which to process first.

Figure 3 shows a circuit with prioritization logic to select the highest priority interrupt. Interrupt inputs are sampled by the 74F377 octal flip-flop. This register is also used to freeze the state of the interrupt inputs when the output of the priority encoder is being read by the microprocessor. If one (or more) interrupt input is asserted, the output of the 74F148 priority encoder will indicate the number of the highest priority active interrupt.

The $\overline{GS}$ output of the encoder is effectively the OR of all the inputs, and produces the interrupt signal to the microprocessor. The microprocessor then reads the interrupt number via the 74F244 3-state buffer connected as an input port. The microprocessor can use the interrupt number as an index pointer into a branch table, to access the appropriate service routine.

A 74F138 3-to-8 decoder decodes the interrupt number to generate individual reset signals for each interrupt source. The decoder is enabled when the microprocessor reads the interrupt number, so the interrupt output of the device being serviced is automatically reset.

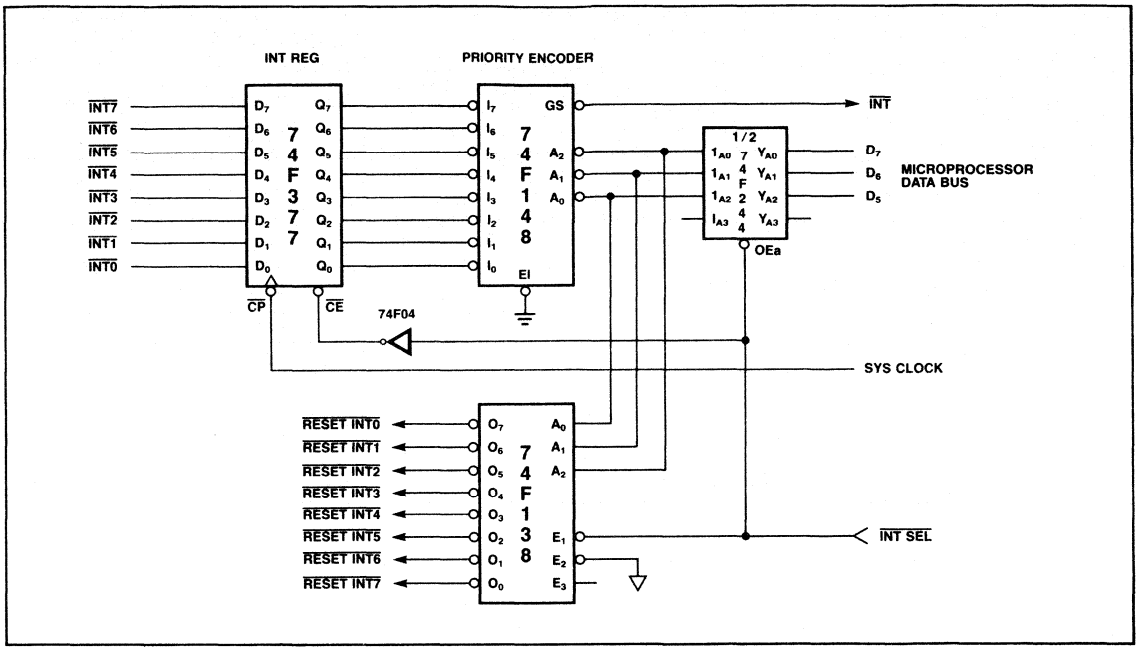


Figure 3. Interrupt Prioritizing

RESTART VECTOR GENERATION FOR 8080-FAMILY PROCESSORS

The 8080, 8085, NSC800, and Z80 all have interrupt modes in which a vector is automatically read from the interrupting device. (For the 8080, this is the only mode; the other processors also have additional modes.) This vector is treated as an instruction; the single-byte CALL instructions called RESTARTs are generally used for the vectors. The format of the restart instructions is 11CBA111 (binary), where CBA represents the three-bit indentifier. Figure 4 illustrates a restart vector generation circuit.

The 74F148 priority encoder generates the interrupt request to the microprocessor when any interrupt input is asserted. It also provides the three-bit identifier to the appropriate inputs of the 74F244. When the microprocessor performs an interrupt acknowledge cycle, the restart instruction is read via the 74F244 octal buffer. Table 1 shows the vectors generated for each input. Interrupt input 7 produces an identification code of 000, since the priority encoder outputs are active low.

Note that the interrupt inputs are not latched by this circuit, and thus must remain asserted until the interrupt acknowledge cycle is completed.

Table 1. 8080-FAMILY INTERRUPT VECTOR GENERATION

HIGHEST PRIORITY ACTIVE INPUT	VECTOR GENERATED	INSTRUCTION NAME 8080	Z80
INT7	11000111	RST0	RST 0
INT6	11001111	RST1	RST 8
INT5	11010111	RST2	RST 16
INT4	11011111	RST3	RST 24
INT3	11100111	RST4	RST 32
INT2	11101111	RST5	RST 40
INT1	11110111	RST6	RST 48
INT0	11111111	RST7	RST 56

The Z80 microprocessor has several modes of interrupt operation. The mode described above is called mode 1. Mode 2 is a table-driven mode in which the vector supplied by the peripheral is used as a pointer to a table. The service routine address is then read from the table.

Figure 5 shows a circuit for generating the vectors for Z80 mode 2 interrupts. The 74F148 priority encoder generates a three-bit binary number corresponding to the highest priority active interrupt. This number is read by the microprocessor during the interrupt acknowledge cycle via the 74F244 octal 3-state driver.

Table 2 shows the vectors generated by the circuit. The least significant data input of the 74F244 is grounded, and the code from the priority encoder provides the next three bits. This is necessary because each interrupt vector must point to a two-byte entry in the service routine address table. The four most significant bits are set by the switches. This allows the same circuit to be used in several places in a system by setting the switches differently on each.

Table 2. INTERRUPT VECTORS GENERATED BY CIRCUIT IN FIGURE 5.

HIGHEST-PRIORITY ACTIVE INPUT	VECTOR GENERATED (HEX)
INT7	X 0
INT6	X 2
INT5	X 4
INT4	X 6
INT3	X 8
INT2	X A
INT1	X C
INT0	X E

NOTE:
1. X = switch settings

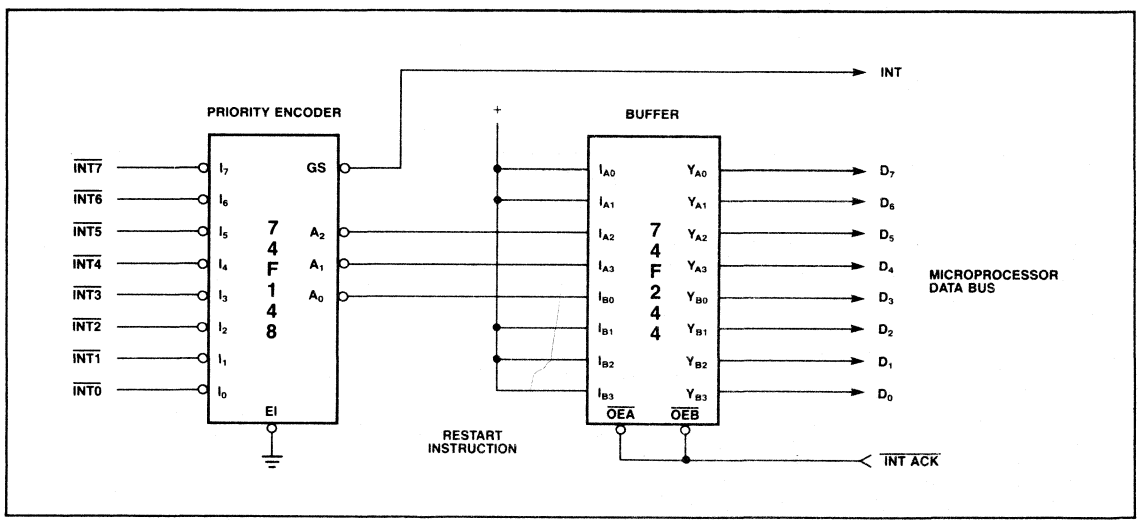


Figure 4. Restart Vector Generation Circuit

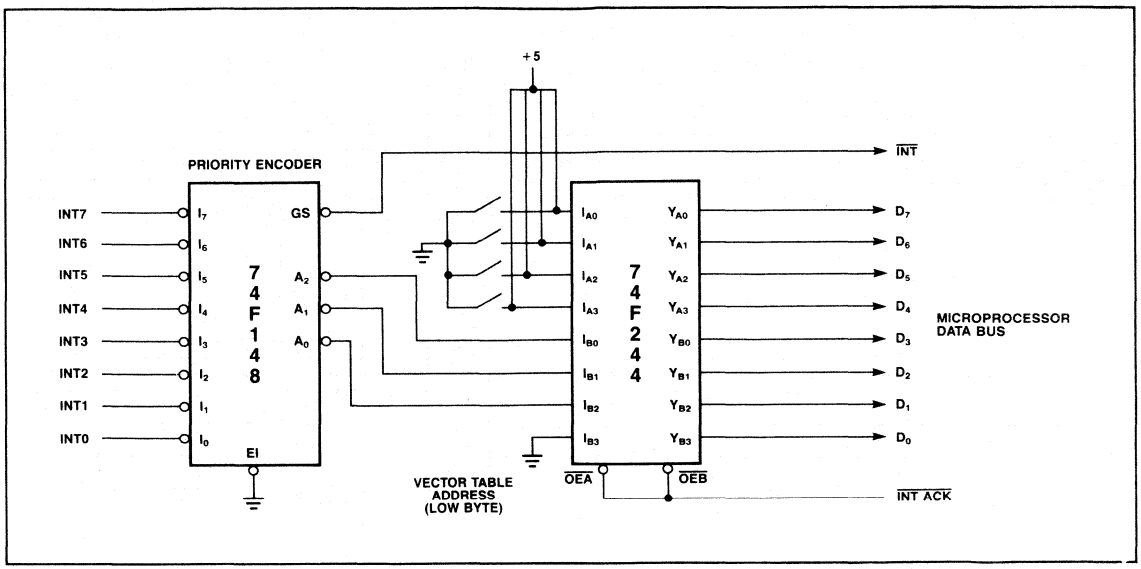


Figure 5. Vector Generation for Two Interrupt Modes

VECTORED INTERRUPTS FOR 6800-FAMILY MICROPROCESSORS

The 6800 microprocessor and its derivatives (6802 and 6502) do not have a built-in mechanism for handling vectored interrupts. When an interrupt occurs, the microprocessor fetches the address of the service routine from memory locations FFF8 and FFF9 (for the 6502, locations FFFE and FFFF). Normally these are ROM locations, and the interrupt service routine address is therefore fixed.

Figure 6 shows a circuit that provides vectored, prioritized interrupts for these microprocessors. When the microprocessor reads from address FFF8 or FFF9, this circuit disables the normal address buffers and substitutes a different address via a second set of 74F244 octal 3-state drivers. Bits 1, 2 and 3 of the substituted address are determined by the highest priority active interrupt input. Thus, the service routine address is fetched from a different memory location for each interrupt input. The high-order address bits are set by the switches.

DAISY CHAIN INTERRUPT PRIORITY SYSTEM

In the previous examples, a priority encoder was used to set the priority of each interrupt source. Another way to set priority is with an interrupt priority daisy chain, as shown in Figure 7. The priority of each device is determined by its physical location in the chain. Support for an interrupt daisy chain is built into the peripheral chips for some microprocessor families, such as the Z80. This example shows how a similar daisy chain can be implemented for other microprocessors, such as the 8085 or 68000.

When one or more device asserts an interrupt, the microprocessor responds by asserting $\overline{\text{INTACK}}$ active. This signal connects directly to the highest priority device's $\overline{\text{INTACK IN}}$ input. If that device had not asserted an interrupt, then it passes the interrupt acknowledge signal to the next device via its $\overline{\text{INTACK OUT}}$ signal. Thus, the interrupt acknowledge is passed along from one device to the next until it reaches the highest priority device that generated an interrupt. That device then places its interrupt vector on the data bus.

Figure 8 shows an implementation of this system. The two 74F74 flip-flops latch the interrupt request and synchronize it with the system clock. The signal at $\overline{\text{INTACK IN}}$ is passed to $\overline{\text{INTACK OUT}}$ unless the interrupt latch is set. The 74F244 drives the interrupt vector (restart instruction) to the data bus when $\overline{\text{INTACK IN}}$ is active and the interrupt latch is set. Switches allow the interrupt instruction to be selected for each device.

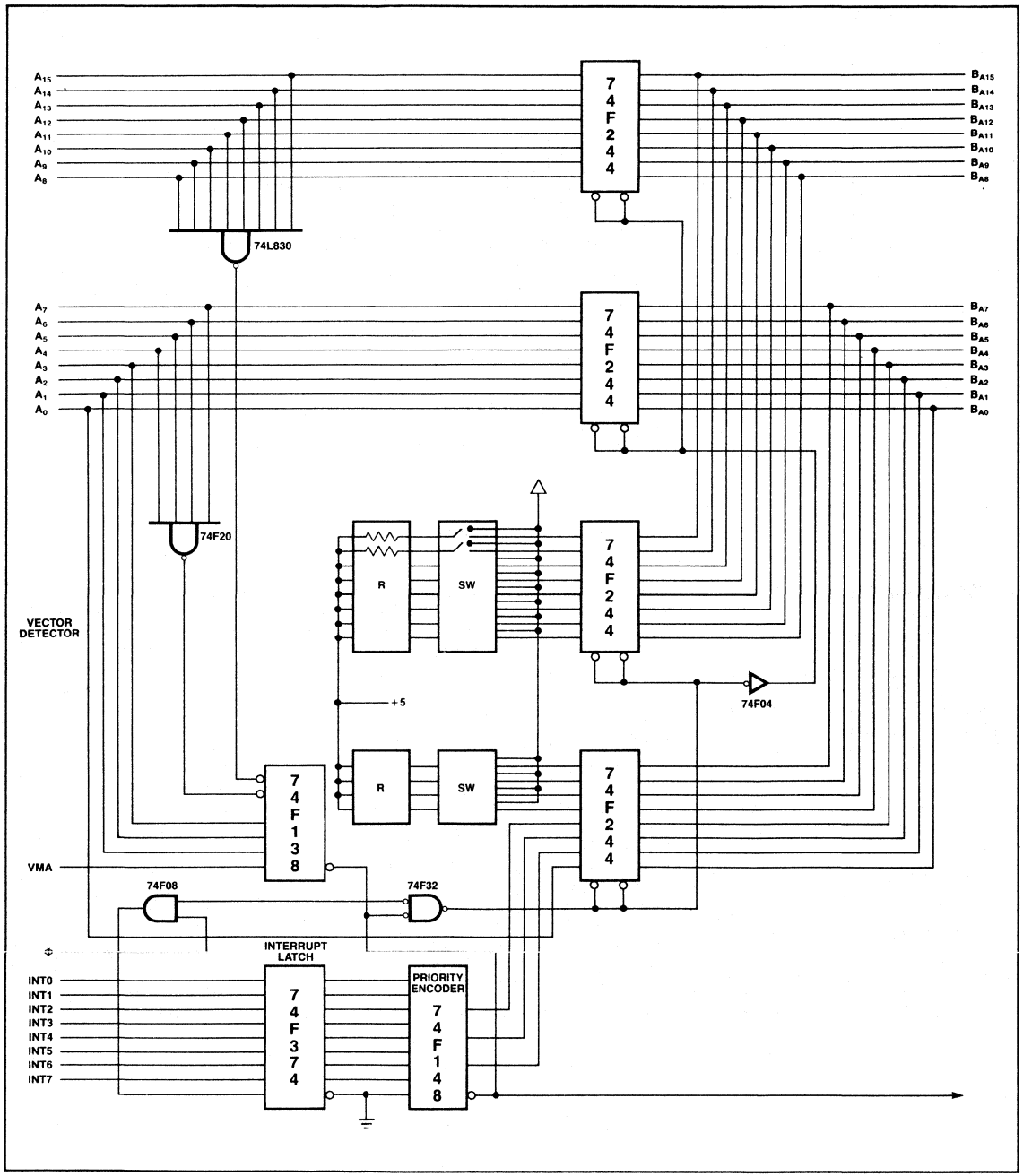


Figure 6. Prioritized Interrupt Vector Generator

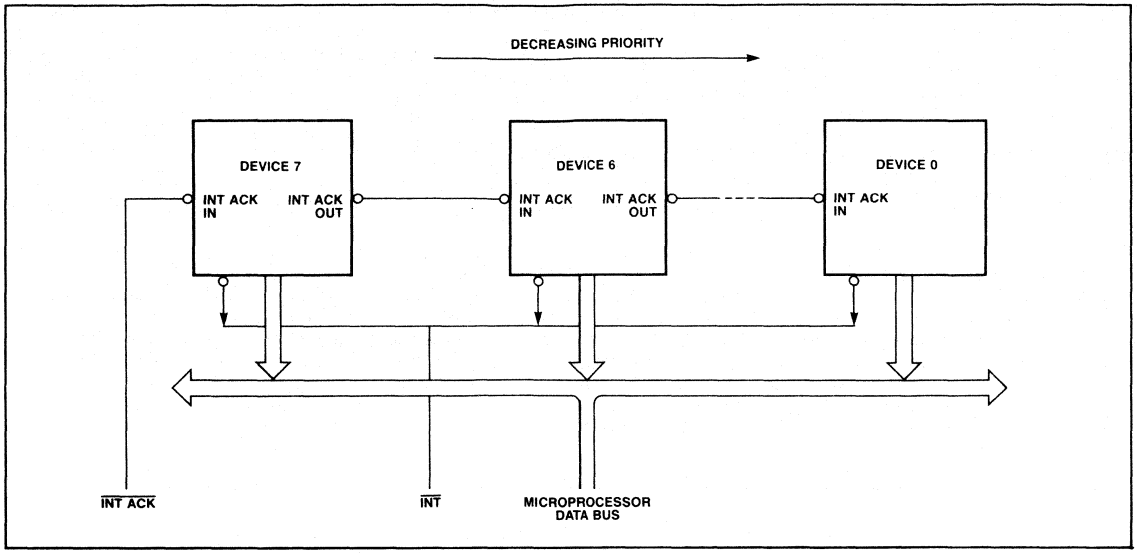


Figure 7. Daisy Chain Interrupt

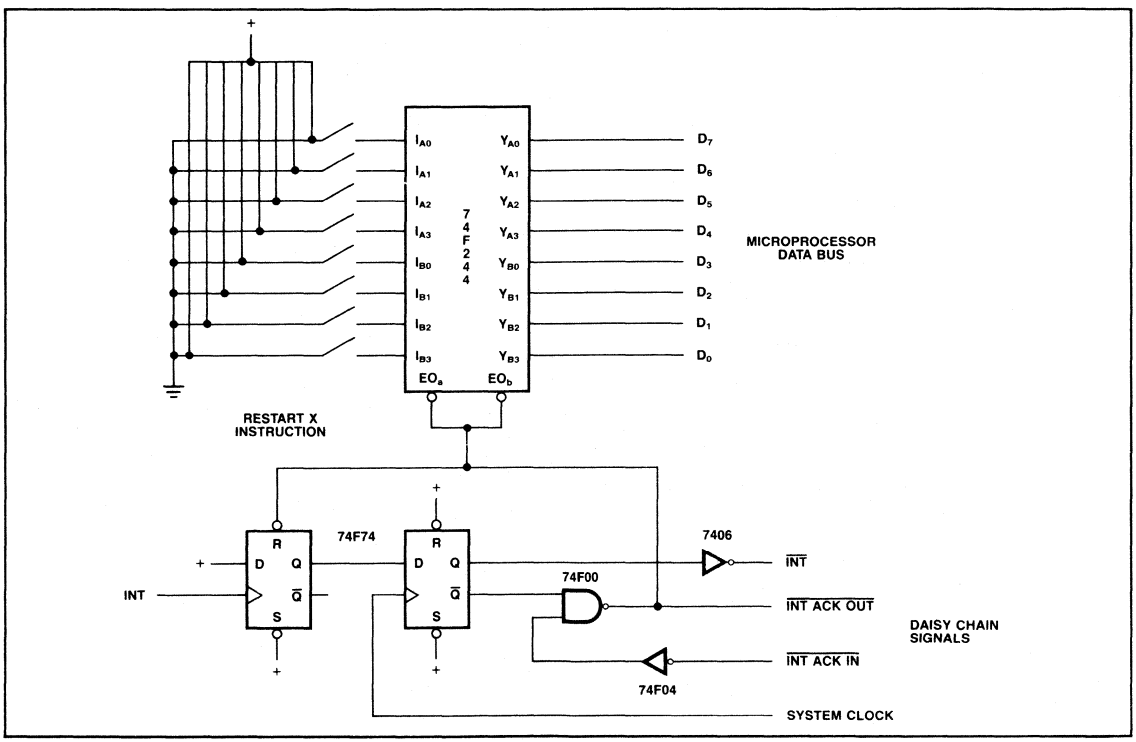


Figure 8. Logic Circuit for Implementation of Daisy Chain Interrupt

68000 INTERRUPT STRUCTURE

The 68000 16-bit microprocessor provides an extremely versatile interrupt structure. There are seven interrupt priority levels with up to 256 different vectors per level. The 68000 has a three-bit interrupt input which specifies the interrupt level. A code of 000 means no interrupt; any other code produces an interrupt, and the level corresponds to the code.

Figure 9 shows the timing diagram for the interrupt acknowledge cycle. When the 68000 recognizes the interrupt, it places the interrupt acknowledge code on the function code outputs /FC_0–/FC_2, and outputs the interrupt level being serviced on address lines A_0, A_1 and A_2. The interrupting device then places the interrupt vector on the data bus from which it is read by the 68000.

Figure 10 shows a circuit that allows the user, under program control, to generate an interrupt of any priority level and to supply any interrupt vector. The program uses a MOVE instruction to output the desired interrupt level and vector. The circuit then generates the interrupt. This allows subroutines to be implemented as interrupt service routines. It is also useful for testing interrupt service routines.

All signals are VERSABUS™ signals, with the exception of INT ADDR* which is the output of the address decoder, and RD/$\overline{WR}$* which must be derived from the VERSABUS™ control signals. Note that the address and data buses are active low; VERSABUS™ notation is used (active low signal names are followed by an asterisk "*"). DS0* and DS1* are basically the same as the 68000's $\overline{UDS}$ and $\overline{LDS}$. IACKIN* and IACKOUT* are priority daisy chain signals as described previously. IPL1* through IPL7* are the seven interrupt signals which are fed through a priority encoder on the CPU board (not shown) to generate the binary-encoded interrupt signals to the 68000.

The operation of the circuit is as follows:

- The software performs a move instruction to the address decoded as INTADDR*, with the interrupt vector in D_0–D_7 and the interrupt level in D_8, D_9 and D_A.
- Flip-flop I is set, releasing the clear from the 74F175 priority register C. The new interrupt level is clocked into the register and an interrupt of that level is generated by the 74F138 decoder D.
- At the same time, the interrupt vector is loaded into the 74F373 latch L.

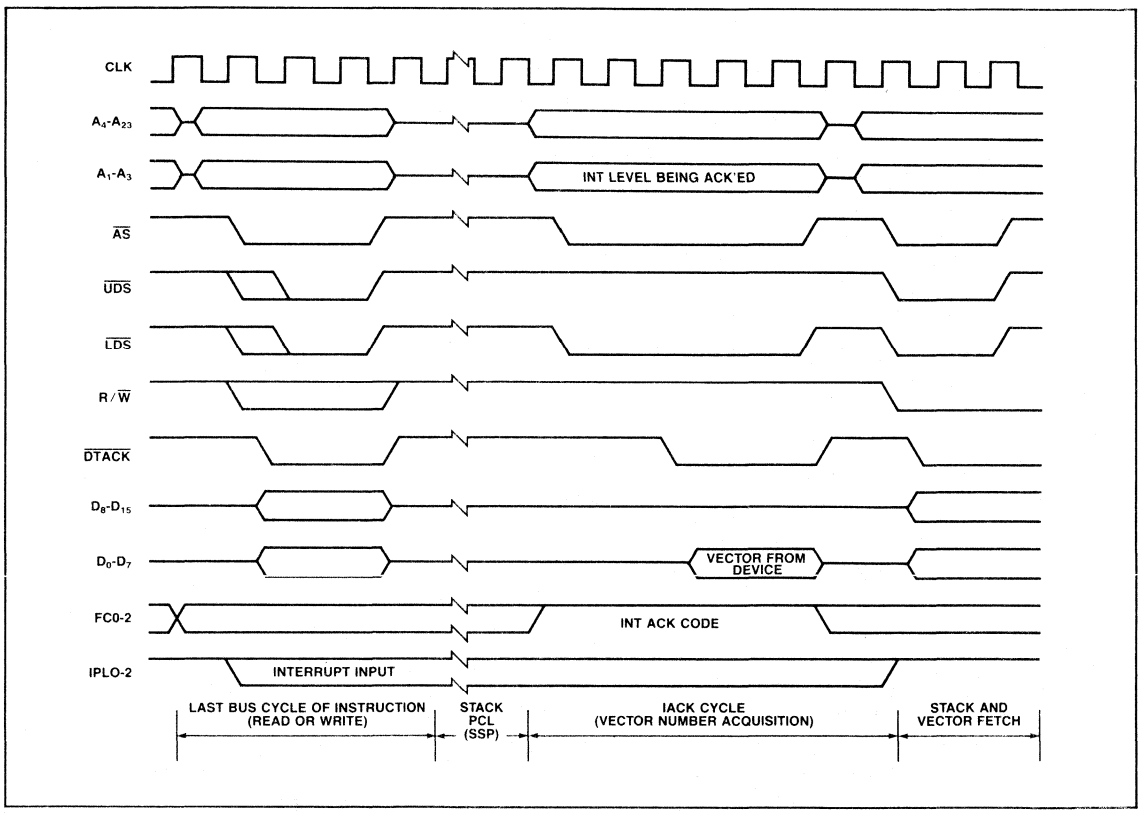


Figure 9. 68000 Interrupt Timing Diagram

- After an appropriate delay 74F73A flip-flops P and Q generate XACK*, and the cycle completes.

When the 68000 recognizes the interrupt, the following sequence occurs:

- The priority level being serviced, as indicated by the state of A_0, A_1 and A_2, is compared to the contents of the interrupt priority latch C by the 74F85 comparator B. (Note that the $\overline{Q}$ outputs of the 74F175 are used to invert the active low address signals.)
- If the levels match, the interrupt vector is placed on the data bus, XACK* is generated, and the cycle terminates. Flip-flop I is reset, which removes the interrupt by clearing the interrupt request register.

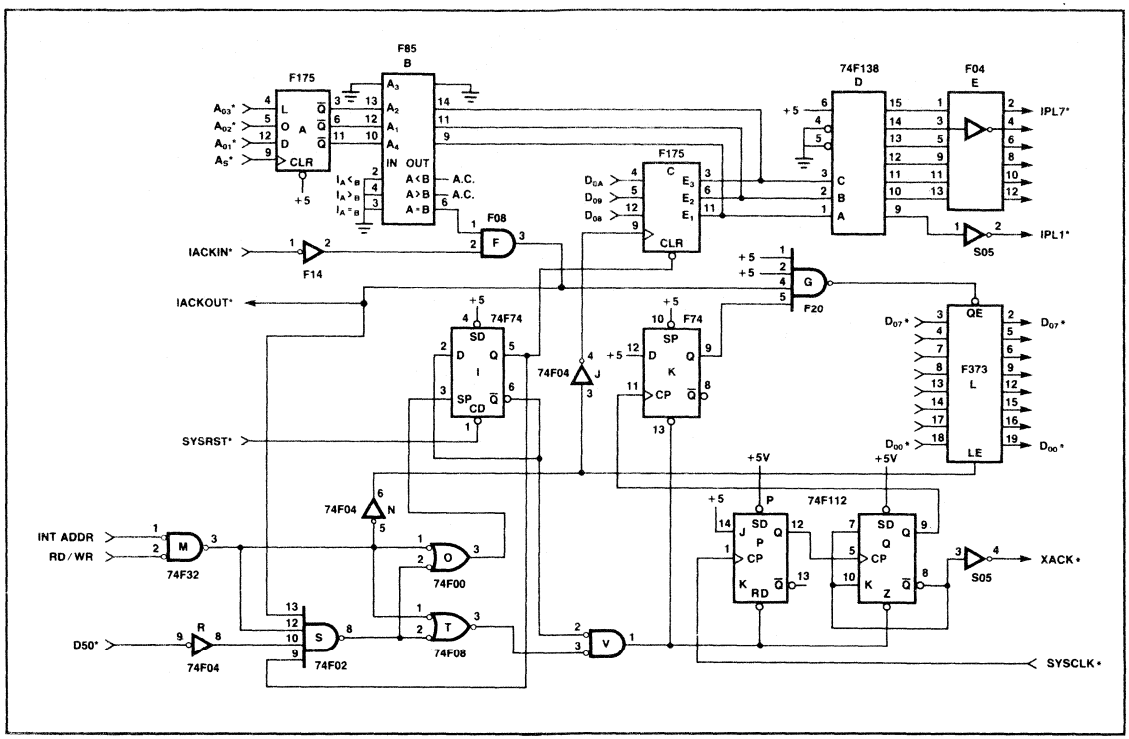


Figure 10. Complete Interrupt Circuit for 68000

BIBLIOGRAPHY

Many of the applications illustrated in this note were contributed or influenced by entries in Signetics' Interface Circuit design contest. Special thanks are due to the individuals whose entries were referenced in whole or in part in this note.

Section 7
Surface Mounted Devices

SMD PACKAGE INFORMATION

INTRODUCTION

A Surface-Mounted Device (SMD) is an electronic device which, due to advances in packaging technology, is mounted on the surface of a circuit board instead of being inserted through plated-through holes drilled in the surface. SMDs are soldered directly to bonding pads on the board. In some cases, e.g., leadless chip carriers, they must be socketed.

Throughout the years there have been rapid advances in IC design and manufacturing resulting in faster, more dense, and more reliable die. IC packaging and PC board assembly technology has finally caught up, offering much smaller packages which reduce signal paths, resulting in lower capacitance and impedance.

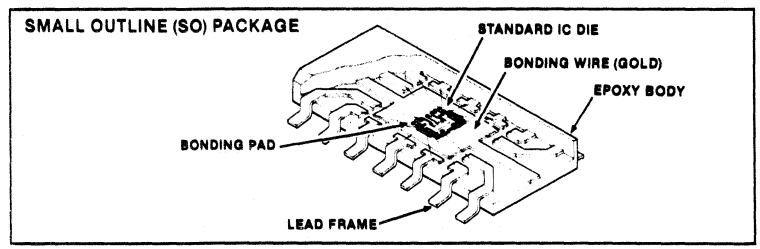
Surface-mounted PC boards are more dense and more reliable than their predecessors. Further, the automated assembly processes reduce process time, improve yields, and reduce board rework. These benefits add up to a better product at a lower price.

COMPARISON OF BASIC SMD PACKAGES

NAME	MATERIAL	SHAPE	LOCATION OF LEADS	LEAD* SPACING	LEAD CONFIGURATION	JEDEC REGISTRATION	SIGNETICS AVAILABILITY
Small Outline (SO)	Plastic	Rectangle	2 Sides	0.050 in.	Down and Out	Yes	Yes
Plastic Leaded Chip Carrier (PLCC)	Plastic	Square	4 Sides	0.050 in.	Down and Under/ J-Hook	Yes	Yes
Flatpack	Ceramic	Rectangle	2 Sides	0.050 in.	Straight out	Yes	Yes
Leadless Chip Carrier (Type C)	Ceramic	Square	4 Sides	0.050 in.	None	Yes	Yes

SO — THE WORLD'S SMALLEST PLASTIC DIP

As you can see below, there is very little difference between the assembly SO and a DIP. The major difference is that the SO is much smaller and has a different lead bend. Both DIPs and SO packages use the same materials and assembly technology.



THERMAL CHARACTERISTICS

Junction Temperature (T_J)

Actual junction temperature can be calculated using the following:

$$T_J = (P_D \times R_{\theta JA}) + T_A$$

where:

T_J = Actual Junction Temperature
P_D = Power Dissipation
$(V_{CC}\ Max) \times (I_{CC}\ Max)$
$R_{\theta JA}$ = Thermal Resistance Junction to Ambient

Example:

A device is operated at +55°C with a power dissipation of 145 mW and a $R_{\theta JA}$ of 100°C/W.

$T_J = (0.145 \times 100) + 55$
$T_J = (15) + 55$
$T_J = 70°C$

Power Dissipation (P_D)

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_D(T_A) = \frac{T_J(Max) - T_A}{R_{\theta JA}(Typ)}$$

where:

$P_D(T_A)$ = Power dissipation allowable at a given operating ambient temperature. This must be ***greater*** than the sum of the products of the supply voltages and supply currents at the worst case operating condition.
$T_J(Max)$ = Maximum operating junction temperature.
T_A = Maximum desired operating ambient temperature.
$R_{\theta JA}$ = Typical thermal resistance junction to ambient.

Example:

The maximum allowable power dissipation for a 14-pin device mounted on a ceramic substrate with maximum junction temperature $T_J = 150°C$ and maximum temperature $T_A = 70°C$.

$$P_D(70°) = \frac{150° - 70°}{130°/W}$$

$$P_D(70°) = \frac{80}{130} = 615\ mW$$

7

SMD PACKAGE INFORMATION

RELIABILITY

This section summarizes the activities undertaken by Reliability Engineering to evaluate and qualify the SO package. The evaluation demonstrated that the stress performance of the SO package is equivalent to the larger standard molded epoxy dual-in-line package in all aspects, and mounted, the package thermal resistance characteristics are exceptional considering the reduced size and mass of the package.

Evaluation Program

The evaluation/qualification program conducted in 1979 included three Analog products: LM311 Voltage Comparator, μA747 Dual Op Amp, and NE532 Dual Op Amp.

These devices encompass three wafer fabrication processes and both 8-pin and 14-pin package configurations.

All products were assembled on Alloy 42 lead frames, die attached utilizing conventional gold-silicon eutectic and molded in our standard Morton 410B epoxy Novalac compound. The devices were subjected to a series of accelerated stresses and tested to conventional data sheet parameters. Variables data were taken and drift analysis was performed.

The stress conditions employed were as follows:

- High Temperature Bias Life $T_A = 125°C$, $V_{CC} = \pm 15V$
- High Temperature Storage Life $T_A = 150°C$
- Temperature/Humidity Bias Life $T_A = 85°C$, RH = 85%, $V_{CC} = \pm 15V$
- Temperature/Humidity/Pressure (Pressure Cooker) $T_A = 121°C$, 15 PSIG 100%, Sat. Steam
- Thermal Shock (Liquid-to-Liquid) – 65°C to 150°C

Program Results

The small dimensions of the SO package raised questions on its reliability, particularly in high humidity environments. The test results, however, compare favorably to the standard dual-in-line product. Our corporate requirements for product qualification were met or exceeded. The detailed results are presented in the Reliability Evaluation Results table.

SO packaging materials are being improved. As qualification evaluations are completed, results will be made available through the SURE III program.

RELIABILITY EVALUATION RESULTS

RELIABILITY ENGINEERING PROJECT ID	SIGNETICS PRODUCT TYPE	STRESS	STRESS CONDITIONS	STRESS DURATION	CUMULATIVE RESULT	ANALYSIS
79070	LM311 (14-Lead "SO")	HTOL	125°C	2,000 hrs	1/49	1 @ 168 hrs: ball bond to trace short
		HTSL	150°C	2,000 hrs	0/50	
		Bias/ temperature/ humidity	85°C @ 85% RH $V_{CC} = 5.5V$	2,000 hrs	2/50	2 @ 2,000 hrs: internal metal corrosion
		Pressure pot	121°C 14 PSIG	432 hrs	2/51	1 @ 192 hrs: output leakage = 68 nA 1 @ 432 hrs: output leakage = 100 nA Both internal metal corrosion
		Thermal shock	– 65°C to + 150°C	1,000 ~	0/45	
790708	μA747 (14-Lead "SO")	HTOL	125°C to ± 15V	2,000 hrs	2/50	1 @ 168 hrs: $V_{OS} = 10$ mV, $V_{OS} = 7.4$ mV @ 2K hrs 1 @ 1,500 hrs: $V_{OS} = -80$ mV, $I_B = 8$ μA Suspect static damage
		HTSL	150°C	2,000 hrs	0/50	
		Bias/ temperature/ humidity	85°C @ 85% RH $V_{CC} = 5.5V$	2,000 hrs	1/50	V_{OS} rejects @ 500 hrs (– 80 mV) Suspect static damage
		Pressure pot	121°C 15 PSIG	312 hrs	3/50	3 V_{OS} rejects @ 312 hrs (~ 8 mV)
		Thermal shock	– 65°C to + 150°C	1,000 ~	1/48	V_{OS} rejects @ 700 ~ (– 170 mV, $I_B = 14$ μA) Suspect static damage
795003	NE532 (8-Lead "SO")	HTOL	150°C	2,000 hrs	0/45	To 500 hrs, 0/18 from 500 to 2,000 hrs (due to capacity limitations)
		HTSL	150°C	2,000 hrs	0/46	
		Bias/ temperature/ humidity	85°C @ 85% RH	2,000 hrs	2/49	1 @ 1,500, 1 @ 2,000 hrs Both output sink current failures due to corrosion
		Pressure pot	121°C 15 PSIG	456 hrs	1/43	Output sink current @ 288 hrs
		Thermal shock	– 65°C to + 150°C	1,000 ~	1/45	V_{OS} rejects @ 200 ~ (15 mV)

SMD PACKAGE INFORMATION

SO PACKAGE THERMAL DATA

PACKAGE TYPE	PACKAGE MOUNTING TECHNIQUE*	MAX. ALLOWABLE POWER DISSIPATION (mW) AT 25°C	MAX. ALLOWABLE POWER DISSIPATION (mW) AT 70°C	THERMAL RESISTANCE (θ_{JA}°C/Watt)	
				Average	Maximum
SO-14	PCB	658	421	190	225
	Ceramic	962	615	130	165
	Ceramic w/H.S.	1471	941	85	110
SO-16	PCB	862	551	145	170
	Ceramic	1250	800	100	125
	Ceramic w/H.S.	1923	1231	65	85
SO-16L	PCB	1250	800	100	140
	Ceramic	1743	1143	70	100
	Ceramic w/H.S.	2500	1600	50	65
SO-20	PCB	1471	941	85	115
	Ceramic	2273	1454	55	85
	Ceramic w/H.S.	3572	2286	35	55
SO-24	PCB	1563	1000	80	110
	Ceramic	2000	1600	50	80
	Ceramic w/H.S.	4167	2667	30	50

NOTES
1. PCB = Printed circuit board
2. Ceramic = Alumina substrate
3. Ceramic w/H.S. = Alumina substrate with heat sink and/or thermal compound

*Air gap between package and surface is 0.006-inch unless thermal compound is used.

PACKAGE AVAILABILITY

COMMERCIAL PACKAGES				MILITARY (CERAMIC) PACKAGES	
Pin Count	SO 0.150 Wide	SOL 0.300 Wide	PLCC	Leadless Chip Carrier	Flatpack
8	Available	—	—	—	—
14	Available	—	—	—	Available
16	Available	Available	—	—	Available
20	—	Available	—	Available	—
24	—	Available	—	Available	Available
28	—	Available	—	Available	—
44	—	—	1984	Available	—
52	—	—	—	Available	Available
68	—	—	—	Available	Available
84	—	—	—	—	—

TECHNOLOGIES AVAILABLE IN SIGNETICS SURFACE-MOUNTED PACKAGES

PACKAGE TYPE	PRODUCT TYPES	AVAILABILITY
SO-14	CMOS-4000, TTL-S, TTL-LS, TTL-Std.	Now
SO-14	High-Speed CMOS, TTL-Fast	1984
SO-16	CMOS-4000, TTL-S, TTL-LS, TTL-Std.	Now
SO-16	High-Speed CMOS, TTL-Fast	1984
SO-16L	TTL-S, TTL-LS, TTL-Std.	Now
SO-16L	TTL-Fast	1984
SO-20	TTL-S, TTL-LS	Now
SO-20	TTL-Fast, High-Speed CMOS	1984
SO-24	TTL-Fast, High-Speed CMOS	1984
SO-28	TTL-Fast	1984

SMD PACKAGE INFORMATION

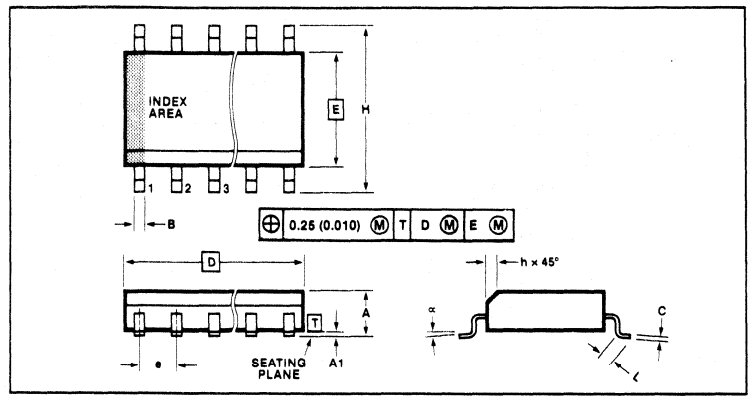
PACKAGE OUTLINE/JEDEC REGISTRATION

The following SO package outlines have been registered with the JC11.3 committee of the Joint Electronic Devices Engineering Council of the Electronics Industry Association:

SO-8 SO-20
SO-14 SO-24
SO-16 SO-28
SO-16L

Outlines and dimensions for each package are shown below:

A. Dimensions and tolerancing per ANSI Y14.5-1973.
B. "T" is a reference datum.
C. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (0.006 in.).
D. The chamfer on the body is used to designate pin 1. The beveled side to the left denotes lead number 1.
E. "L" is the length of terminal for soldering to a substrate.
F. Controlling dimension: Millimeter.



MILLIMETERS

Symbol	SO 8-PIN Min.	SO 8-PIN Max.	SO 14-PIN Min.	SO 14-PIN Max.	SO 16-PIN Min.	SO 16-PIN Max.	SOL 16L-PIN Min.	SOL 16L-PIN Max.	SOL 20-PIN Min.	SOL 20-PIN Max.	SOL 24-PIN Min.	SOL 24-PIN Max.	SOL 28-PIN Min.	SOL 28-PIN Max.	Notes
A	1.35	1.75	1.35	1.75	1.35	1.75	2.35	2.65	2.35	2.65	2.35	2.65	2.35	2.65	
A_1	0.10	0.25	0.10	0.25	0.10	0.25	0.10	0.30	0.10	0.30	0.10	0.30	0.10	0.30	
B	0.35	0.49	0.35	0.49	0.35	0.49	0.35	0.49	0.35	0.49	0.35	0.49	0.35	0.49	
C	0.19	0.25	0.19	0.25	0.19	0.25	0.23	0.32	0.23	0.32	0.23	0.32	0.23	0.32	
D	4.80	5.00	8.55	8.75	9.80	10.00	10.1	10.5	12.6	13.0	15.2	15.6	17.7	18.1	C
E	3.80	4.00	3.80	4.00	3.80	4.00	7.4	7.6	7.4	7.6	7.4	7.6	7.4	7.6	C
e	1.27 BSC		1.27 BSC		1.27 BSC		1.27 BSC		1.27 BSC		1.27 BSC		1.27 BSC		
H	5.80	6.20	5.80	6.20	5.80	6.20	10.00	10.65	10.00	10.65	10.00	10.65	10.00	10.65	
L	0.40	1.27	0.40	1.27	0.40	1.27	0.40	1.27	0.40	1.27	0.40	1.27	0.40	1.27	E
α	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°	
h	0.25	0.50	0.25	0.50	0.25	0.50	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75	D

INCHES

Symbol	SO 8-PIN Min.	SO 8-PIN Max.	SO 14-PIN Min.	SO 14-PIN Max.	SO 16-PIN Min.	SO 16-PIN Max.	SOL 16L-PIN Min.	SOL 16L-PIN Max.	SOL 20-PIN Min.	SOL 20-PIN Max.	SOL 24-PIN Min.	SOL 24-PIN Max.	SOL 28-PIN Min.	SOL 28-PIN Max.	Notes
A	0.053	0.069	0.053	0.069	0.053	0.069	0.093	0.104	0.093	0.104	0.093	0.104	0.093	0.104	
A_1	0.004	0.010	0.004	0.010	0.004	0.010	0.004	0.012	0.004	0.012	0.004	0.012	0.004	0.012	
B	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	
C	0.007	0.010	0.007	0.010	0.007	0.010	0.009	0.013	0.009	0.013	0.009	0.013	0.009	0.013	
D	0.189	0.197	0.337	0.344	0.386	0.394	0.398	0.413	0.496	0.512	0.598	0.614	0.647	0.713	C
E	0.150	0.157	0.150	0.157	0.150	0.157	0.2914	0.2992	0.2914	0.2992	0.2914	0.2992	0.2914	0.2992	C
e	0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		
H	0.228	0.244	0.228	0.244	0.228	0.244	0.394	0.419	0.394	0.419	0.394	0.419	0.394	0.419	
h	0.010	0.02	0.010	0.02	0.010	0.02	0.010	0.30	0.010	0.30	0.010	0.30	0.010	0.30	D
L	0.016	0.050	0.016	0.050	0.016	0.050	0.016	0.050	0.016	0.050	0.016	0.050	0.016	0.050	E
α	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°	

Section 8
Military Products

MILITARY PRODUCTS/ PROCESS LEVELS

The Signetics MIL-M-38510 and MIL-STD-883 Programs are organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. These programs are designed to provide our customers:

- Fully compliant 883/M5004 flows on all products.
- Standard processing flows to help minimize the need for custom specifications.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allow customers to buy products off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specifications.

The following explains the different processing options available. Special device marking clearly distinguishes the type of screening performed. Refer to Tables 2 and 3.

Table 1 MILITARY PACKAGE AVAILABILITY

JAN CASE OUTLINE AND LEAD FINISH	SIGNETICS MILITARY PACKAGE TYPES					
	CERAMIC					
	8-PIN	14-PIN	16-PIN	18-PIN	20-PIN	24-PIN
PB	FE	—	—	—	—	—
CB	—	F	—	—	—	—
EB	—	—	F	—	—	—
JB	—	—	—	—	—	F
DB	—	W	—	—	—	—
FB	—	—	W	—	—	—
RB	—	—	—	—	F	—
VB	—	—	—	F	—	—

All products listed are also available in Die form.

Table 2 MILITARY SUMMARY

	JS	JB	RB
	JAN QUALIFIED		883B
54	X	X	X
54LS	X	X	X
54S	X	X	X
54F	—	—	X
82	—	—	X
8T	—	—	X
93XX	—	X	X
96XX	—	—	X
Analog	—	X	X
Bipolar Memory	—	X	X
Microprocessor	—	—	X

JAN QUALIFIED (JS and JB)

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M-38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List (QPL 38510).

Quality conformance inspection testing, per MIL-STD-883, Method 5005, is performed according to Mil-M-38510 as follows:

- Group A; each sublot. (Alternate Group A)
- Group B; one sublot for each package type every week. (Alternate Group B)
- Group C; one sublot for each microcircuit group every 13 weeks.
- Group D; one sublot for each package type every 26 weeks.

NOTE: This category of part conforms to Quality Level B ($\pi_Q = 1.0$) of MIL-HDBK-217D.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

By implementing this government standardization program, Signetics complies with the trend of reducing the numerous similar Source Control Drawings (SCD's). This standardized trend results in a *single* complete and comprehensive specification, a *single* product flow, and a *single* administrative effort—for both the aerospace community and for Signetics. Because the list of Signetics' qualified products will change periodically, you may wish to contact your nearest Signetics' Sales Office or refer to the *Products Qualified* under Military Specification from DESC for our current update.

JAN Class S products are quoted on a unit price basis only (similar to present Class B programs). There will be no lot charges for SEM inspection, electrical testing, or Group B or D quality conformance inspection. All additional charges are amortized in the unit price.

Package types currently qualified are:
1) Cerdip—ceramic dual-in-line
2) Cerpac—ceramic flat pack

Government Source Inspection (GSI) is a requirement of the JAN 38510 Class S specification. No alterations to this specification may be instituted. Therefore, the only allowed customer source inspection option is at pre-ship (verification only).

Additional program data options (such as wafer lot acceptance, attributes, Group B, D, and others) are available upon request for a nominal fee.

MIL-STD-883, LEVEL B

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to MIL-STD-883 Method 5004, and is 100% electrically tested to Signetics data sheets.

Quality conformance inspection per MIL-STD-883, Method 5005, Group A, is performed on each sublot. Group A subgroup electrical parameters are those included in the detailed Signetics data book. Contact the factory for parametric subgroup assignments.

Generic quality conformance data per Method 5005, Groups B, C, and D, is generally available on popular device types and packages, but availability is not guaranteed. The factory must be consulted

prior to ordering generic data. When available, generic data is defined as follows:

- Group B: Performed once per package type every six weeks of seal.
- Group C: Performed once per microcircuit group every 52 weeks of seal.
- Group D: Performed once per package type every 52 weeks of seal.

Quality conformance endpoint electrical parameters for Groups C and D are the Group A subgroups 1, 2, and 3.

Copies of generic data, Groups A, B, C, and D, may be ordered by customers at a nominal charge.

NOTE: This category of part conforms of Quality Level B-2 ($\pi_Q = 6.5$) of MIL-HDBK-217D.

Table 3. REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 and MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS		
			JAN CLASS S	JAN QUALIFIED (B)	883
General Mil-M-38510 1. Pre-Certification A. Product Assurance Program B. Manufacturer's Certification	The Manufacturer shall establish and implement a Products Assurance Program Plan and provide for a manufacturer survey by the qualifying activity.	—	X	X	N/A
2. Certification	Received after manufacturer has completed a successful DESC survey.	—	X	X	N/A
3. Device Qualification	Device qualification shall consist of subjecting the desired device to Groups A, B, C, and D of Method 5005.	—	X	X	N/A
4. Traceability	Traceability maintained back to wafer production lots.	—	X	X	X
5. Country of Origin	Devices must be manufactured, assembled, and tested within the U.S. or its territories.	—	X	X	N/A
Screening Per Method 5004 of Mil-Std-883					
6. Non-Destructive Bond Pull	2023	100%	×	N/A	N/A
7. Internal Visual (Precap)	2010, Cond. A or B	100%	A	B	B
8. Stabilization Bake	1008, Cond. C Min	100%	×	×	×
9. Temperature Cycling	1010, Cond. C; (10 cycles, -65°C to +150°C)	100%	×	×	×
10. Constant Acceleration	2001 Cond. E; Y1 (30 kg in Y1 Plane)	100%	×	×	×
11. Visual Inspection	There is no test method for this screen; it is intended only for the removal of Catastrophic Failures defined as Missing Leads, Broken Packages or Lids Off.	100%	×	×	×
12. Seal (Hermeticity) A. Fine B. Gross	 1014 Cond. A or B; (5.0×10^{-8} CC/Sec) 1014 Cond. C.	 100% 100%	 × ×	 × ×	 × ×
13. Marking	Fungus inhibiting ink	100%	X	×	×
14. Particle Impart Noise Test	2020, Cond. A	100%	×	N/A	N/A
15. Radiographic	2012; two views	100%	×	N/A	N/A
16. Interim Electricals (Pre Burn-In)	Per applicable device specification	100%	×	Optional	Optional
17. Burn-In	1015, Cond. as specified (160 hrs. Min at 125°C Min)	100%	240 hrs.	×	×

Table 3. REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS (Continued)

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 and MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS		
			JAN CLASS S	JAN QUALIFIED (B)	883
18. Final Electricals	Per applicable device specification	100%	100% Read & Record	Slash Sheet	Data Sheet
a. Static Tests @25°C	Subgroup 1		×	×	×
b. Static Tests @ + 125°C	Subgroup 2		×	×	×
c. Static Tests @ – 55°C	Subgroup 3		×	×	×
d. Dynamic Test @25°C	Subgroup 4 (for Linear Products only)		×	×	×
e. Functional Test @25°C	Subgroup 7		×	×	×
f. Switching Test @25°C	Subgroup 9		×	×	×
g. Switching Test @ temperature	Subgroup 10, 11, (as applicable)		×	×	×
19. Percent Defective Allowable (PDA)	A PDA of 10% is a requirement applied against the static tests @25°C (A-1). This is controlled by the slash sheets for JAN products. For RB, 10% is standard.	10%	5%	×	×
20. External Visual	2009	100%	×	×	×
Quality Conformance Inspection per Method 5005 of Mil-Std 883	**ATTRIBUTE DATA ONLY**				
21. Group A	Electrical Tests — Final Electricals (#18 above) repeated on a sample basis (Subgroups 1 through 12 as specified) performed in line with final electricals.	Each sublot	×	×	×
22. Group B	Package functional and constructional related test (package dimensions; resistance to solvents; internal, visual, and mechanical bond strength; and solderability).	Each pkg. type	Each sublot	Each week of seal	Generic
23. Group C	Die related tests (1,000 hour operating life, temperature cycling, and constant acceleration.	Each μcircuit group	N/A	Each 13 weeks of seal	Generic
24. Group D.	Package related tests (physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration, variable frequency, constant acceleration, and salt atmosphere).	Each pkg. type	Each 26 weeks of seal	Each 26 weeks of seal	Generic

MILITARY PRODUCTS GUIDE

ORDERING INFORMATION

The Signetics Military Products are available in a variety of different process levels and several different packages. The correct ordering code or part number for the devices is an alphanumeric sequence as explained below. Not all devices are available in all the packages. The ordering codes on the individual data sheets indicate the present or planned availability of the products. However, availability of specific part numbers can be obtained from your local sales office or franchised distributor.

Ordering Code

1) JM38510/07801BJB

- B — LEAD FINISH
- J — PACKAGE TYPE
- 07801 — CLASS "B"
- 38510 — SLASH SHEET NUMBER (BASIC DEVICE TYPE)
- JM — JAN QUALIFIED

2) JB54S181F

- F — PACKAGE TYPE
- 54S181 — BASIC DEVICE TYPE
- B — CLASS "B"
- J — JAN QUALIFIED

3) S54S181F883B

- B — LEVEL "B"
- 883 — MIL-STD-883
- F — PACKAGE TYPE
- 54S181 — BASIC DEVICE TYPE
- S — MILITARY TEMPERATURE RANGE (—55 TO 125°C)

4) RB54S181F

- F — PACKAGE TYPE
- 54S181 — BASIC DEVICE TYPE
- RB — MIL-STD-883, LEVEL "B"

NOTE:
1) and 2) JAN qualified products.
3) and 4) Non-JAN MIL-STD-883 products.

For minimum quantity orders, contact your local Signetics sales representative.

PACKAGES AVAILABLE*

F = Ceramic DIP
i = Ceramic DIP
G = Ceramic Leadless Chip Carrier
W = Ceramic Flatpack

* See Package Outlines section for more information

For the latest military product information, please request a Military Products Guide from Publications Services, 408/746-2111.

Section 9
Package Outlines

PACKAGE OUTLINES

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
   a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative.
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power applications across V_{CC} and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

Plastic Only

5. Lead material: Olin 194 (Copper Alloy) or equivalents, solder dipped.
6. Body material: Plastic (Epoxy)
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.

Hermetic Only

9. Lead material
   a. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
   b. ASTM alloy F-30 (Alloy 42) or equivalent—tin plated, gold plated, or solder dipped.
   c. ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
10. Body Material
    a. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
    b. Ceramic with glass seal at leads.
    c. BeO ceramic with glass seals at leads.
    d. Ceramic with ASTM alloy F-30 or equivalent.
11. Lid Material
    a. Nickel or tin plated nickel, weld seal.
    b. Ceramic, glass seal.
    c. ASTM alloy F-15 or equivalent, gold plated, alloy seal.
    d. BeO ceramic with glass seal.
12. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
13. Recommended minimum offset before lead bend.
14. Maximum glass climb 0.010 inches.
15. Maximum glass cimb or lid skew is 0.010 inches.
16. Typical four places.
17. Dimension also applied to seating plane.

PACKAGE OUTLINES

PLASTIC PACKAGES

NO. OF LEADS	PACKAGE CODE	Θ_{ja}/Θ_{jc} (°C/W)[2]	DESCRIPTION
SO Packages			
14-Pin	D	NA	SO-14
16-Pin	D	NA	SO-16
16L-Pin	D	NA	SO-16L
20-Pin	D	NA	SO-20
24-Pin	D	NA	SO-24
28-Pin	D	NA	SO-28
Standard Dual-In-Line Packages			
14-Pin	N	86/48	
16-Pin	N	83/42	
20-Pin	N	61/24	
24-Pin	N	52/23	
28-Pin	N	85/23	

NOTE
1. For SO packages θ_{ja} (°C/W) only

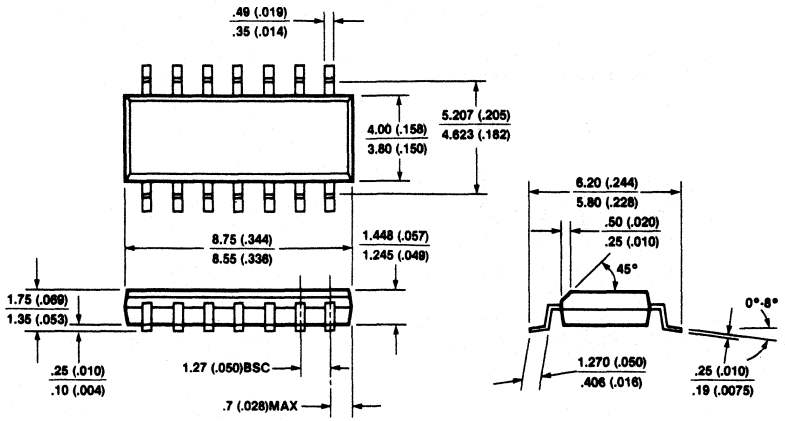
HERMITIC PACKAGES FOR MILITARY ONLY

NO. OF LEADS	PACKAGE CODE	Q_{ja}/Q_{jc} (°C/W))	DESCRIPTION
Cerdip Family			
14-Pin	F	110/30	Dual-In-Line Ceramic
16-Pin	F	100/30	Dual-In-Line Ceramic
20-Pin	F	90/25	Dual-In-Line Ceramic
24-Pin	F	60/26	Dual-In-Line Ceramic
Flat Packs			
14-Pin	W	205/50	Flat Ceramic
16-Pin	W	200/50	Flat Ceramic
28-Pin	W	107/22	Flat Ceramic, BEO
Leadless Chip Carrier			
20-Pin	G		Laminated Ceramic Side Brazed Lead

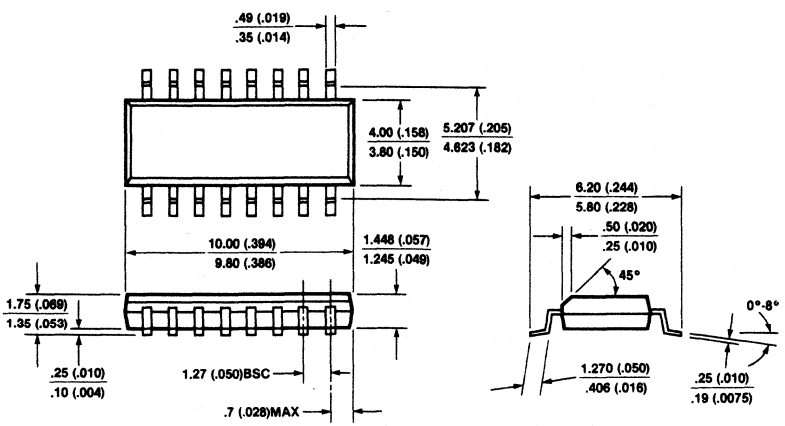
Package Type
D = Small Outline Plastic DIP
F = Cerdip
G = Hermetic Leadless
N = Plastic DIP
W = Ceramic Flatpack

PACKAGE OUTLINES

SO-14 PACKAGE
(14-PIN)



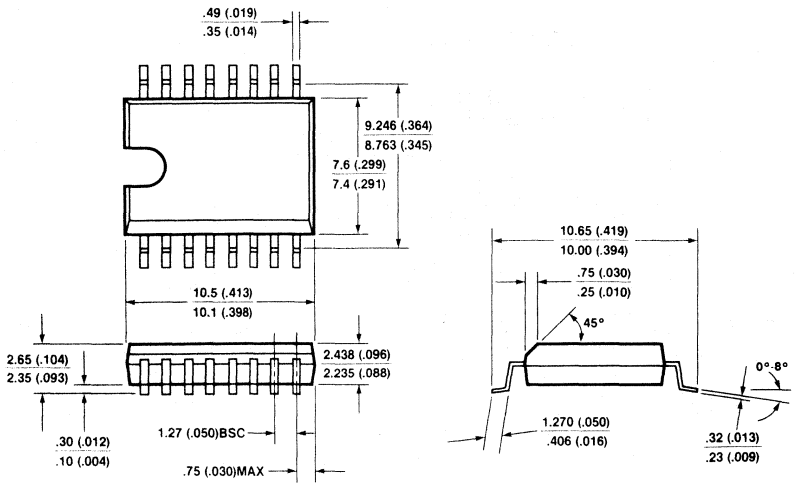
SO-16 PACKAGE
(16-PIN)



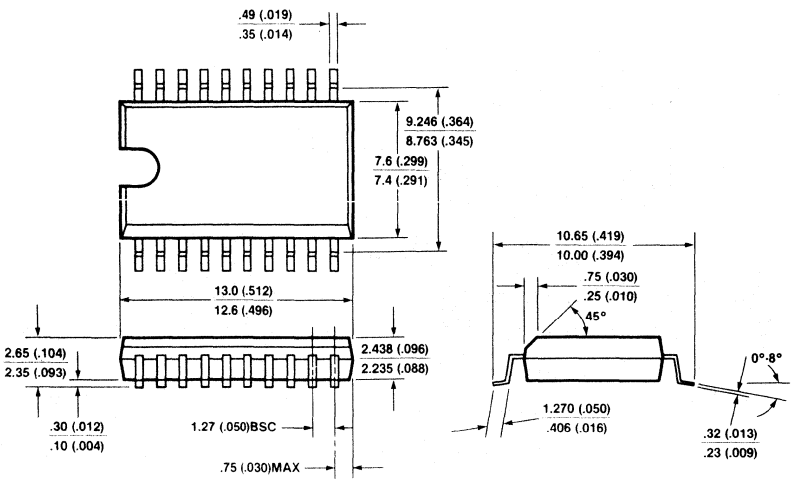
9

PACKAGE OUTLINES

SO-16L PACKAGE (16-PIN)

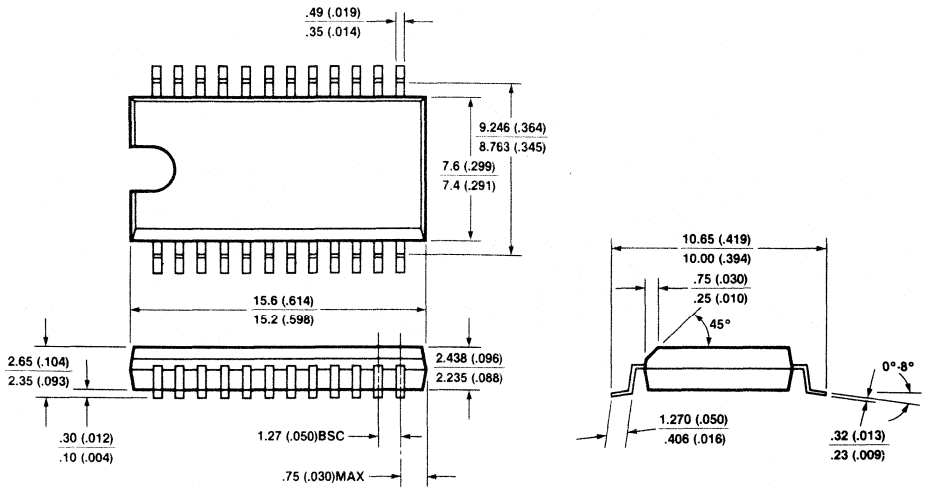


SO-20L PACKAGE (20-PIN)

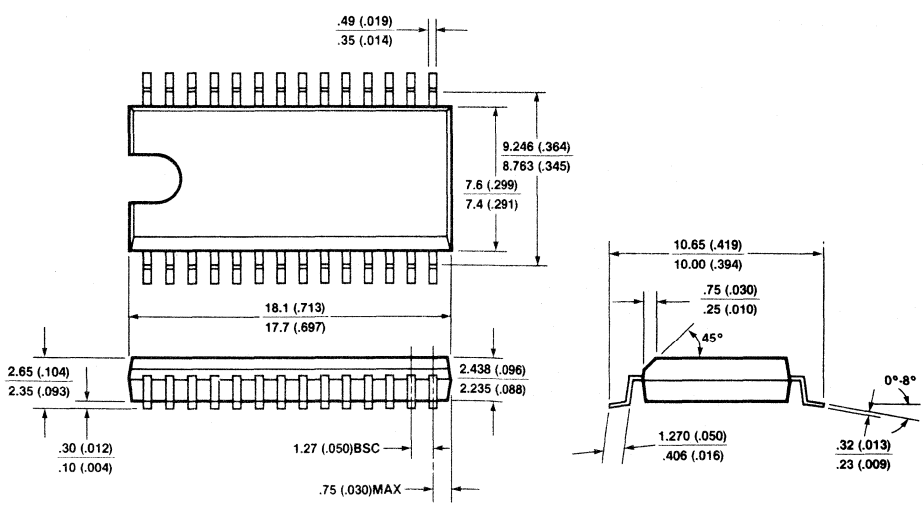


PACKAGE OUTLINES

SO-24 PACKAGE (24-PIN)



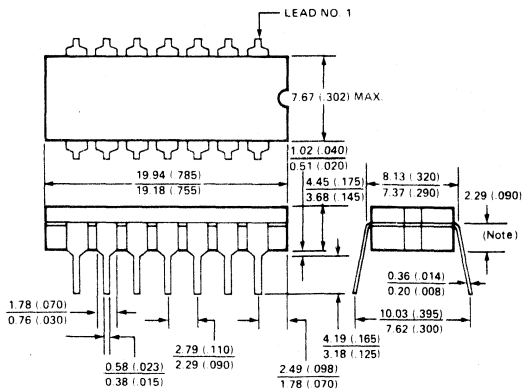
SO-28L PACKAGE (28-PIN)



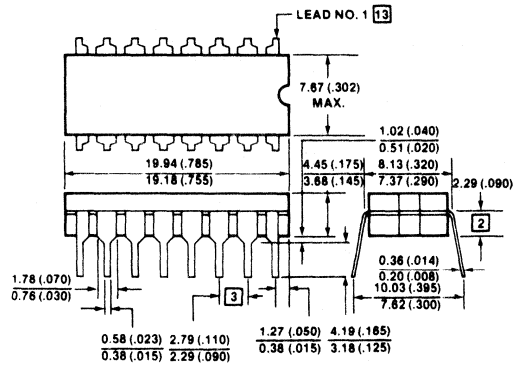
9

PACKAGE OUTLINES

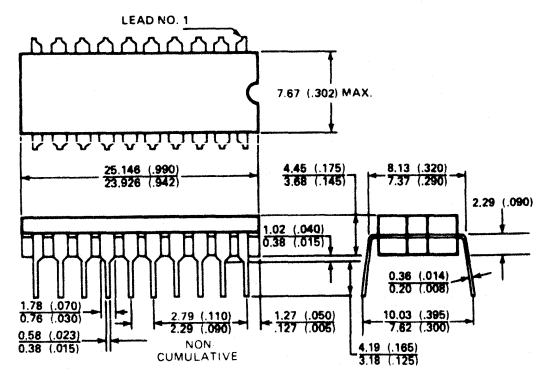
F PACKAGE CERAMIC (14-PIN DIP)



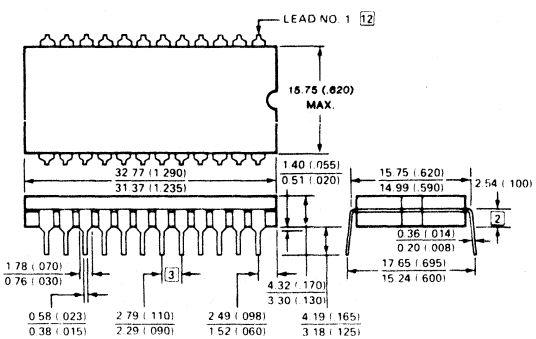
F PACKAGE CERAMIC (16-PIN DIP)



F PACKAGE CERAMIC (20-PIN DIP)

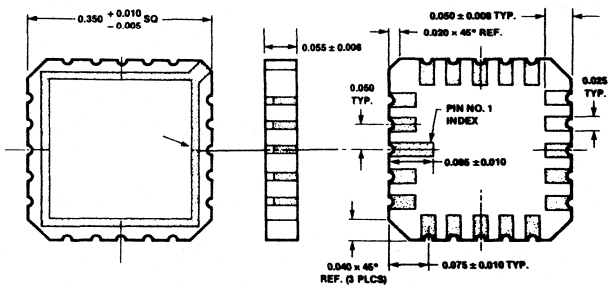


F PACKAGE CERAMIC (24-PIN DIP)

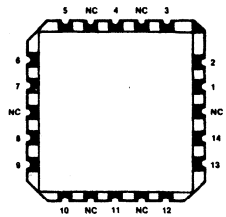


PACKAGE OUTLINES

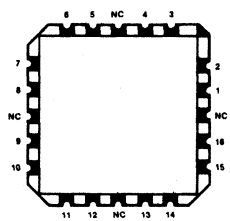
G PACKAGE



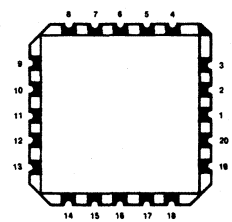
G PACKAGE (14-PIN)



G PACKAGE (16-PIN)



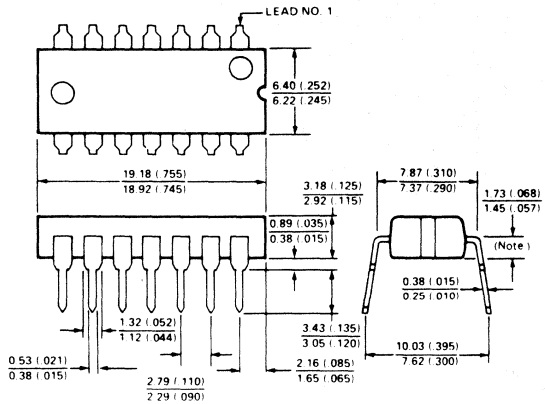
G PACKAGE (20-PIN)



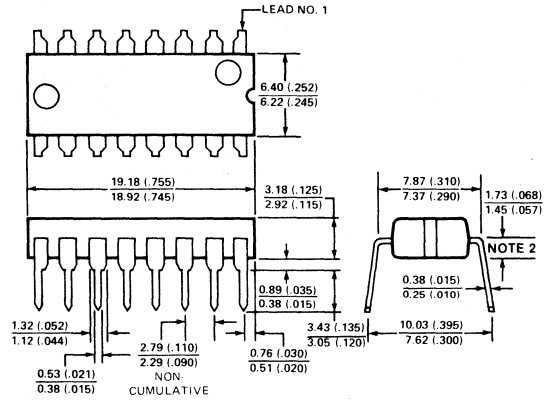
9

PACKAGE OUTLINES

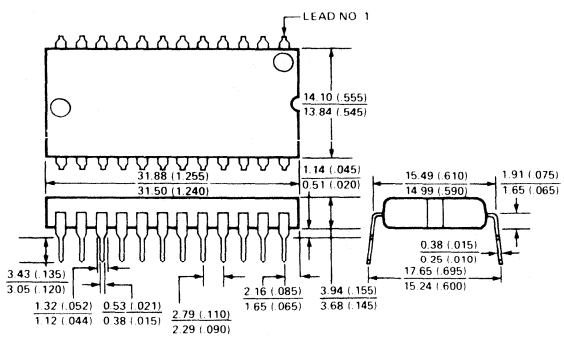
N PACKAGE PLASTIC
(14-PIN DIP)



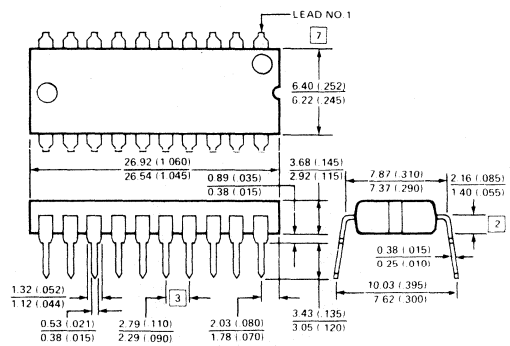
N PACKAGE PLASTIC
(16-PIN DIP)



N PACKAGE PLASTIC
(20-PIN DIP)

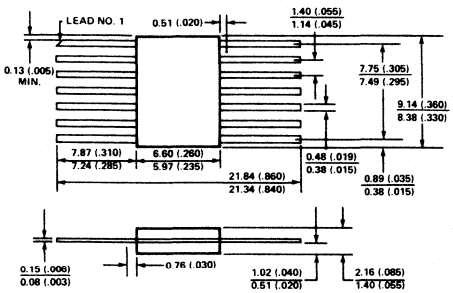


N PACKAGE PLASTIC
(24-PIN DIP)

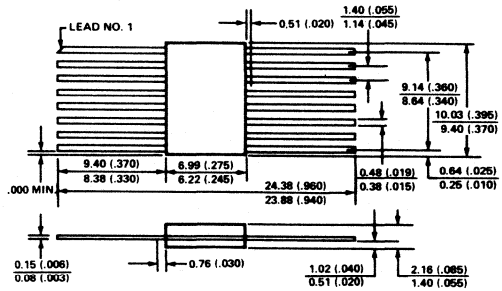


PACKAGE OUTLINES

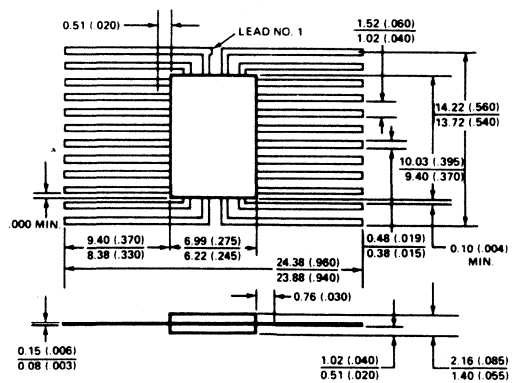
W PACKAGE CERAMIC
(14-PIN FLATPACK)



W PACKAGE CERAMIC
(16-PIN FLATPACK)



W PACKAGE CERAMIC
(24-PIN FLATPACK)



9

NOTES

Electronic components and materials for professional, industrial and consumer uses from the world-wide Philips Group of Companies

Argentina: PHILIPS ARGENTINA S.A., Div. Elcoma, Vedia 3892, 1430 BUENOS AIRES, Tel. 541-7141/7242/7343/7444/7545.
Australia: PHILIPS INDUSTRIES HOLDINGS LTD., Elcoma Division, 67 Mars Road, LANE COVE, 2066, N.S.W., Tel. 427 0888.
Austria: ÖSTERREICHISCHE PHILIPS BAUELEMENTE INDUSTRIE G.m.b.H., Triester Str. 64, A-1101 WIEN, Tel. 629111.
Belgium: N.V. PHILIPS & MBLE ASSOCIATED, 9 rue du Pavillon, B-1030 BRUXELLES, Tel. (02) 242 7400.
Brazil: IBRAPE, Caixa Postal 7383, Av. Brigadeiro Faria Lima, 1735 SAO PAULO, SP, Tel. (011) 211-2600.
Canada: PHILIPS ELECTRONICS LTD., Electron Devices Div., 601 Milner Ave., SCARBOROUGH, Ontario, M1B 1M8, Tel. 292-5161.
Chile: PHILIPS CHILENA S.A., Av. Santa Maria 0760, SANTIAGO, Tel. 39-4001.
Colombia: SADAPE S.A., P.O. Box 9805, Calle 13, No.51 + 39, BOGOTA D.E. 1., Tel. 600600.
Denmark: MINIWATT A/S, Strandlodsvej 2, P.O. Box 1919, DK 2300 COPENHAGEN S, Tel. (01) 54 11 33.
Finland: OY PHILIPS AB, Elcoma Division, Kaivokatu 8, SF-00100 HELSINKI 10, Tel. 172 71.
France: R.T.C. LA RADIOTECHNIQUE-COMPELEC, 130 Avenue Ledru Rollin, F-75540 PARIS 11, Tel. 338 80-00.
Germany (BRD): VALVO, UB Bauelemente der Philips G.m.b.H., Valvo Haus, Burchardstrasse 19, D-2 HAMBURG 1, Tel. (040) 3296-0.
Greece: PHILIPS S.A. HELLENIQUE, Elcoma Division, 52, Av. Syngrou, ATHENS, Tel. 9215111.
Hong Kong: PHILIPS HONG KONG LTD., Elcoma Div., 15/F Philips Ind. Bldg., 24-28 Kung Yip St., KWAI CHUNG, Tel. (0)-245121.
India: PEICO ELECTRONICS & ELECTRICALS LTD., Elcoma Div., Ramon House, 169 Backbay Reclamation, BOMBAY 400020, Tel. 221012.
Indonesia: P.T. PHILIPS-RALIN ELECTRONICS, Elcoma Div., Panim Bank Building, 2nd Fl., Jl. Jend. Sudirman, P.O. Box 223, JAKARTA, Tel. 716131.
Ireland: PHILIPS ELECTRICAL (IRELAND) LTD., Newstead, Clonskeagh, DUBLIN 14, Tel. 693355.
Italy: PHILIPS S.p.A., Sezione Elcoma, Piazza IV Novembre 3, I-20124 MILANO, Tel. 2-6752.1.
Japan: NIHON PHILIPS CORP., Shuwa Shinagawa Bldg., 26-33 Takanawa 3-chome, Minato-ku, TOKYO (108), Tel. 448-5611.
(IC Products) SIGNETICS JAPAN LTD., 8-7 Sanbancho Chiyoda-ku, TOKYO 102, Tel. (03) 230-1521.
Korea (Republic of): PHILIPS ELECTRONICS (KOREA) LTD., Elcoma Div., Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. 794-4202.
Malaysia: PHILIPS MALAYSIA SDN. BERHAD, No. 4 Persiaran Barat, Petaling Jaya, P.O.B. 2163, KUALA LUMPUR, Selangor, Tel. 774411.
Mexico: ELECTRONICA, S.A de C.V., Carr. Mexico-Toluca km. 62.5, TOLUCA, Edo. de Mexico 50140, Tel. Toluca 91 (721) 613-00.
Netherlands: PHILIPS NEDERLAND, Marktgroep Elonco, Postbus 90050, 5600 PB EINDHOVEN, Tel. (040) 793333.
New Zealand: PHILIPS ELECTRICAL IND. LTD., Elcoma Division, 110 Mt. Eden Road, C.P.O. Box 1041, AUCKLAND, Tel. 605-914.
Norway: NORSK A/S PHILIPS, Electronica Dept., Sandstuveien 70, OSLO 6, Tel. 680200.
Peru: CADESA, Av. Alfonso Ugarte 1268, LIMA 5, Tel. 326070.
Philippines: PHILIPS INDUSTRIAL DEV. INC., 2246 Pasong Tamo, P.O. Box 911, Makati Comm. Centre, MAKATI-RIZAL 3116, Tel. 86-89-51 to 59.
Portugal: PHILIPS PORTUGUESA S.A.R.L., Av. Eng. Duarte Pacheco 6, 1009 LISBOA Codex, Tel. 683121.
Singapore: PHILIPS PROJECT DEV. (Singapore) PTE LTD., Elcoma Div., Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. 2538811.
South Africa: EDAC (PTY.) LTD., 3rd Floor Rainer House, Upper Railway Rd. & Ove St., New Doornfontein, JOHANNESBURG 2001, Tel. 614-2362/9.
Spain: MINIWATT S.A., Balmes 22, BARCELONA 7, Tel. 3016312.
Sweden: PHILIPS KOMPONENTER A.B., Lidingövägen 50, S-11584 STOCKHOLM 27, Tel. 08/7821000.
Switzerland: PHILIPS A.G., Elcoma Dept., Allmendstrasse 140-142, CH-8027 ZÜRICH, Tel. 01-4882211.
Taiwan: PHILIPS TAIWAN LTD., 3rd Fl., San Min Building, 57-1, Chung Shan N. Rd, Section 2, P.O. Box 22978, TAIPEI, Tel. (02)-5631717.
Thailand: PHILIPS ELECTRICAL CO. OF THAILAND LTD., 283 Silom Road, P.O. Box 961, BANGKOK, Tel. 233-6330-9.
Turkey: TÜRK PHILIPS TICARET A.S., EMET Department, Inonu Cad. No. 78-80. ISTANBUL, Tel. 435910.
United Kingdom: MULLARD LTD., Mullard House, Torrington Place, LONDON WC1E 7HD, Tel. 01-5806633.
United States: (Active Devices & Materials) AMPEREX SALES CORP., Providence Pike, SLATERSVILLE, R.I. 02876, Tel. (401) 762-9000.
(Passive Devices) MEPCO/ELECTRA INC., Columbia Rd., MORRISTOWN, N.J. 07960, Tel. (201) 539-2000.
(Passive Devices & Electromechanical Devices) CENTRALAB INC., 5855 N. Glen Park Rd., MILWAUKEE, WI 53201, Tel. (414)228-7380.
(IC Products) SIGNETICS CORPORATION, 811 East Arques Avenue, SUNNYVALE, California 94086, Tel. (408) 739-7700.
Uruguay: LUZILECTRON S.A., Avda Uruguay 1287, P.O. Box 907, MONTEVIDEO, Tel. 914321.
Venezuela: IND. VENEZOLANAS PHILIPS S.A., Elcoma Dept., A. Ppal de los Ruices, Edif. Centro Colgate, CARACAS, Tel. 360511

For all other countries apply to: Philips Electronic Components and Materials Division, International Business Relations, Building BAE-3, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Tel. +31 40 72 33 04, Telex 35000 phtcnl

A40

Printed in The Netherlands

9398 125 60011